MP7612

Octal 12-Bit DAC Array™
D/A Converter with Output Amplifier
and Serial Data/Address
µP Control Logic

EXAR ...the analog plus company™

April 1996-4

FEATURES

- **Eight Independent 12-Bit DACs with Output Amplifiers**
- **Low Power 320 mW (typ.)**
- **Serial Digital Data and Address Port (3-Wire Standard)**
- **12-Bit Resolution, 11 Bit Accuracy**
- **Extremely Well Matched DACs**
- **Extremely Low Analog Ground Current (<60µA/Channel)**
- **±10 V Output Swing with ±11.4 V Supplies**
- **Zero Volt Output Preset (Data = 10 .. 00)**
- **Rugged Construction – Latch-Up Free**
- **Parallel Version: MP7613**

APPLICATIONS

- **Data Acquisition Systems**
- **ATE**
- **Process Control**
- **Self-Diagnostic Systems**
- **Logic Analyzers**
- **Digital Storage Scopes**
- **PC Based Controller/DAS**

GENERAL DESCRIPTION

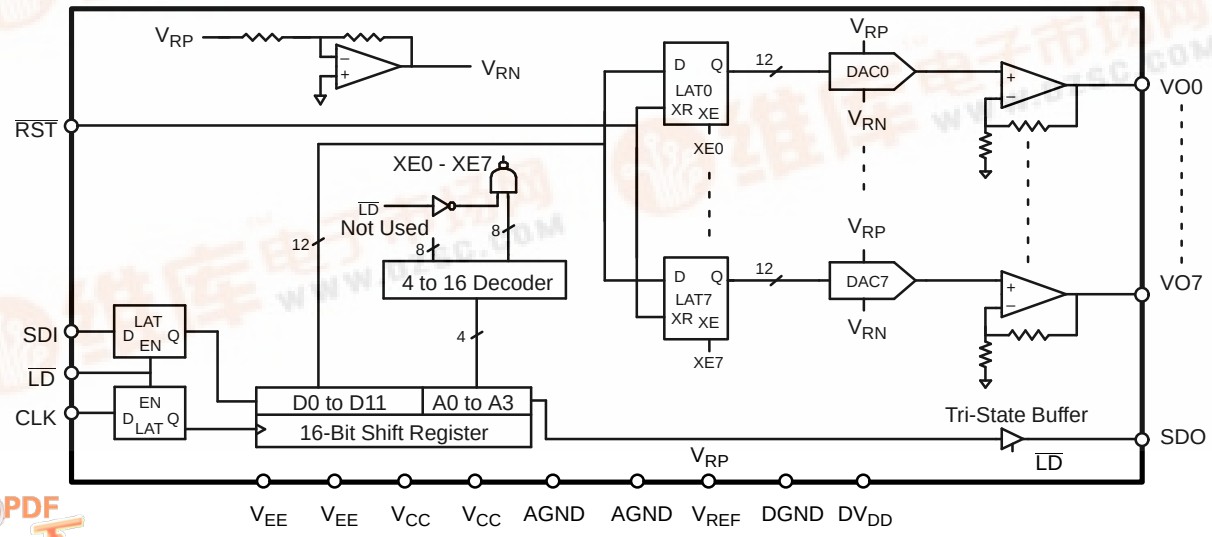
The MP7612 provides eight independent 12-bit resolution Digital-to-Analog Converters with voltage output amplifiers and a 3-wire standard serial digital address and data port.

Typical DAC matching for B grade versions is 0.7 LSB across all codes. Accuracy of ±0.75 LSB for DNL and ±1 LSB for INL is also achieved for B grades. The output amplifier is capable of sinking and sourcing 5mA, and the output voltage settles to 12-bits in less than 30µs (typ.).

The MP7612 is equipped with a serial data (3-wire standard) µ-processor logic interface to reduce pin count, package size, and board space.

Built using an advanced linear BiCMOS, these devices offer rugged solutions that are latch-up free, and take advantage of EXAR's patented thin-film resistor process which exhibits excellent long term stability and reliability.

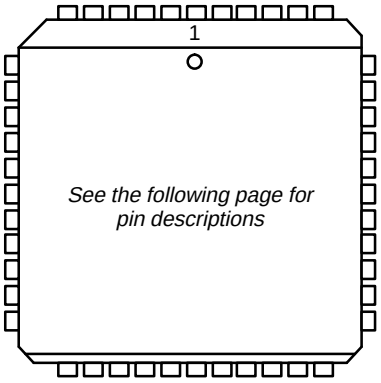
SIMPLIFIED BLOCK DIAGRAM



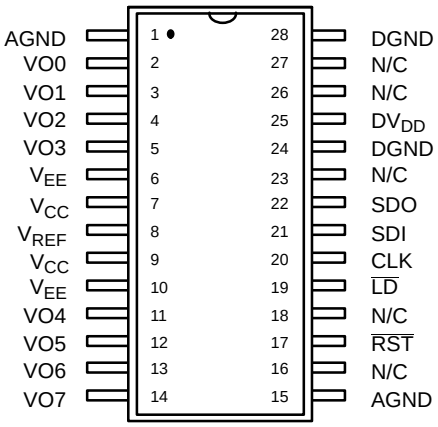
ORDERING INFORMATION

Package Type	Temperature Range	Part No.	Res. (Bits)	INL (LSB)	DNL (LSB)	FSE (LSB)
PLCC	–40 to +85°C	MP7612BP	12	±1	±0.75	±6
PLCC	–40 to +85°C	MP7612AP	12	±2	±1	±8
SOIC	–40 to +85°C	MP7612BS	12	±1	±0.75	±6
SOIC	–40 to +85°C	MP7612AS	12	±2	±1	±8

PIN CONFIGURATIONS



44 Pin PLCC



28 Pin SOIC (Jedec, 0.346")

PIN DESCRIPTION

SOIC Pin #	PLCC Pin #	Symbol	Description
1	2	AGND	Analog Ground
2	3	VO0	DAC 0 Output
3	4	VO1	DAC 1 Output
4	5	VO2	DAC 2 Output
5	6	VO3	DAC 3 Output
6	7	V_{EE}	Analog Negative Power Supply (–12 V)
7	9	V_{CC}	Analog Positive Power Supply (+12 V)
8	12	V_{REF}	Voltage Reference Input (+5 V)
9	13	V_{CC}	Analog Positive Power Supply (+12 V)
10	15	V_{EE}	Analog Negative Power Supply (–12 V)
11	18	VO4	DAC 4 Output
12	19	VO5	DAC 5 Output
13	20	VO6	DAC 6 Output
14	21	VO7	DAC 7 Output
15	24	AGND	Analog Ground
16		N/C	No Connection
17	26	$\overline{RST}$	Reset all DACs to 0 V Output
18		N/C	No Connection
19	29	$\overline{LD}$	Load Signal; Load Data to Selected DAC
20	31	CLK	Serial Data Clock
21	32	SDI	Serial Data Input
22	34	SDO	Shift Register Serial Output
23		N/C	No Connection
24	37	DGND	Digital Ground
25	40	DV_{DD}	Digital Positive Power Supply (+5 V)
26		N/C	No Connection
27	1, 8, 10, 11, 14, 16, 17, 22, 23, 25, 27, 28, 30, 33, 35, 36, 38, 39, 41, 42, 43	N/C	No Connection
28	44	DGND	Digital Ground

ELECTRICAL CHARACTERISTICS

V_{CC} = +12 V, V_{EE} = –12 V, V_{REF} = 5 V, DV_{DD} = 5.0 V, T = 25°C, Output Load = 5kΩ (unless otherwise noted)

Parameter	Symbol	25°C Min	25°C Typ	25°C Max	Tmin to Tmax Min	Tmin to Tmax Max	Units	Test Conditions/Comments
STATIC PERFORMANCE								
Resolution (All Grades)	N	12					Bits	
Integral Non-Linearity (Relative Accuracy)	INL						LSB	End Point Linearity Spec
A				±2		±2		
B				±1		±1		
Differential Non-Linearity	DNL						LSB	
A				±1		±1		
B				±0.75		±0.75		
Positive Full Scale Error	+FSE						LSB	
A			6	±8		±8		
B			4	±6		±6		
Negative Full Scale Error	–FSE						LSB	
A			6	±8		±8		
B			4	±6		±6		
Bipolar Zero Offset	ZOFS						LSB	
A				±4		±4		
B				±3		±3		
INL Matching	ΔINL						LSB	
A				±2		±2		
B				±1.5		±1.5		
All Channels Maximum Error with DAC 0 adjusted to minimum error	ME						LSB	
A				±4		±4		
B				±2		±2		
Bipolar Zero Matching	ΔZOFS						LSB	
A				±4		±4		
B				±3		±3		
Full Scale Error Matching	FSE						LSB	
A				±4		±4		
B				±3		±3		
DYNAMIC PERFORMANCE								
Voltage Settling from $\overline{LD}$ to VDAC Out[1]	t_{sd}		30	50		50	µsec	ZS to FS (20 V Step)
Channel-to-Channel Crosstalk[1, 6]	CT		0.04				LSB	DC
Digital Feedthrough[1, 6]	Q		–70				dB	CLK and Data to V_{OUTi}
Power Supply Rejection Ratio	PSRR			5			ppm/%	ΔV_{EE} & ΔV_{CC} = ±5%, ppm of FS
REFERENCE INPUTS								
Impedance of V_{REF}	REF	350	700	1.05k	350	1.05k	Ω	See Application Hints for driving the reference input
V_{REF} Voltage1, [2]	V_{REF}	3.5		6			V	

ELECTRICAL CHARACTERISTICS (CONT'D)

Parameter	Symbol	25°C Min	25°C Typ	25°C Max	Tmin to Tmax Min	Tmin to Tmax Max	Units	Test Conditions/Comments
DIGITAL INPUTS[3]								
Logic High	V_{IH}	2.4					V	
Logic Low	V_{IL}			0.8			V	
Input Current	I_L			±10			µA	
Input Capacitance[1]	C_L			8			pF	
ANALOG OUTPUTS								
Output Swing		$-V_{EE}$ +1.4	V_{CC} –1.4				V	
Output Drive Current		–5		5			mA	
Output Impedance	R_O		1				Ω	
Output Short Circuit Current	I_{SC}		25				mA	+FS to AGND
			30				mA	+FS to V_{EE}
			40				mA	–FS to AGND
			55				mA	–FS to V_{CC}
DIGITAL OUTPUTS								
Output High Voltage	V_{OH}		4.5				V	
Output Low Voltage	V_{OL}		0.5				V	
POWER SUPPLIES								
V_{CC} Voltage[5]	V_{CC}	V_{REF}+1.5	12	12.75	V_{REF}+1.5	12.75	V	
V_{EE} Voltage[5]	V_{EE}	–12.75	–12	–5	–12.75	–5	V	
DV_{DD} Voltage	DV_{DD}	4.5	5	5.5	4.5	5.5	V	
Positive Supply Current	I_{CC}		8	10		10	mA	Bipolar zero
Negative Supply Current	I_{EE}		15	20		20	mA	Bipolar zero
Digital Supply Current	I_{DD}			2		2	mA	Bipolar zero
Power Dissipation	PD_{ISS}		320	420		450	mW	Bipolar zero
ANALOG GROUND CURRENT								
Per Channel[1]	I_{AGND}		±60				µA	See Application Notes
DIGITAL TIMING SPECIFICATIONS[1,4]								V_{IL} = 0, V_{IH} = 5.0, C_L = 20 pF
Input Clock Pulse Width	t_{CH}, t_{CL}	35					ns	
Data Setup Time	t_{DS}	15					ns	
Data Hold Time	t_{DH}	15					ns	
CLK to SDO Propagation Delay	t_{PD}			40			ns	
DAC Register Load Pulse Width	t_{LD}	35					ns	
Preset Pulse Width	t_{PR}	50					ns	
Clock Edge to Load Time	t_{CKLD1}	140					ns	Note: t_{LD} and t_{CKLD2} cannot both be min. since t_{CKLD1}=t_{CKLD2}+t_{LD}
	t_{CKLD2}	0						
$\overline{LD}$ Falling Edge to SDO Tri-state Enable	t_{HZ1}	50					ns	
$\overline{LD}$ Rising Edge to SDO Tri-state Disable	t_{HZ2}	50					ns	
$\overline{LD}$ Rising Edge to CLK Enable	t_{LDCK}	50					ns	
$\overline{LD}$ Set-up Time with Respect to CLK	t_{LDSU}	30					ns	

ELECTRICAL CHARACTERISTICS (CONT'D)

NOTES:

1 Guaranteed; not tested.
2 Specified values guarantee functionality.
3 Digital inputs should not go below digital GND or exceed DV_{DD} supply voltage.
4 *See Figures 2 and 3.* All digital input signals are specified with $t_R = t_F = 10$ ns 10% to 90% and timed from a 50% voltage level.
5 For power supply values < $\pm 2 * V_{REF}$, the output swing is limited as specified in Analog Outputs.
6 Digital feedthrough and channel-to-channel crosstalk are heavily dependent on the board layout and environment.

Specifications are subject to change without notice

ABSOLUTE MAXIMUM RATINGS (TA = +25°C unless otherwise noted)[1, 2]

V_{CC} to AGND ..... +16.5 V

V_{EE} to AGND ..... –16.5 V

DV_{DD} to DGND ..... +6.5 V

V_{REF} to DGND ..... +7.0 V

AGND to DGND ..... ±1 V
(Functionality guaranteed for ±0.5 V only)

Digital Input & Output Voltage to DGND –0.5 to DV_{DD} +0.5V

Analog Inputs & Outputs ..... Indefinite Shorts to V_{CC}, V_{EE}, DV_{DD}, AGND, DGND (provided that power dissipation of the package spec is not exceeded)

Operating Temperature Range
Extended Industrial ..... –40°C to +85°C

Maximum Junction Temperature ... –65°C to 150°C

Storage Temperature ..... 150°C

Lead Temperature (Soldering, 10 sec) ..... +300°C

Package Power Dissipation Rating @ 75°C
SOIC, PLCC 1150mW
Derates above 75°C ..... 15mW/°C

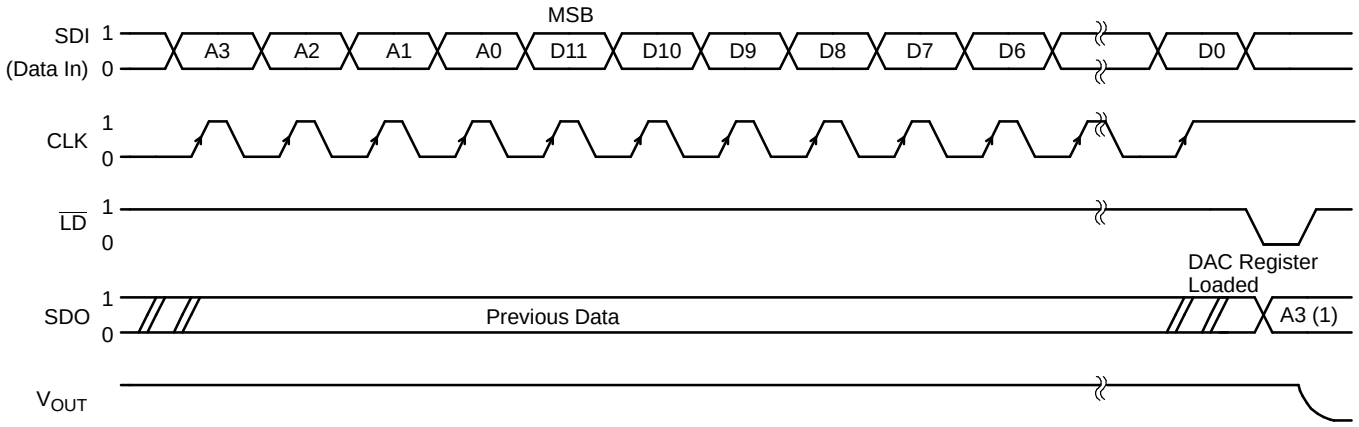
NOTES:

1 Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation at or above this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.
2 Any input pin which can see a value outside the absolute maximum ratings should be protected by Schottky diode clamps (HP5082-2835) from input pin to the supplies. *All inputs have protection diodes* which will protect the device from short transients outside the supplies of less than 100mA for less than 100µs.

APPLICATION NOTES

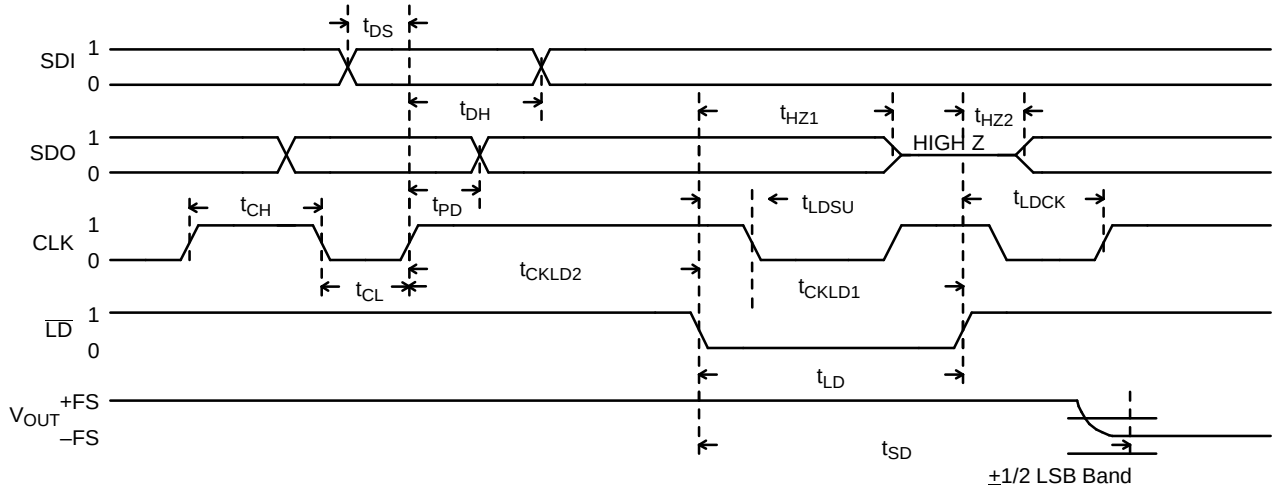
Refer to Section 8 in the 1995 Data Acquisition products Databook for Applications Information

NOTE: When using these DACs to drive remote devices, the accuracy of the output can be improved by utilizing a remote analog ground connection. The difference between the DGND and AGND should be limited to ±300 mV to assure normal operation. If there is any chance that the AGND to DGND can be greater than ±1 V, we recommend two back-to-back diodes be used between DGND and AGND to clamp the voltage and prevent damage to the DAC. Using a buffer between the remote ground location and AGND may help reduce noise induced from long lead or trace lengths.



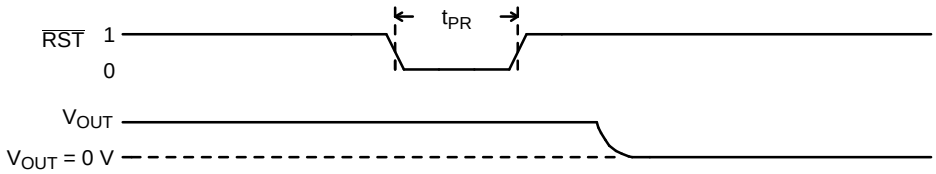
Notes: (1) Because A3 is available immediately after 16th clock edge of DATA Shift-in, only 15 clock cycles are needed to complete the readback.

Figure 1. Serial Data Timing and Loading



Notes: (1) CLK should be high during the falling edge of $\overline{LD}$ to insure proper function of the shift register.

Figure 2. Serial Data Input Timing ($\overline{RST}$ = "1")



Note: Reset settling time is $\leq t_{SD}$ ±1/2 LSB Error Band

Figure 3. Reset Operation

The MP7612 is equipped with a serial data (3-wire standard) µ-processor logic interface to reduce pin count, package size, and board wire (space). If the $\overline{LD}$ signal is high, the CLK signal loads the digital input bits (SDI) into the shift register (4 bits address A3 to A0 plus 12 bits data DB11 to DB0 for the MP7612). The $\overline{LD}$ signal going low loads the data into the selected DAC. The $\overline{LD}$ signal going low also disables the serial data (SDI), output (SDO 3-stated) and the CLK input. This design tremendously reduces digital noise and glitch transients into the DACs due to free running CLK and SDI. Note also that the preset signal ($\overline{RST}$) resets all analog outputs to 0 volt regardless of digital inputs.

Function	A3	A2	A1	A0	$\overline{LD}$	CLK	$\overline{RST}$	SDI	SDO
Shift Data In and Out	X	X	X	X	1	0→1 Repeat	1	Data Input Valid	Data Output Valid
Stop Shifting Data In and Out	X	X	X	X	0	X	1	X	Hi-Z
Load DACs	0	0	0	0	No Operation				
DAC 0	0	0	0	1	1→0	X	1	X	Hi-Z
DAC 1	0	0	1	0	1→0	X	1	X	Hi-Z
DAC 2	0	0	1	1	1→0	X	1	X	Hi-Z
DAC 3	0	1	0	0	1→0	X	1	X	Hi-Z
DAC 4	0	1	0	1	1→0	X	1	X	Hi-Z
DAC 5	0	1	1	0	1→0	X	1	X	Hi-Z
DAC 6	0	1	1	1	1→0	X	1	X	Hi-Z
DAC 7	1	0	0	0	1→0	X	1	X	Hi-Z
⋮	⋮	⋮	⋮	⋮	No Operation	X	⋮	⋮	⋮
⋮	⋮	⋮	⋮	⋮	⋮	X	⋮	⋮	⋮
⋮	⋮	⋮	⋮	⋮	⋮	X	⋮	⋮	⋮
⋮	1	1	1	0	No Operation	X	1	X	Hi-Z
⋮	1	1	1	1	No Operation	X	1	X	Hi-Z
Reset all DACs to 0 V	X	X	X	X	X	X	0	X	X

Table 1. Digital Function Truth Table
Serial In/Serial Out

Note: For timing information see Electrical Characteristics

Hex Code	Binary Code	Output Voltage = 2 • Vr (–1 + $\frac{2 \bullet D}{4096}$) (Vr = +5 V)
0 0 0	000000000000	10 • (–1 + 0) = –10
⋮	⋮	⋮
7 F F	011111111111	10 • (–1 + $\frac{4094}{4096}$) = –4.88 mV
8 0 0	100000000000	10 • (–1 + $\frac{4096}{4096}$) = 0
8 0 1	100000000001	10 • (–1 + $\frac{4098}{4096}$) = 4.88 mV
⋮	⋮	⋮
F F F	111111111111	10 • (–1 + $\frac{8190}{4096}$) = 9.99512

Table 2. MP7612
Ideal DAC Output vs. Input Code

Note: See Electrical Characteristics for real system accuracy

SERIAL INTERFACE DIAGRAMS

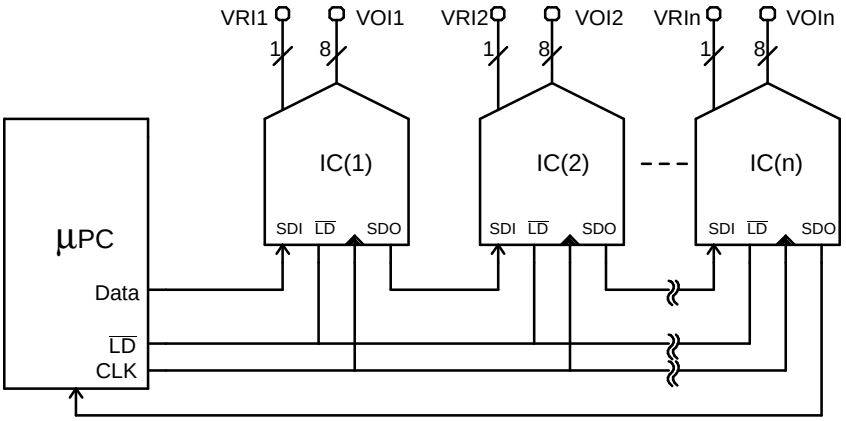


Figure 4. Simplified Diagram

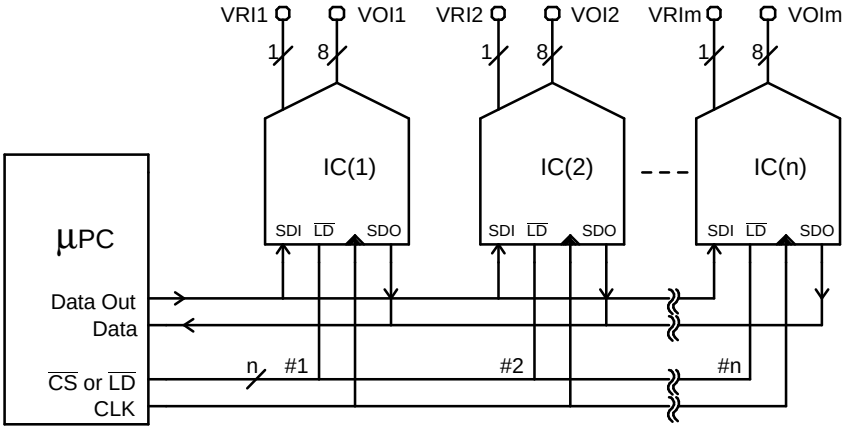


Figure 5. Simplified Diagram

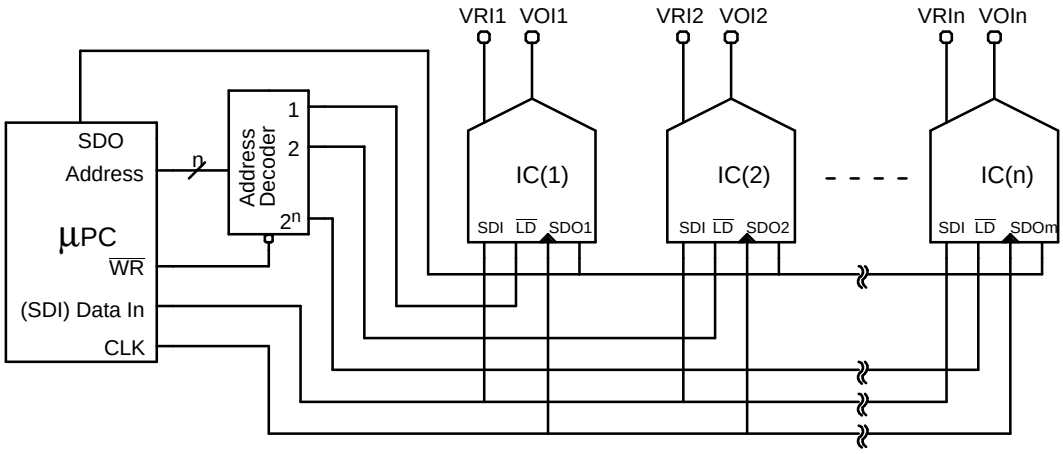
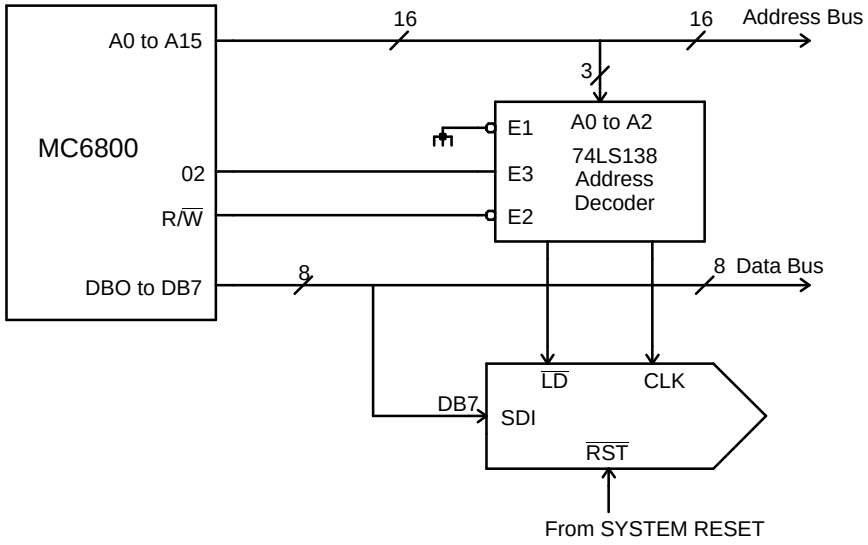
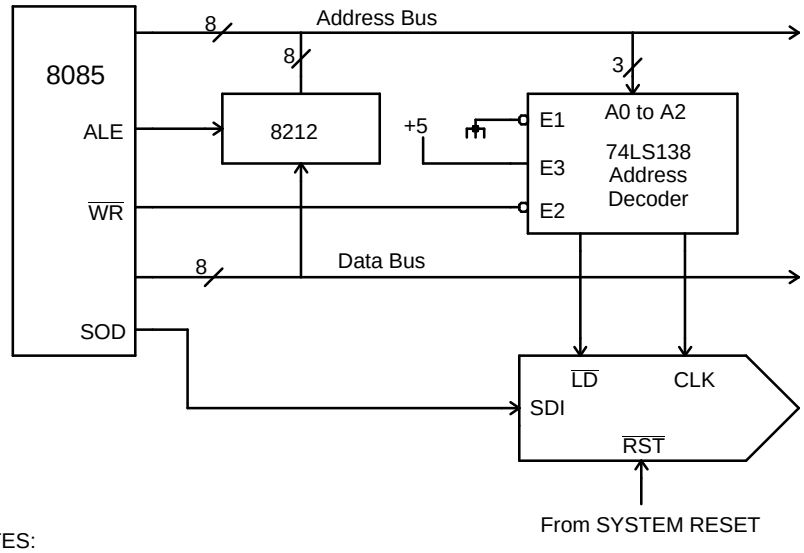


Figure 6. Simplified Diagram



NOTES
1. Execute consecutive memory write instructions while manipulating the data between WRITEs so that each WRITE presents the next bit.
2. The serial data loading is triggered by the CLK pulse which is asserted by a decoded memory WRITE to memory location 2000, R/W, and 02. A WRITE to address 4000 transfers data from input shift register to DAC register.

Figure 7. MC6800 Interface

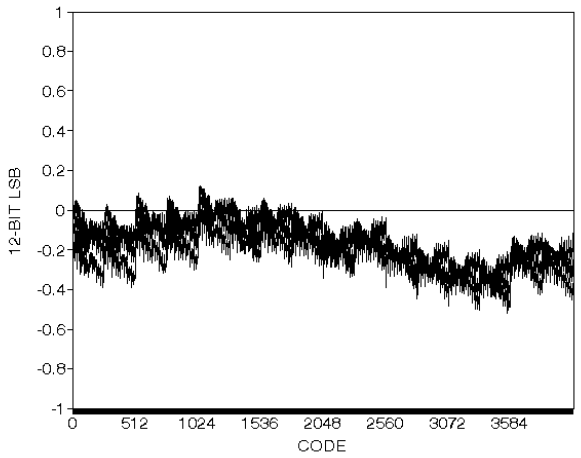


NOTES:
1. Clock generated by $\overline{WR}$ and decoding address 8000.
2. Data is clocked in the DAC shift register by executing memory write instructions. The clock input is generated by decoding address 8000 and WR. Data is then loaded into the DAC register with a memory write instruction to address 4000.
3. Serial data must be present in the right justified format in registers H & L of the microprocessor.

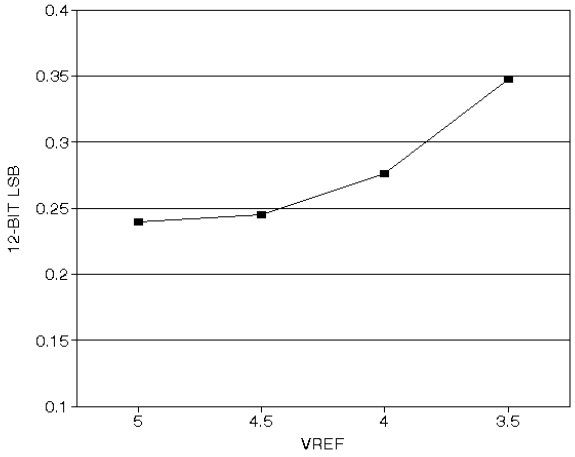
Figure 8. 8085 Interface

Graph 1. Typical Output Settling Characteristic
V_{REF} = 5 V, R_L = 5K, C_L = 500pF

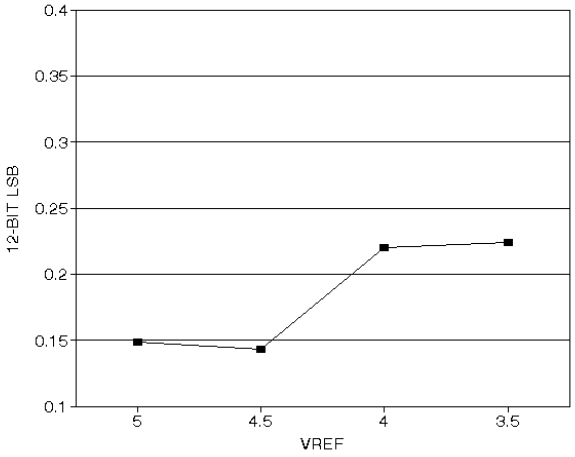
Graph 1 shows the typical output settling characteristic of the MP7610 Family for a RESET →ZS→FS→ZS series of code transitions. The top graph shows the output voltage transients, while the bottom graph shows the difference between the output and the ideal output.



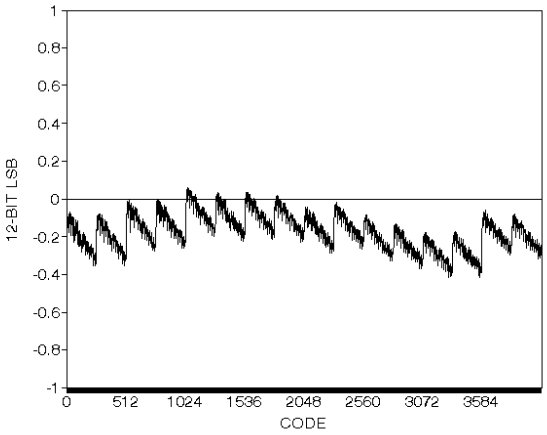
Graph 2. Linearity with
V_{REF} = 5 V, All DACs, All Codes



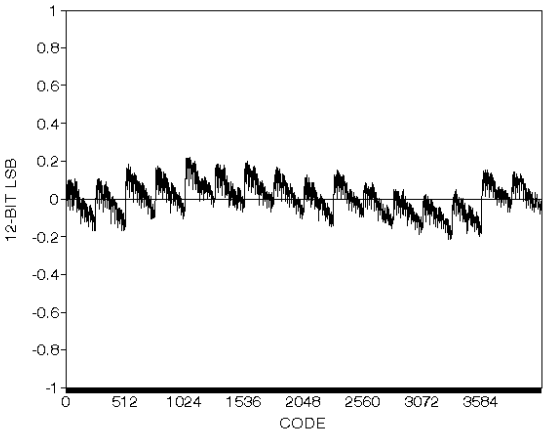
Graph 3. DAC 0 INL vs. V_{REF}



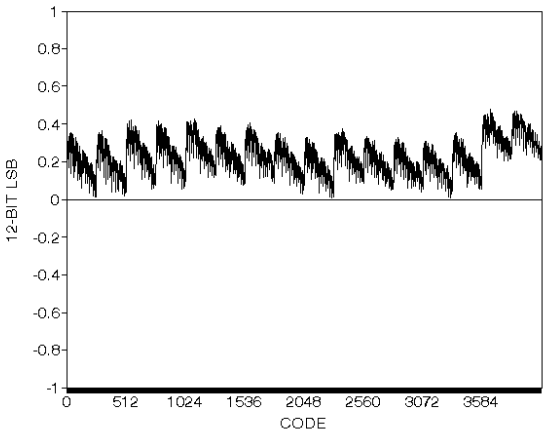
Graph 4. DAC 0 DNL vs. V_{REF}



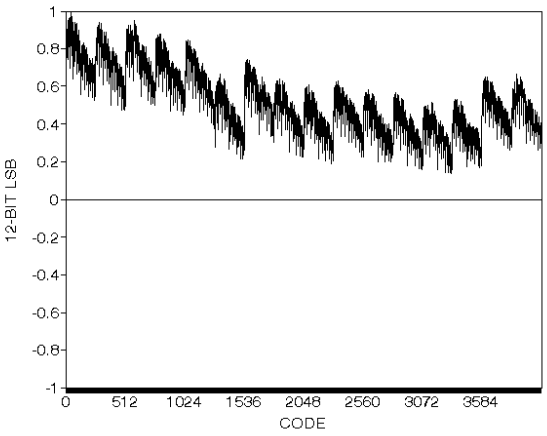
Graph 5. DAC 0 Linearity with V_{REF} = 5 V, V_{OUT} = ±10



Graph 6. DAC 0 Linearity with V_{REF} = 4.5 V, V_{OUT} = ±9



Graph 7. DAC 0 Linearity with V_{REF} = 4 V, V_{OUT} = ±8



Graph 8. DAC 0 Linearity with V_{REF} = 3.5 V, V_{OUT} = ±7

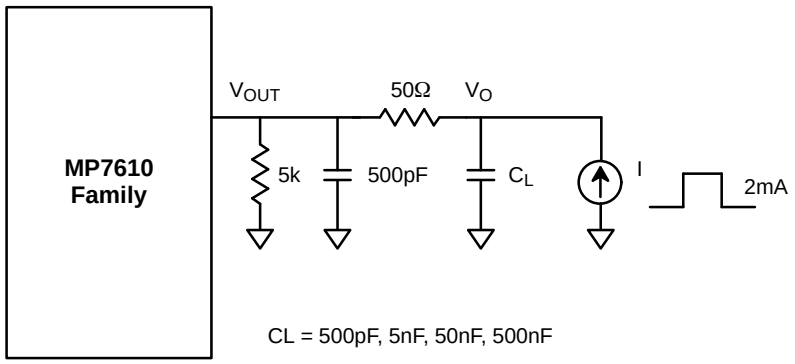
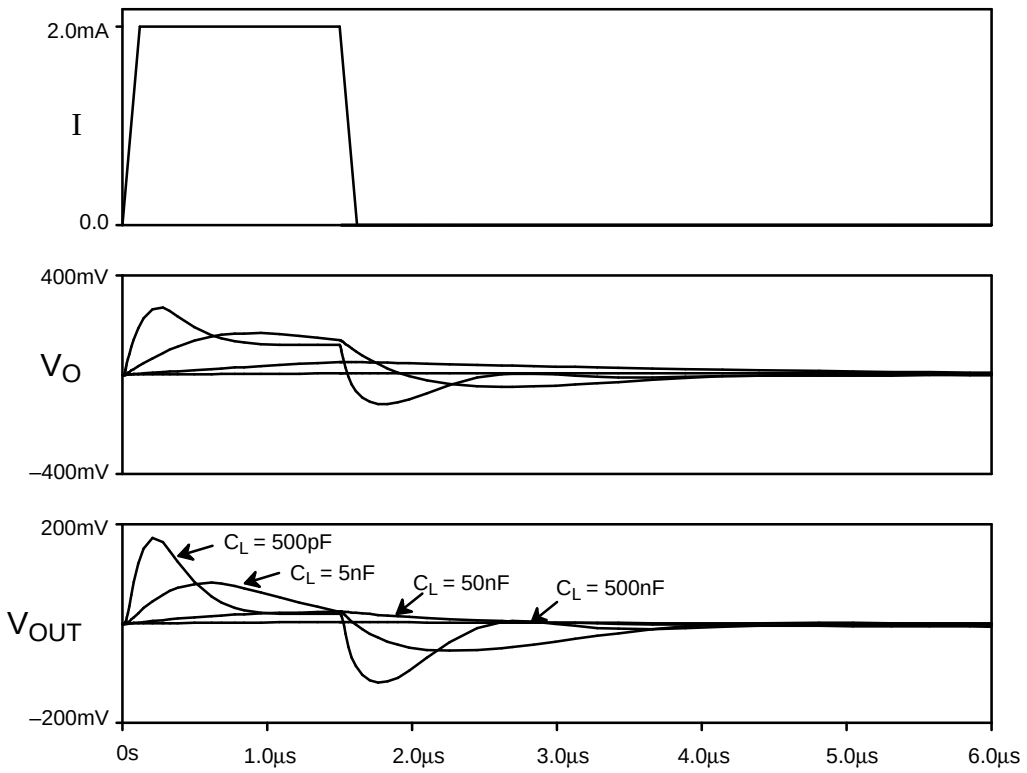
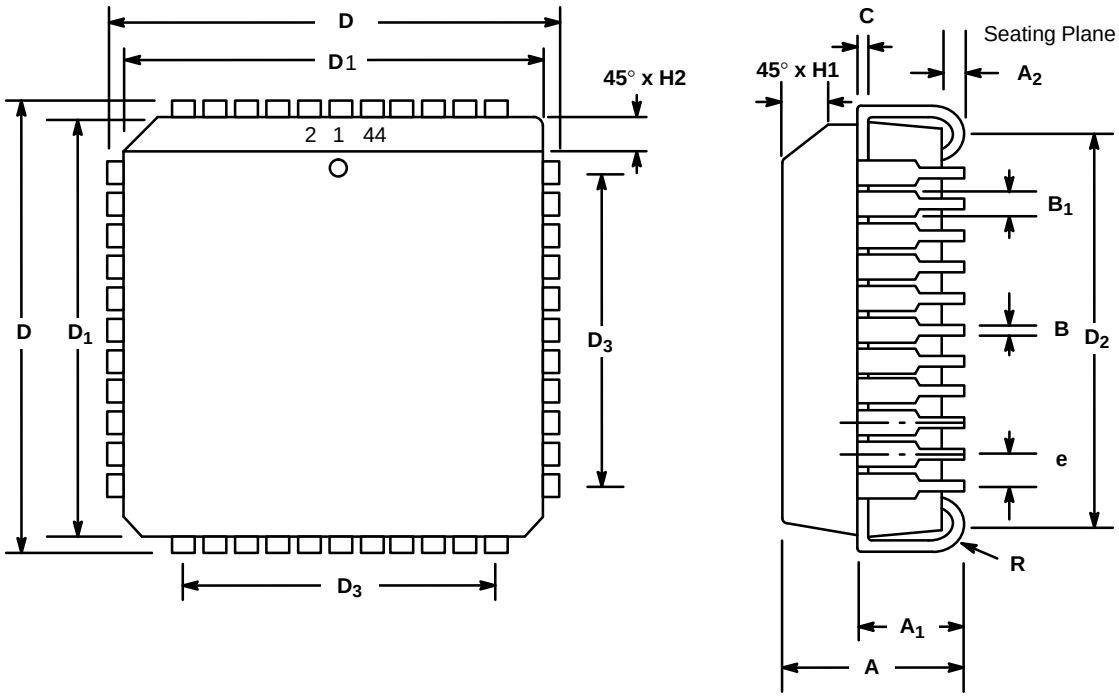


Figure 9. Circuit for Determining Typical Analog Output Pulse Response



Graph 9. Typical Response of the MP7610 Family Analog Output to a Current Pulse with CL=500pF, 5nF, 50nF, 500nF (*See Figure 9. above*)

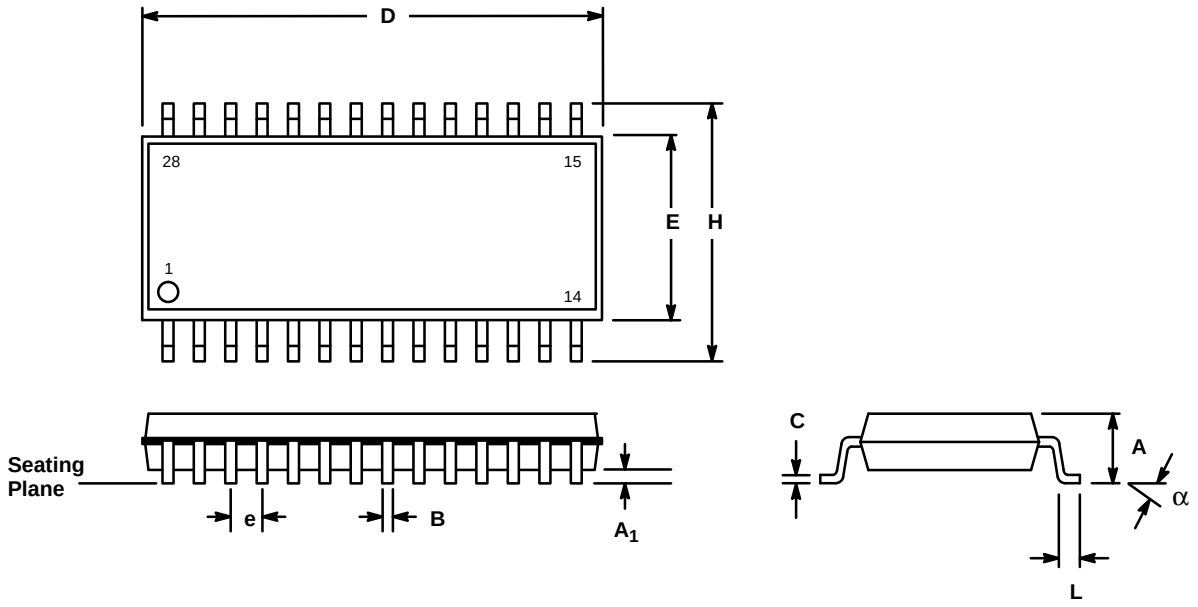
44 LEAD PLASTIC LEADED CHIP CARRIER (PLCC)



SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.165	0.180	4.19	4.57
A_1	0.090	0.120	2.29	3.05
A_2	0.020	—.	0.51	—
B	0.013	0.021	0.33	0.53
B_1	0.026	0.032	0.66	0.81
C	0.008	0.013	0.19	0.32
D	0.685	0.695	17.40	17.65
D_1	0.650	0.656	16.51	16.66
D_2	0.590	0.630	14.99	16.00
D_3	0.500 typ.		12.70 typ.	
e	0.050 BSC		1.27 BSC	
H1	0.042	0.056	1.07	1.42
H2	0.042	0.048	1.07	1.22
R	0.025	0.045	0.64	1.14

Note: The control dimension is the inch column

28 LEAD SMALL OUTLINE
(350 MIL JEDEC SOIC)



SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.093	0.104	2.35	2.65
A_1	0.004	0.012	0.10	0.30
B	0.013	0.020	0.33	0.51
C	0.009	0.013	0.23	0.32
D	0.706	0.718	17.93	18.24
E	0.340	0.350	8.64	8.89
e	0.050 BSC		1.27 BSC	
H	0.460	0.485	11.68	12.32
L	0.016	0.050	0.40	1.27
α	0°	8°	0°	8°

Note: The control dimension is the millimeter column

Notes

Notes

Notes

NOTICE

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