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MP7682

CMOS, 6-Bit High-Speed Analog-to-Digital Converter

March 1998-3

FEATURES

- Sampling Rates from 0.001 to 15 MHz (MSPS)
- Interface to any Analog Input Range between GND and V_{DD}
- Monotonic; No Missing Codes
- Single Power Supply (4 to 6 Volt)
- Low Power CMOS (150 mW typ.)
- ESD Protection: 2000 Volts Minimum
- Latch-Up Free

BENEFITS

- High Conversion Speed at Low Power
- Most Flexible Input Range of any A/D Available
- No Sample/Hold Needed
- Easy Ping-Ponging for 30 MSPS System

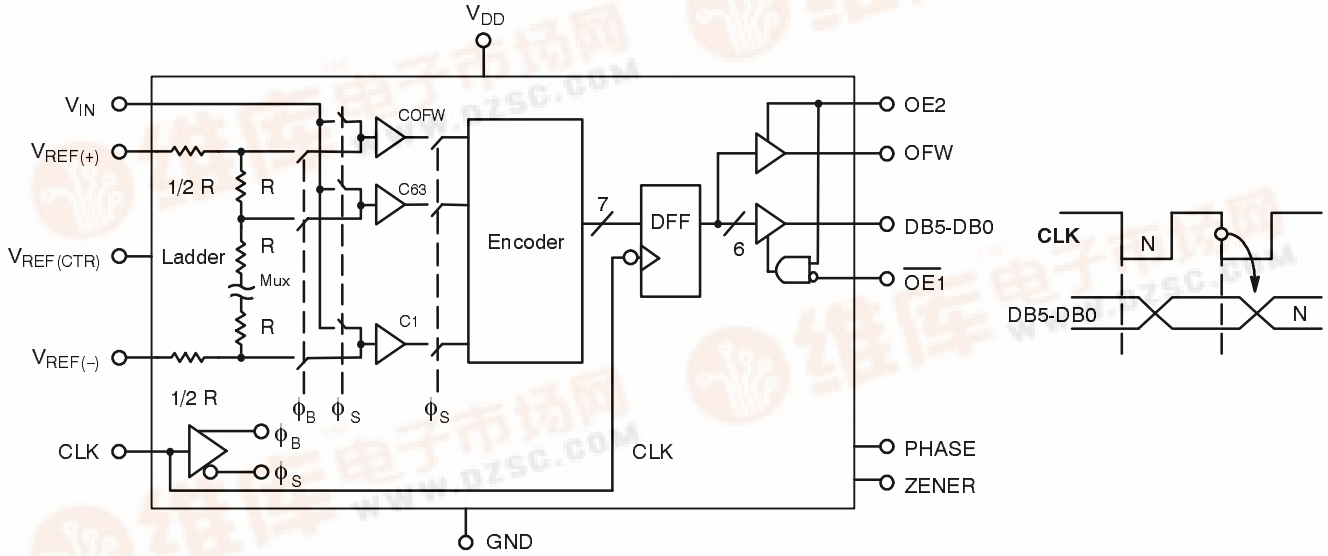
GENERAL DESCRIPTION

The MP7682 is a 6-bit monolithic CMOS single step flash Analog-to-Digital Converter designed for precision 6-bit applications in video, scanning and data acquisition requiring conversion rates to 15 MHz. Differential Linearity error is less than 1/2 LSB at 10 MHz, and power consumption is 150 mW, typical.

The MP7682 has a unique input architecture which eliminates the need for an input track and hold and allows full scale input ranges from about 1 to 5 volts peak-to-peak, referred to ground or offset. The user simply sets $V_{REF(-)}$ and $V_{REF(+)}$ to encompass the desired input range.

MP7682 includes 64 auto-balanced clocked comparators, an encoder, 3-state output buffers, a reference resistor ladder, and associated timing circuitry. An overflow bit (or flag) has been provided to make it possible to achieve 7-bit resolution by connecting two devices in series. In normal operation this flag has no effect on the data bits.

SIMPLIFIED BLOCK AND TIMING DIAGRAM



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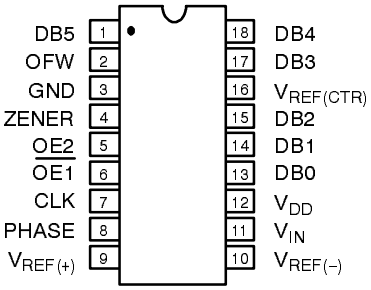
ORDERING INFORMATION

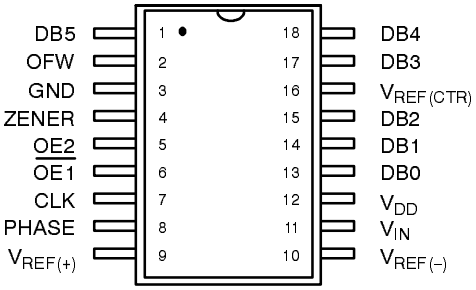
Package Type	Temperature Range	Part No.	DNL (LSB)	INL (LSB)
Plastic Dip	–40 to +85°C	MP7682JN	±2	±2
Plastic Dip	–40 to +85°C	MP7682KN	±1	±1
SOIC	–40 to +85°C	MP7682JS	±2	±2
SOIC	–40 to +85°C	MP7682KS	±1	±1
Ceramic Dip	–55 to +125°C	MP7682SD	±2	±2

PIN CONFIGURATIONS

See Packaging Section for Package Dimensions



18 Pin CDIP, PDIP (0.300")



18 Pin SOIC (0.300", Jedec)

PIN OUT DEFINITIONS

PIN NO.	NAME	DESCRIPTION
1	DB5	Data Output Bit 5 Output (MSB)
2	OFW	Digital Output Overflow
3	GND	Ground
4	ZENER	On Chip Zener Output
5	OE2	Output Enable Control
6	$\overline{OE1}$	Output Enable Control
7	CLK	Clock Input
8	PHASE	Sampling Clock Phase Control
9	$V_{REF(+)}$	Reference Voltage (+) Input

PIN NO.	NAME	DESCRIPTION
10	$V_{REF(-)}$	Reference Voltage (–) Input
11	V_{IN}	Analog Input
12	V_{DD}	Power Supply
13	DB0	Data Output Bit 0 Output (LSB)
14	DB1	Data Output Bit 1 Output
15	DB2	Data Output Bit 2 Output
16	$V_{REF(CTR)}$	R Ladder Mid Point
17	DB3	Data Output Bit 3 Output
18	DB4	Data Output Bit 4 Output

ELECTRICAL CHARACTERISTICS TABLE

Unless Otherwise Specified: V_{DD} = 5 V, F_S = 15 MHz (Duty Cycle: 1/3 Sample & 2/3 Balance), $V_{REF(+)}$ = 4.1, $V_{REF(-)}$ = GND, T_A = 25°C

Parameter	Symbol	25°C Min	25°C Typ	25°C Max	Tmin to Tmax Min	Tmin to Tmax Max	Units	Test Conditions/Comments
KEY FEATURES								
Resolution		6			6		Bits	
Sampling Rate	F_S	0.001		15	0.001	15	MHz	
ACCURACY (J, S Grades)[1]								
Differential Non-Linearity	DNL			±1		±2	LSB	
Integral Non-Linearity (Relative Accuracy)	INL			±1		±2	LSB	Best Fit Line (Max INL – Min INL) / 2
Zero Scale Error	EZS		±1.7				LSB	
Full Scale Error	EFS		±1.7				LSB	
ACCURACY (K, T Grades)[1]								
Differential Non-Linearity	DNL			±1/2		±1	LSB	
Integral Non-Linearity	INL			±1/2		±1	LSB	Best Fit Line
Zero Scale Error	EZS		±1.7				LSB	
Full Scale Error	EFS		±1.7				LSB	
REFERENCE VOLTAGES								
Positive Ref. Voltage	$V_{REF(+)}$			5			V	
Negative Ref. Voltage	$V_{REF(-)}$	GND			GND		V	
Differential Ref. Voltage[3]	V_{REF}	1.0		V_{DD}-GND		V_{DD}-GND	V	
Ladder Resistance	R_L	175		500	150	600	Ω	
Ladder Temp. Coefficient[2]	R_{TCO}					3000	ppm/°C	
ANALOG INPUT[2]								
Input Voltage Range	V_{IN}	$V_{REF(-)}$		$V_{REF(+)}$	$V_{REF(-)}$	$V_{REF(+)}$	V p-p	
Input Impedance	Z_{IN}		3				MΩ	
Input Capacitance Sample[5]	C_{INA}		30				pF	
Aperture Delay	t_{AP}		20				ns	
Aperture Uncertainty (Jitter)	t_{AJ}		220				ps	
DIGITAL INPUTS								
Logical "1" Voltage	V_{IH}	3.5			3.5		V	
Logical "0" Voltage	V_{IL}			0.4		0.4	V	
Leakage Currents								V_{IN}=GND to V_{DD}
CLK	I_{IN}			±1		±30	μA	
OE2				±1		±30	μA	
$\overline{OE1}$				±1		±30	μA	
Phase				±1		±30	μA	
Input Capacitance[2]	C_{IND}		5				pF	
Clock Timing (*See NO TAG*)								
Clock Period	t_S	66					ns	
"High" Time	t_H	33					ns	
"Low" Time	t_L	33					ns	
Duty Cycle			50				%	

ELECTRICAL CHARACTERISTICS TABLE CONT'D

Parameter	Symbol	25°C Min	25°C Typ	25°C Max	Tmin to Tmax Min	Tmin to Tmax Max	Units	Test Conditions/Comments
DIGITAL OUTPUTS								
Logical "1" Voltage	V_{OH}	4.3			4.3		V	I_{LOAD} = –1.0 mA
Logical "0" Voltage	V_{OL}			0.6		0.6	V	I_{LOAD} = 2.0 mA
3-state Leakage	I_{OZ}	±1			±20		µA	V_{OUT} = GND to V_{DD}
Data Valid Delay[2]	t_{DL}		66				ns	
Data Enable Delay[2]	t_{DEN}		20				ns	
Data 3-state Delay[2]	t_{DHZ}		26				ns	
Output Capacitance[2]	C_O		5				pF	
POWER SUPPLIES								
Operating Voltage	V_{DD}	4		6	4	6	V	
Current	I_{DD}		20	30		50	mA	

Notes:

1 *Tester measures code transitions by dithering the voltage of the analog input (V_{IN}). The difference between the measured and the ideal code width (V_{REF}/64) is the DNL error (Figure 3.). The INL error is the maximum distance (in LSBs) from the best fit line to any transition voltage (Figure 4.). Accuracy is a function of the sampling rate (F_S).*

2 *Guaranteed. Not tested.*

3 *Specified values guarantee functionality. Refer to other parameters for accuracy.*

4 *3 dB bandwidth is a measure of performance of the A/D input stage (S/H + amplifier). Refer to other parameters for accuracy within the specified bandwidth.*

5 *See V_{IN} input equivalent circuit (Figure 5.). Switched capacitor analog input requires driver with low output resistance.*

Specifications are subject to change without notice

ABSOLUTE MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)[1, 2]

V_{DD} to GND ..... +7 V
$V_{REF(+)}$ & $V_{REF(-)}$ ..... GND –0.5 to V_{DD} +0.5 V
V_{IN} ..... GND –0.5 to V_{DD} +0.5 V
Digital Inputs ..... GND –0.5 to V_{DD} +0.5 V
Digital Outputs ..... GND –0.5 to V_{DD} +0.5 V

Storage Temperature ..... –65°C to +150°C
Lead Temperature (Soldering 10 seconds) ..... +300°C
Package Power Dissipation Rating to 75°C
CDIP, PDIP, SOIC 850mW
Derates above 75°C ..... 11mW/°C

Notes:

1 *Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation at or above this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.*

2 *Any input pin which can see a value outside the absolute maximum ratings should be protected by Schottky diode clamps (HP5082-2835) from input pin to the supplies. All inputs have protection diodes which will protect the device from short transients outside the supplies of less than 100mA for less than 100µs.*

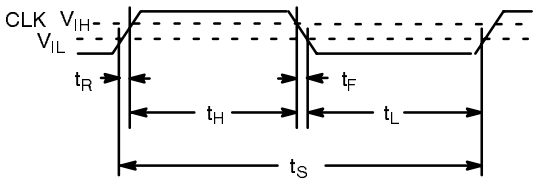


Figure 1. Clock Timing Specification (t_R = t_F = 10 ns typical)

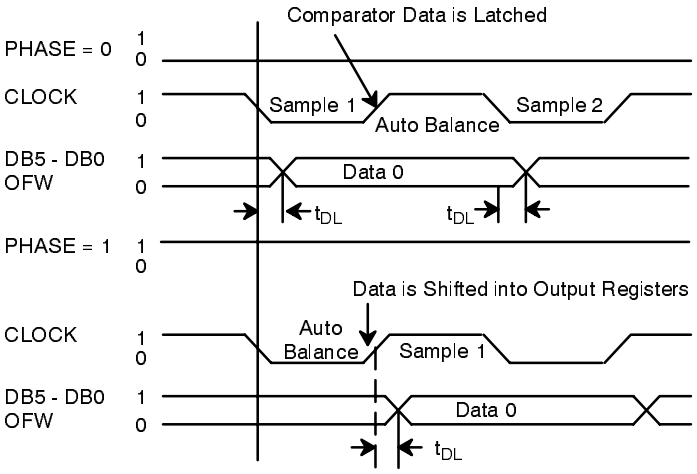


Figure 2. Data Line Enable Delay

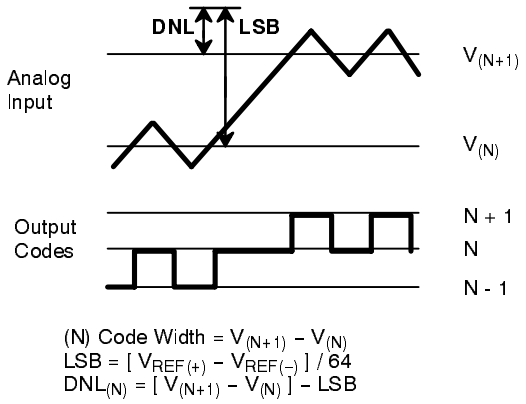


Figure 3. DNL Measurement

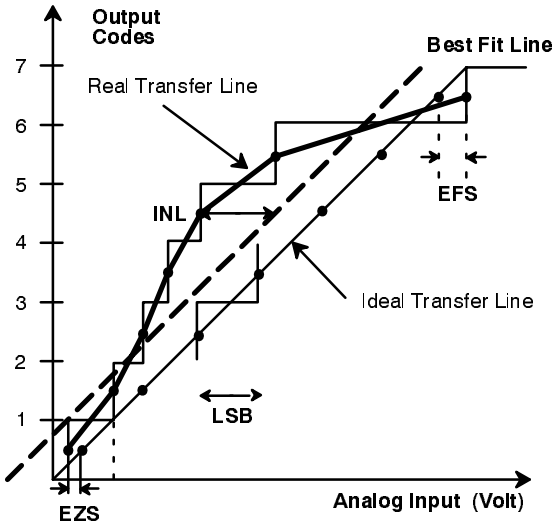


Figure 4. INL Error Calculation

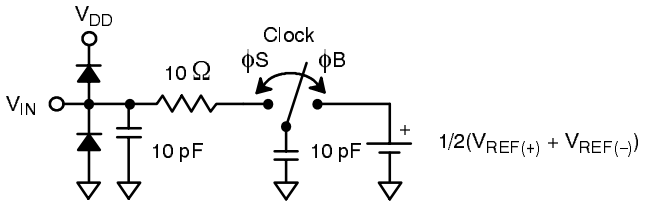


Figure 5. Analog Input Equivalent Circuit

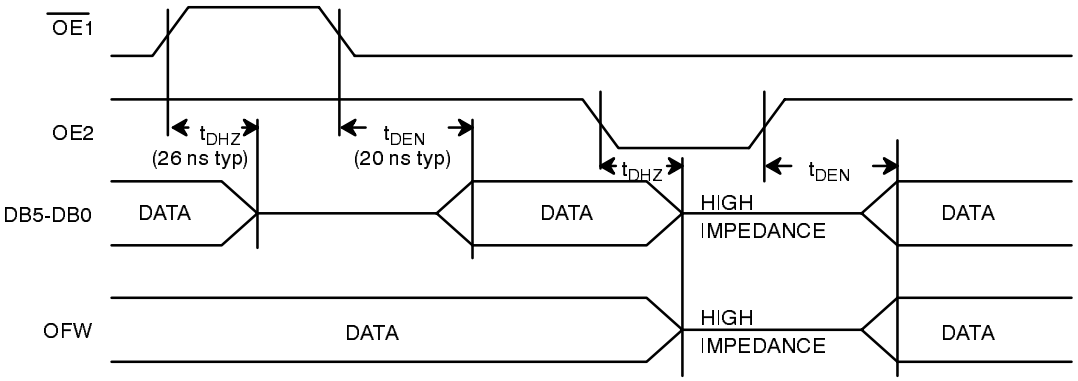


Figure 6. Output Enable and Disable Timing Diagram

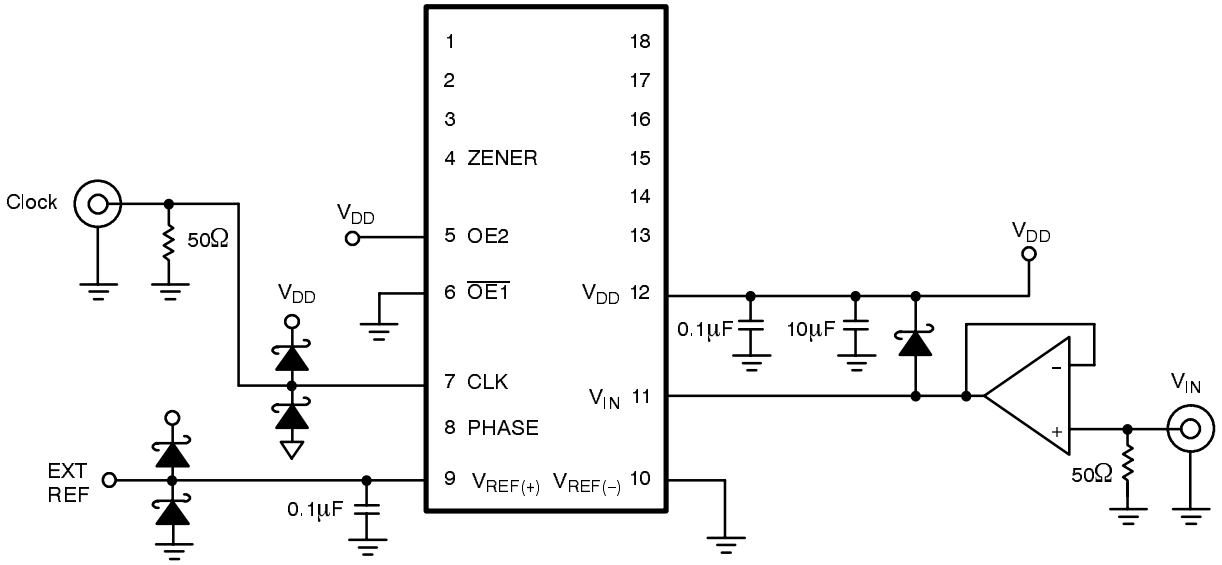
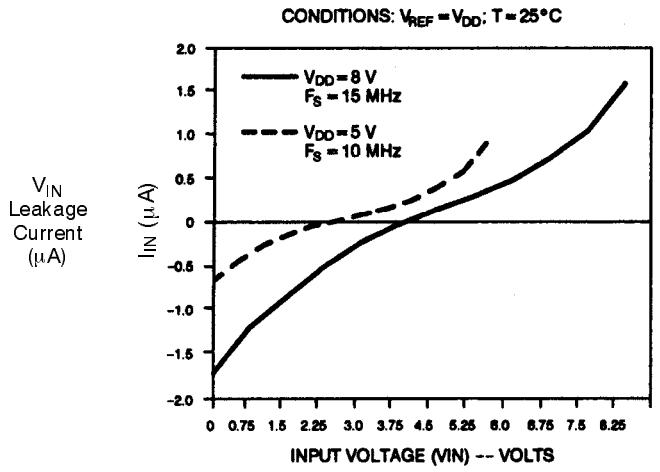


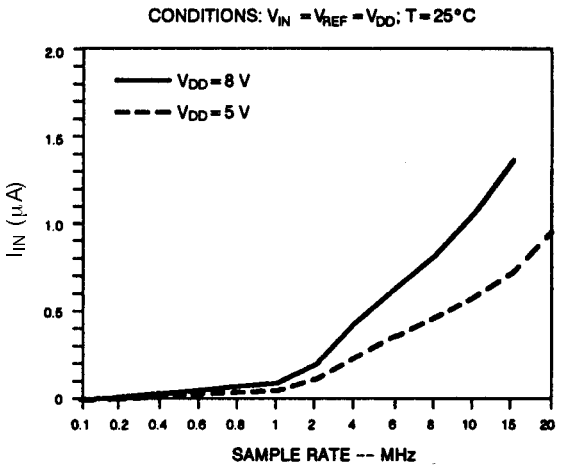
Figure 7. Typical Connections

$\overline{OE1}$	OE2	DB0 - DB5	OFW
0	1	Valid	Valid
1	1	3-State	Valid
X	0	3-State	3-State

Table 1. Truth Table



Graph 1. Analog Input Current vs. Input Voltage



Graph 2. Analog Input Current vs. Sample Rate