MP8780

CMOS
8-Bit Video
Analog-to-Digital Converter

March 1998-3

FEATURES

- 15 MHz Input Bandwidth (–0.3 dB)
- SNR > 44 dB @ Fin 2.4 MHz
- 1.2 to 5.0 Volts (Peak to Peak) Input Range
- 1/2 LSB Dynamic DNL at 14.4 MHz
- 3/4 LSB Dynamic DNL at 17.7 MHz
- Monotonic. No Missing Codes
- Latch Up Free CMOS Technology
- High ESD Protection - 2000 Volts Minimum

BENEFITS

- Optimized Combination of Performance, Power, Packaging and Cost for Video Digitizing Applications
- Excellent Video Digitizing Performance
- Smaller Board Space
- Lower System Power

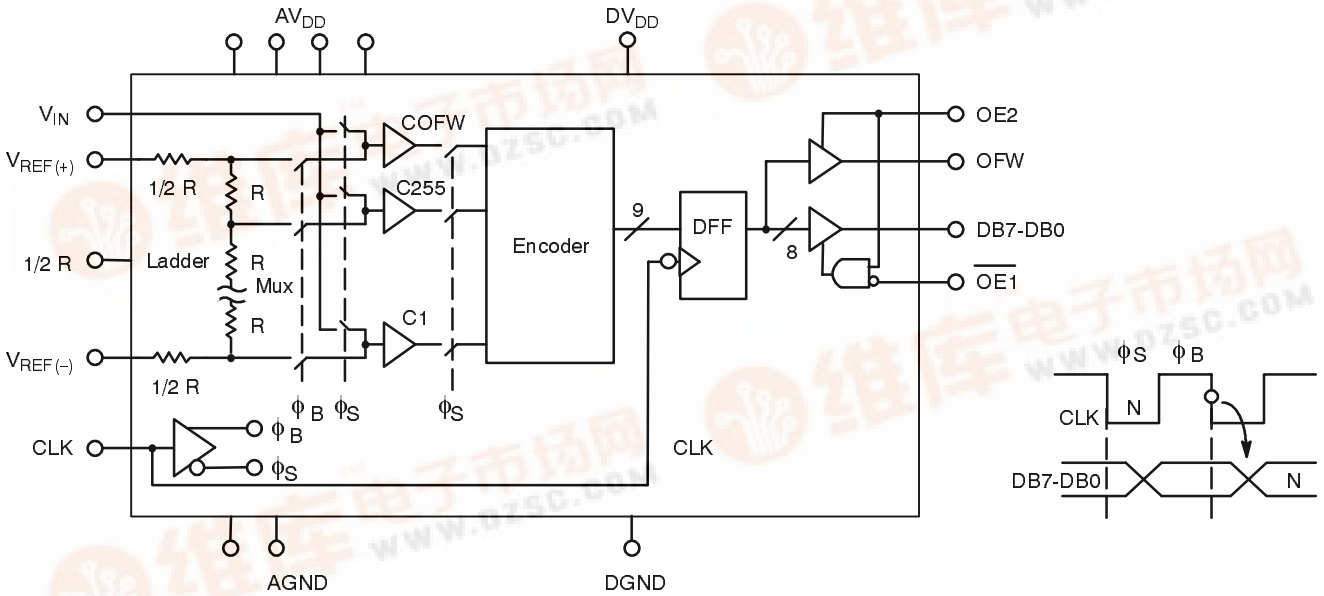
GENERAL DESCRIPTION

The MP8780 is a CMOS 8-bit high speed Analog-to-Digital Converter designed and specified for applications in imaging and video digitizing. With Signal to Noise Ratio greater than 44 dB in the Video Input Bandwidth and encode rates up to 20 MHz, the MP8780 easily meets the requirements needed to digitize standard American and European video signals.

A fast digital interface simplifies connection to most modern DSP and CPU chips.

Careful design and layout have reduced static sensitivity, while our proprietary latch-up free process virtually eliminates the need for many of the diode protection schemes used in the past.

SIMPLIFIED BLOCK AND TIMING DIAGRAM



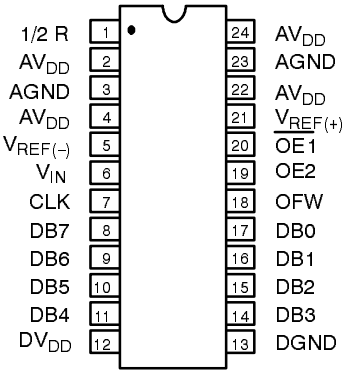
EXAR Corporation, 48720 Kato Road, Fremont, CA 94538 ◆ (510) 668-7000 ◆ (510) 668-7017

ORDERING INFORMATION

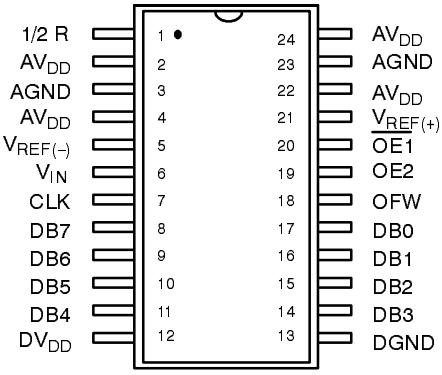
Package Type	Temperature Range	Part No.	DNL (LSB)	INL (LSB)
Plastic Dip	–40 to +85°C	MP8780JN	±1	1 1/2
SOIC	–40 to +85°C	MP8780JS	±1	1 1/2

PIN CONFIGURATIONS

See Packaging Section for Package Dimensions



24 Pin PDIP (0.300")



24 Pin SOIC (Jedec, 0.300")

PIN OUT DEFINITIONS

PIN NO.	NAME	DESCRIPTION
1	1/2R	50% Point of Reference on Resistance Ladder
2	AV_{DD}	Analog Power Supply Voltage
3	AGND	Analog Ground
4	AV_{DD}	Analog Power Supply Voltage
5	$V_{REF(-)}$	Lower Reference Voltage Input
6	V_{IN}	Analog Input Voltage
7	CLK	Sampling Clock Input
8	DB7	Data Output Bit 7 (MSB)
9	DB6	Data Output Bit 6
10	DB5	Data Output Bit 5
11	DB4	Data Output Bit 4
12	DV_{DD}	Digital Power Supply Voltage

PIN NO.	NAME	DESCRIPTION
13	DGND	Digital Ground
14	DB3	Data Output Bit 3
15	DB2	Data Output Bit 2
16	DB1	Data Output Bit 1
17	DB0	Data Output Bit 0 (LSB)
18	OFW	Overflow flag
19	OE2	Output Enable Control Pin
20	$\overline{OE1}$	Output Enable Control Pin
21	$V_{REF(+)}$	Upper Reference Voltage Input
22	AV_{DD}	Analog Power Supply Voltage
23	AGND	Analog Ground
24	AV_{DD}	Analog Power Supply Voltage

ELECTRICAL CHARACTERISTICS

Unless Otherwise Specified: AV_{DD} = DV_{DD} = 5 V, F_S = 14.4MHz (Duty Cycle: 1/3 Sample & 2/3 Balance) $V_{REF(+)}$ = 2.5 V, $V_{REF(-)}$ = GND, Temp = 25°C

		MP8780J				
RESOLUTION		8			Bits	
Maximum Sampling Rate	FS	14.4			MHz	
ACCURACY[1]						
Differential Non-Linearity	DNL		1/2	1	LSB	
Integral Non-Linearity	INL		1	1 1/2	LSB	
Zero Scale Error	EZS		-27		mV	
Full Scale Error	EFS		12		mV	
DNL[6]	DNL		1/4		LSB	F_S = 10MHz
INL[6]	INL		3/4		LSB	F_S = 10MHz
DYNAMIC ACCURACY[6]						
(Histogram Test)						F_S (MHz) / F_{IN} (MHz) / V_{REF} (V)
Differential Non-Linearity			1/2		LSB	14.4 / 2.0 / 4
Differential Non-Linearity			1/2		LSB	14.4 / 2.0 / 2.5
Differential Non-Linearity			3/4		LSB	17.7 / 2.0 / 4
Differential Non-Linearity			3/4		LSB	17.7 / 2.0 / 2.5
REFERENCE VOLTAGES						
Positive Ref. Voltage	$V_{REF(+)}$			V_{DD}	V	
Negative Ref. Voltage	$V_{REF(-)}$	GND			V	
Differential Ref. Voltage	V_{REF}	2.0		V_{DD}-GND	V	
Ladder Resistance	R_L	180	225	285	Ω	
Ladder Temp. Coefficient[6]	R_{TCO}			2000	ppm/°C	
ANALOG INPUT[2, 6]						
Input Voltage Range	V_{IN}	$V_{REF(-)}$		$V_{REF(+)}$	V	
Input Impedance (*See Figure 3.*)	C_{INA}		50		pF	
Aperture						
Aperture Delay	t_{AP}		15		ns	
Aperture Uncertainty	t_{AJ}		45		ps	
Clock Kickback Pulse			10		pA•s	V_{REF}=2.5 V
			20		pA•s	V_{REF}=4.0 V
Input Bandwidth (-0.3 dB)	BW		15		MHz	
DIGITAL INPUTS[3] **(Tmin to Tmax)**						
Logical "1" Voltage	V_{IH}	2.0			V	
Logical "0" Voltage	V_{IL}			0.8	V	
Current (CLK)		-100		100	µA	V_{IN}=0 to V_{DD}
Current ($\overline{-0E1}$: Res to GND)		-5		50	µA	V_{IN}=0 to V_{DD}
Current (0E2: Res to V_{DD})		-50		5	µA	V_{IN}=0 to V_{DD}
Input Capacitance[6]	C_{IND}		5		pF	
Clock Timing (***See Figure 1.***)[6]						
Rise & Fall Time[4]	t_R, t_F			8	ns	
"High" Time (Autozero/Autobalance)	t_B	20			ns	
"Low" Time (Sampling)	t_S	20			ns	

ELECTRICAL CHARACTERISTICS TABLE, (CONT'D)

Description	Symbol	MP8780J Min	Typ	Max	Units	Conditions
DIGITAL OUTPUTS						C_{OUT}= 15 pF
Logical "1" Voltage	V_{OH}	V_{DD}–0.5			V	
Logical "1" Source Current	I_{OH}	2			mA	
Logical "0" Voltage	V_{OL}			0.4	V	
Logical "0" Sink Current	I_{OL}	4			mA	
3-state Leakage	I_{OZ}	–10		10	uA	V_{OUT}=0 to V_{DD}
Min Data Hold Time (*See Figure 1.*)[6]	t_{HLD}	12	15		ns	
Max Data Valid Delay[6]	t_{DL}		30	33	ns	
Data Enable Delay (*See Figure 2.*)[6]	t_{DEN}			20	ns	
Data Tristate Delay[6]	t_{DHZ}			20	ns	
POWER SUPPLIES						
Operating Voltage[5]	V_{DD}	4		6	V	
I_{DD}	I_{DD}		30	50	mA	
AC PARAMETERS[6]						
Differential Gain Error			2		%	F_S = 3 x NTSC
Differential Phase Error			1		Degree	
Signal Noise Ratio (RMS/RMS)	SNR					F_S (MHz) / F_{IN} (MHz)
			46		dB	14.4 / 2.4
			44		dB	17.7 / 2.4

Notes:

1 *Linearity (DNL, INL) is a function of clock frequency. INL is specified as the best straight line fit. See characterization chart.*

2 *See V_{IN} Input Equivalent Circuit (Figure 3.). Switched capacitor analog input requires input buffer with lowest output resistance possible.*

3 *All inputs have current leakage to V_{DD} and GND. OE2 has pull-up transistor. $\overline{OE1}$ has pull-down transistors. These DC currents will not exceed the specified values for any input voltage between 0 and V_{DD}.*

4 *CLK Input spec to meet MP8780 aperture specifications. Actual rise/fall timing can be less stringent with no loss of accuracy.*

5 *Specified values guarantee functional device. Refer to other parameters for accuracy.*

6 *Guaranteed. Not production tested.*

Specifications are subject to change without notice

ABSOLUTE MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)[1, 2]

V_{DD} to GND ..... +7 V

$V_{REF(+)}$ & $V_{REF(-)}$ ..... GND –0.5 to V_{DD} +0.5 V

V_{IN} ..... GND –0.5 to V_{DD} +0.5 V

All Inputs ..... GND –0.5 to V_{DD} +0.5 V

All Outputs ..... GND –0.5 to V_{DD} +0.5 V

Storage Temperature ..... –65 to +150°C

Lead Temperature (Soldering 10 seconds) ..... +300°C

Package Power Dissipation Rating to 75°C

PDIP, SOIC 1000mW

Derates above 75°C ..... 13mW/°C

Notes:

1 *Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation at or above this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.*

2 *Any input pin which can see a value outside the absolute maximum ratings should be protected by Schottky diode clamps (HP5082-2835) from input pin to the supplies. All inputs have protection diodes which will protect the device from short transients outside the supplies of less than 100mA for less than 100µs.*

TIMING DIAGRAMS

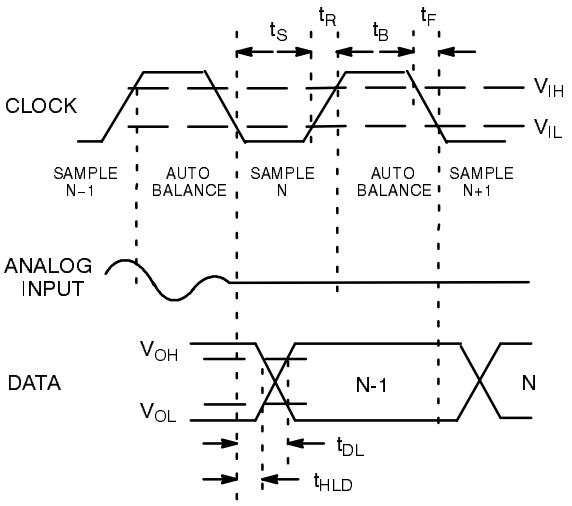


Figure 1. MP8780 Timing Diagram

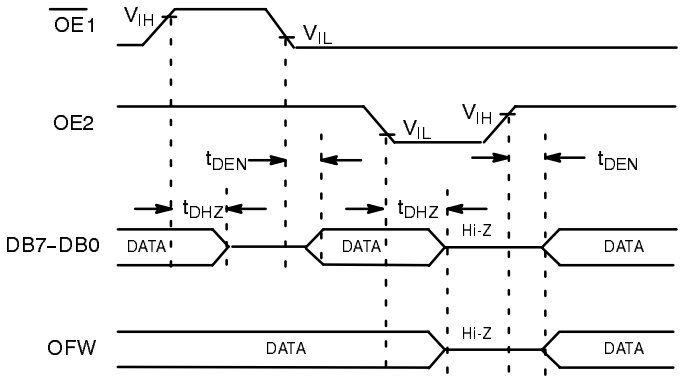


Figure 2. Output Enable/Disable Timing Diagram

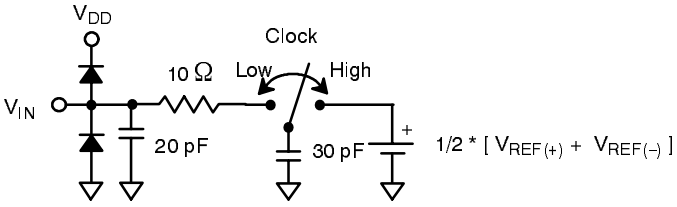


Figure 3. Analog Input Equivalent Circuit

THEORY OF OPERATION

The MP8780 converts analog voltages into 256 digital codes by encoding the outputs of 255 comparators. A 256th comparator is used to generate the overflow bit. The conversion is synchronous with the sample clock. A complete conversion cycle is accomplished in 1.5 cycles. Data is transferred from the comparator latches to the output register each cycle at the same time the input is sampled.

The clock signal generates the two internal phases, ϕ_B (CLK high = balance) and ϕ_S (CLK low = sample). Phase B connects the comparators to the reference tap points. Phase S connects the comparators to the analog input voltage.

The reference resistance ladder is a series of 257 resistors. The first and the last resistor of the ladder are half the value of the others so that the following relations apply:

$R_{REF} = 256 * R \quad V_{REF} = V_{REF(+)} - V_{REF(-)} = 256 * LSB$

The ideal transfer function for MP8780 is shown in *Figure 4.*

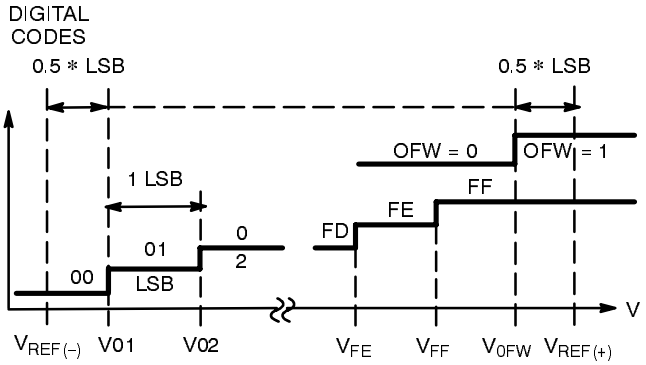


Figure 4. Ideal A/D Transfer Function

The overflow transition (V_{0FW}) takes place at:

$V_{IN} = V_{0FW} = V_{REF(-)} = 0.5$ LSB

Thus the first and the last transitions for the data bits take place at:

$V_{IN} = V01 = V_{REF(-)} + 0.5 * LSB$

$V_{IN} = V_{FF} = V_{REF(+)} - 1.5 * LSB$

$LSB = V_{REF}/256 = (V_{FF} - V01) / 254$

Note that the overflow transition is a flag and has no impact on the data bits.

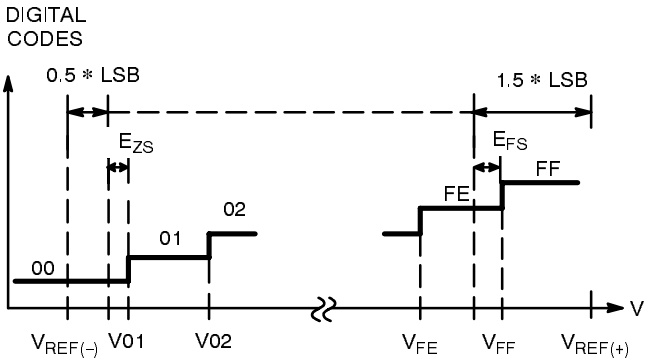


Figure 5. Real A/D Transfer Curve

The formulas define the various error relationships for Differential Non-linearity (DNL), Integral Non-Linearity (INL) and zero and full scale errors (E_{ZS}, E_{FS}).

DNL (01) = V02 – V01 – LSB

: : :

DNL (FE) = $V_{FF} - V_{FE}$ – LSB

E_{FS} (full scale error) = $V_{FF} - [V_{REF(+)} - 1.5 * LSB]$

E_{ZS} (zero scale error) = $V_{01} - [V_{REF(-)} + 0.5 * LSB]$

INL (i) = Σ DNL (i)

Figure 5. shows the effect of the zero scale and full scale error terms.

Systems that adjust the V_{REF} voltages only increase the DNL accuracy at the two extreme points. In the MP8780, such adjustments have little impact at frequencies lower than 10 MHz. Refer to the characterization data for frequency dependence.

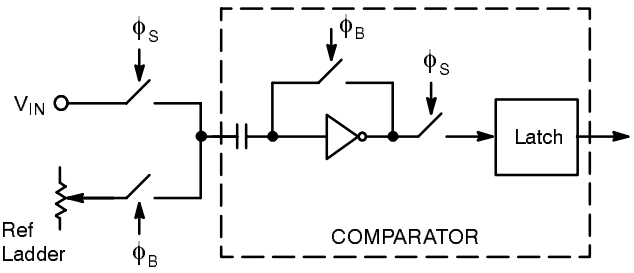


Figure 6. MP8780 Comparator

$\overline{OE1}$	OE2	OFW	DB0-DB7
X	0	High Z	High Z
1	1	Valid	High Z
0	1	Valid	Valid

Table 1. Output Enable Logic

The MP8780 uses the balance phase (ϕ_B) to charge one plate of the capacitors to the reference ladder tap point and the other to the inverter/comparator trigger point. During the sample phase (ϕ_S), one plate of the capacitors switches to V_{IN}. The change in voltage ($V_{IN} - V_{TAP}$) transfers across the capacitor and forces the inverter into one of the two possible logic states. A latch (connected to the comparator during ϕ_S) restores and propagates the digital level to the decode logic.

The rising edge of the CLK input marks the end of the sampling phase (ϕ_S). Internal delay of the clock circuitry will delay the actual instant when ϕ_S disconnects the latch from the comparator. This delay is called aperture delay (t_{AP}).

The aperture delay is not constant but changes from one cycle to the next. Internal thermal noise, power supply noise and slow input clock edges are major contributors to this variation. The aperture jitter (t_{AJ}) is the variation of the aperture delay distribution.

This uncertainty shows as digital code errors if the input slew rate multiplied by t_{AJ} is of the same order of magnitude as the LSB. That is, if $(dv/dt) * t_{AJ} \approx V_{REF}/256$, an internal 1 LSB of error results.

The logic encodes the 255 bits into a binary code and latches the data in a D-type flip-flop for output. The inputs $\overline{OE1}$ and OE2 control the output buffers in an asynchronous mode.

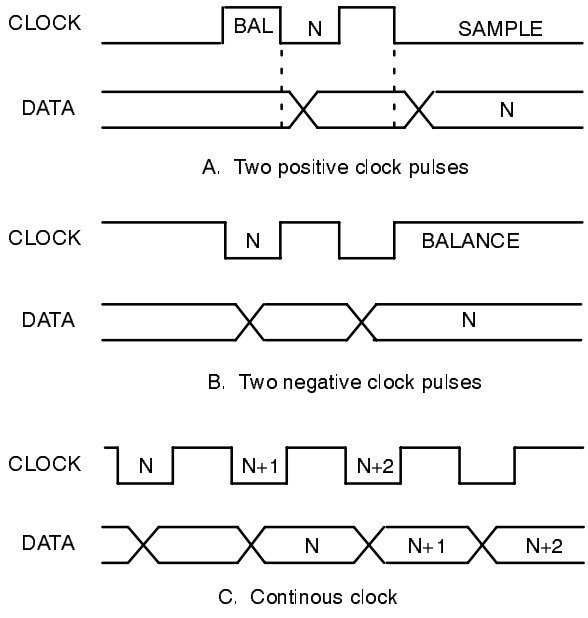


Figure 7. Relationship of Data to Clock

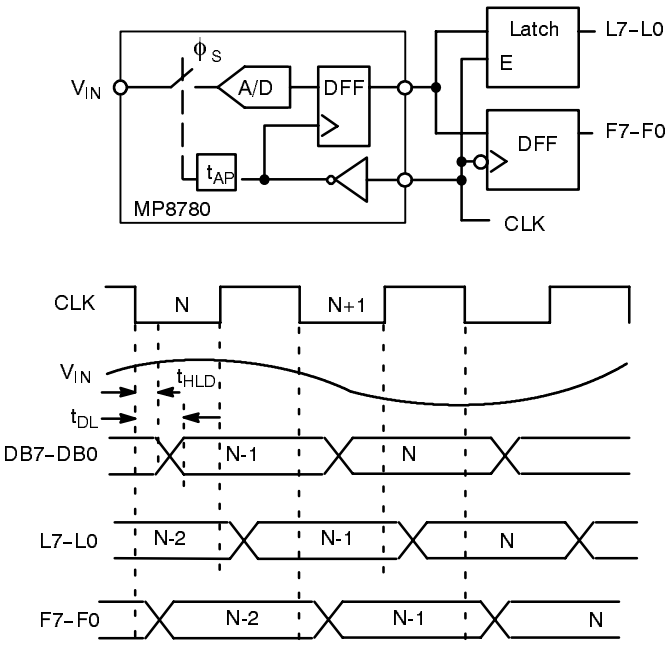


Figure 8. MP8780 Functional Equivalent Circuit and Interface Timing

A system can clock the MP8780 continuously or it may choose to give clock pulses intermittently when a conversion is desired. The timing of *Figure 7B.* keeps the MP8780 comparators in balance and ready to sample the analog input. This mode draws the most current from AV_{DD}. The timing of *Figure 7*A leaves the comparator inputs floating (and AC coupled to the V_{IN} input) and a balance phase is needed before a valid sampling phase. In this mode, I_{DD} varies because of the floating comparator inputs.

This will work at any frequency. If the system must latch with the positive going edge, then care must be taken to avoid the overlay of the clock edge with the changing outputs. If a latch follows the ADC, the positive half of the clock used as enable signal guarantees stable output at the end of the enable pulse.

CHARACTERIZATION CHARTS

Unless Otherwise Specified: V_{DD} = 5 V, F_S = 14.4 MHz (50% Duty Cycle)
$V_{REF(+)}$ = 2.5 V, $V_{REF(-)}$ = GND, Temp = 25°C

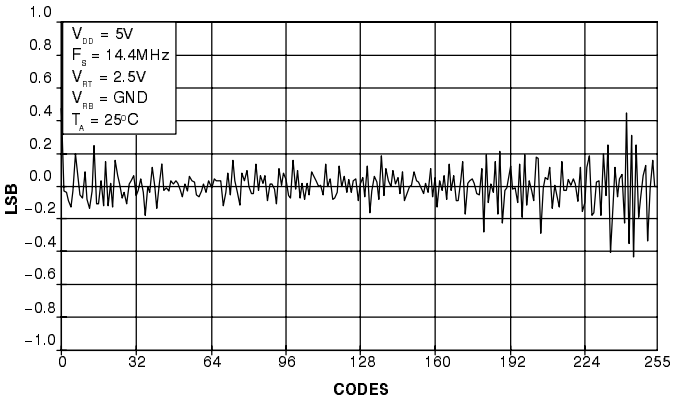


Figure 9. DNL ERROR PLOT

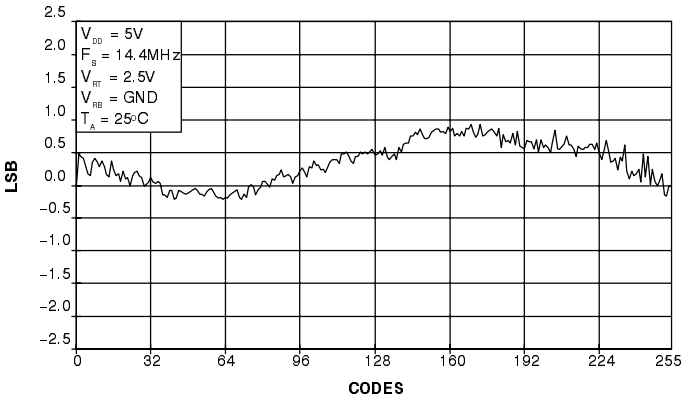


Figure 10. INL ERROR PLOT

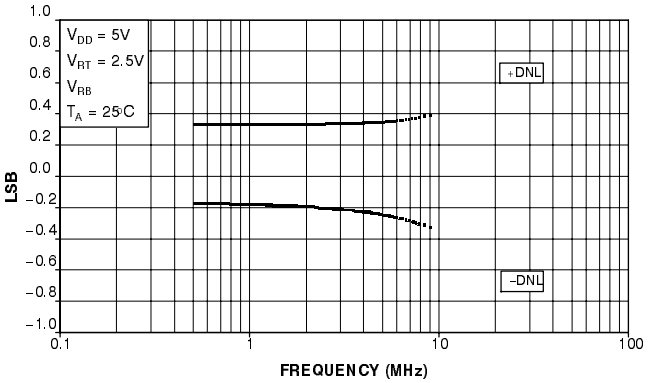


Figure 11. DNL vs FREQUENCY

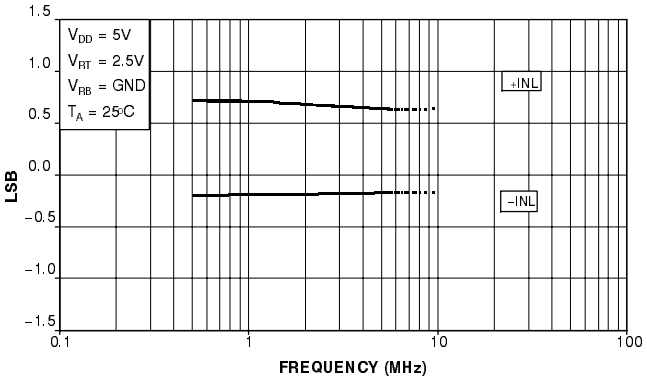


Figure 12. INL vs FREQUENCY

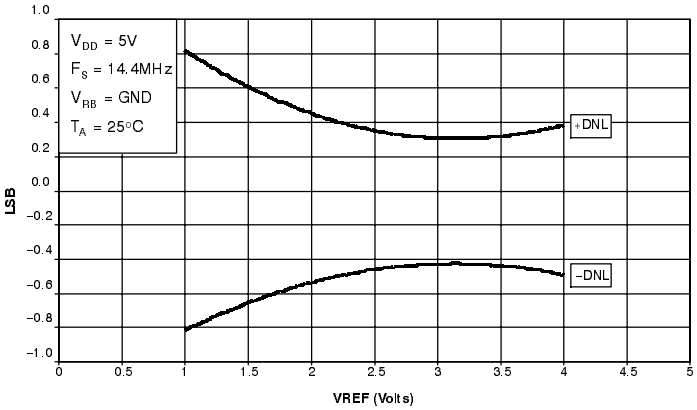


Figure 13. DNL vs VREF

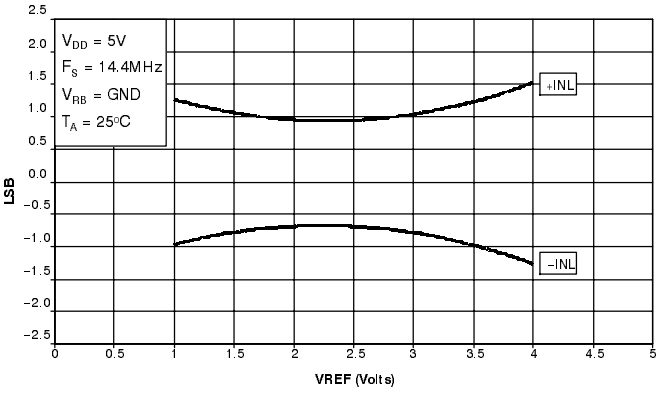


Figure 14. INL vs VREF

CHARACTERIZATION CHARTS (CONT'D)

Unless Otherwise Specified: V_{DD} = 5 V, F_S = 15 MHz (50% Duty Cycle)
$V_{REF(+)}$ = 2.5 V, $V_{REF(-)}$ = GND, Temp = 25°C

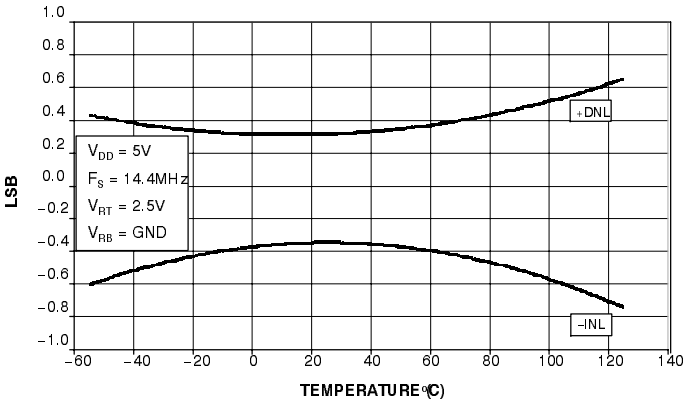


Figure 15. DNL vs TEMPERATURE

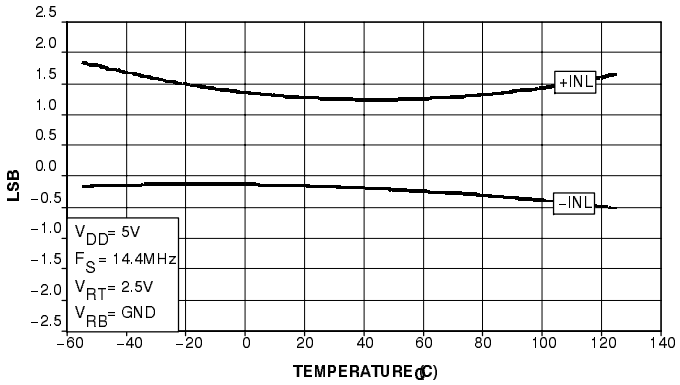


Figure 16. INL vs Temperature

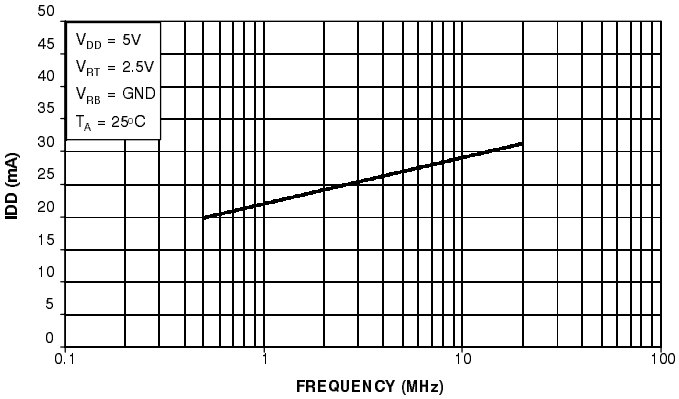


Figure 17. IDD vs FREQUENCY

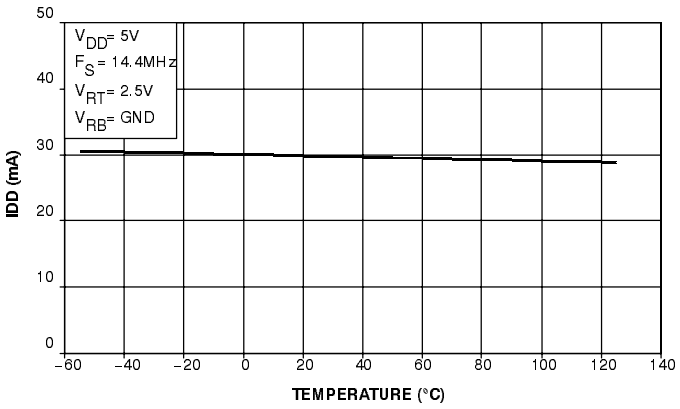


Figure 18. IDD vs TEMPERATURE

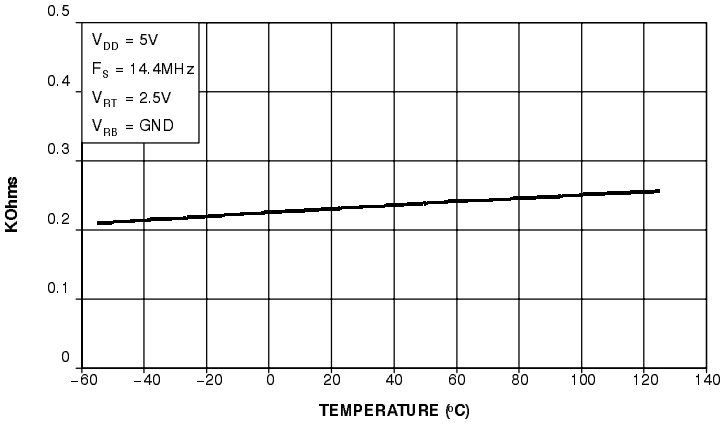


Figure 19. LADDER RESISTANCE vs TEMPERATURE

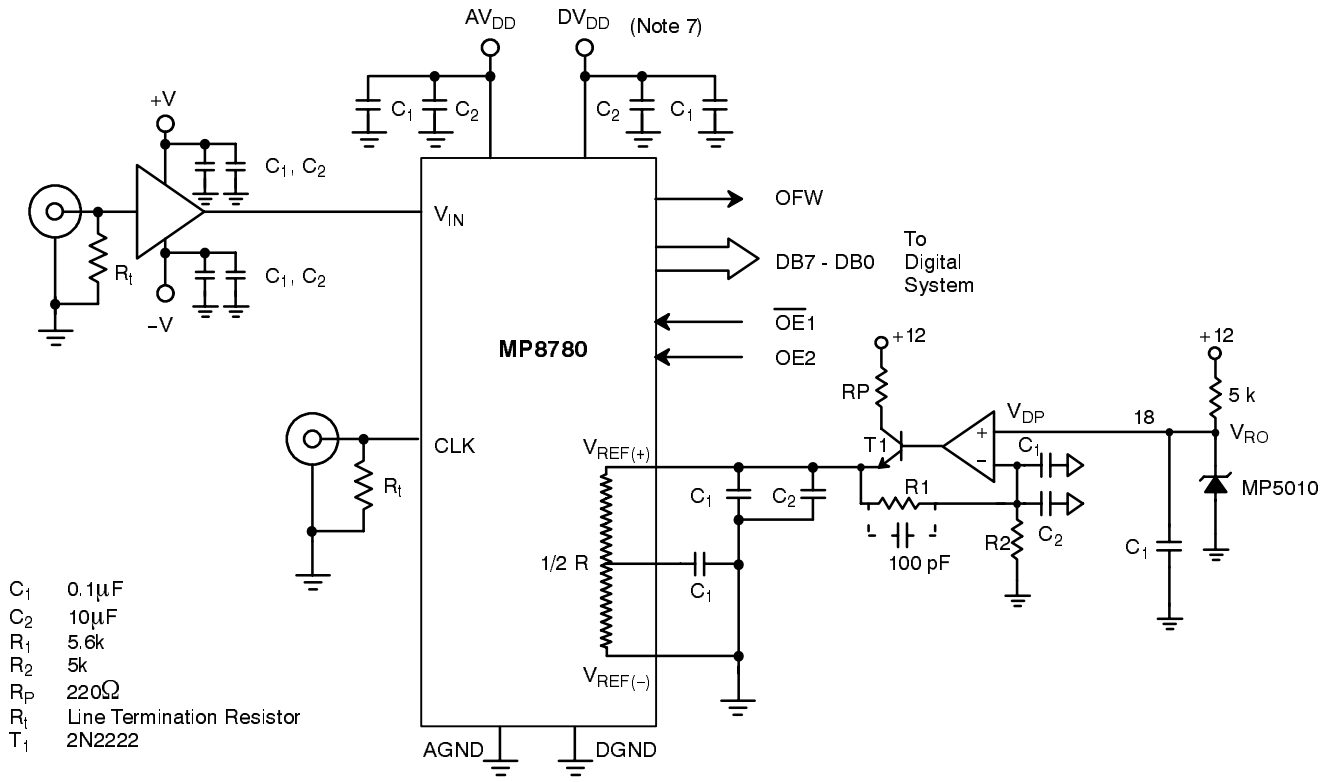


Figure 20. Typical Circuit Connections

The following information will be useful in maximizing the performance of the MP8780.

1. No signals should exceed V_{DD} +0.5 V or GND –0.5 V.
2. Any input pin which can see a signal below GND or above V_{DD} should be protected by diode clamps (1N4148 or HP5082-2835) from input pin to the supplies. All MP8780 inputs have input protection diodes which will protect the device from short transients outside the supply range.
3. The design of a PC board will affect the accuracy of MP8780. Use of wire wrap is not recommended.
4. The analog input signal (V_{IN}) is quite sensitive and should be properly routed and terminated. It should be shielded from the clock and digital outputs so as to minimize cross coupling and noise pickup.
5. The analog input should be driven by a low impedance (less than 50Ω).
6. Analog and digital ground planes should be substantial and common at one point only. The ground plane should act as a shield for parasitics and not a return path for signals. Separate low impedance ground paths will reduce noise levels.
7. DV_{DD} should not be shared with other digital circuitry to avoid conversion errors caused by digital supply transients. In case a separate DV_{DD} for the MP8780 cannot be provided, then DV_{DD} should be connected to AV_{DD} next to the MP8780.
8. Each power supply and reference voltage pin should be decoupled with a ceramic (0.1µF) and a tantalum (10µF) capacitor as close to the device as possible.
9. The digital output should not be driving long wires as the capacitive coupling and reflection will contribute noise to the conversion. When driving distant loads, buffers should be used.

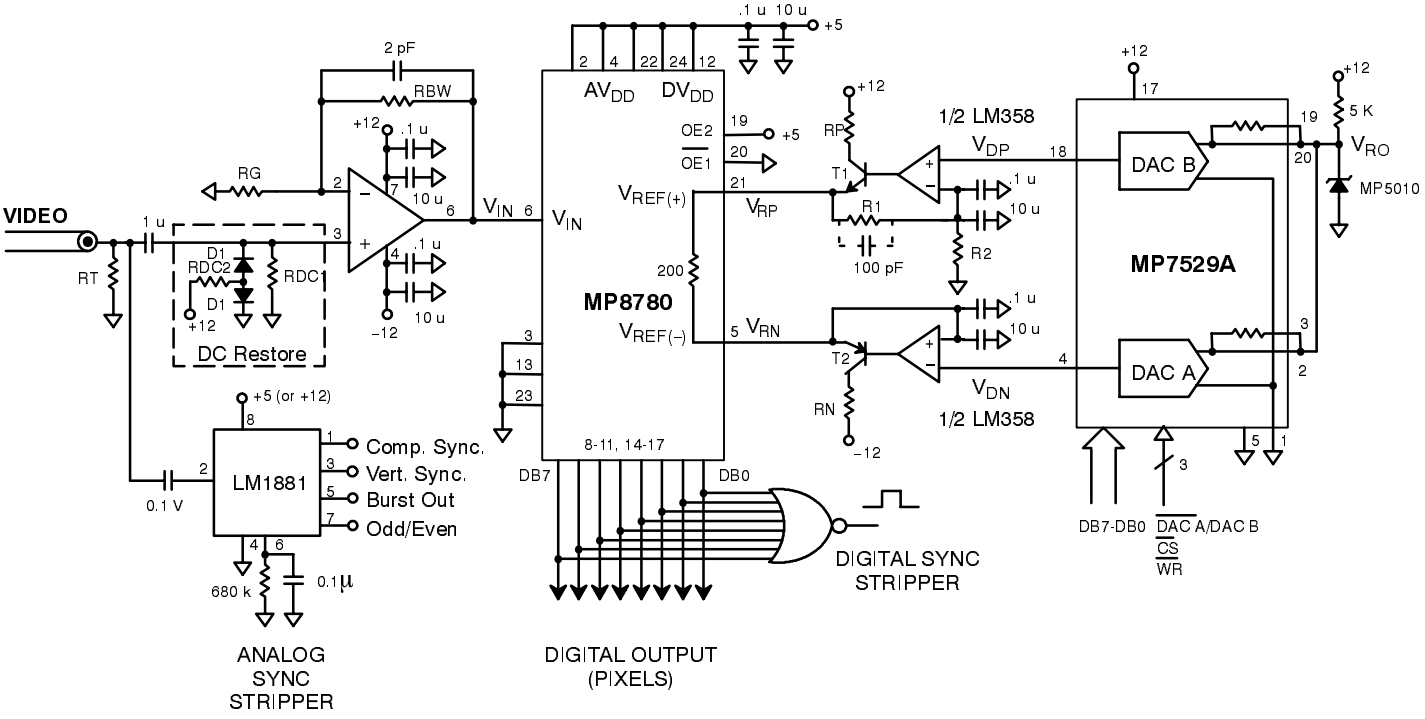


Figure 21. Video Digitizer

D_1	1N4148 (any diode would do)
T_1	2N3903, 2N3904
T_2	2N3905, 2N3906
U_1	EL2030 (others under test)
R_T	75Ω
R_{BW}	750Ω
R_G	750Ω
R_{DC1}	100kΩ
R_{DC2}	100kΩ
R_1	5.6k
R_2	5k
R_P	220Ω
R_N	390Ω