Power Products Division

Advance Information

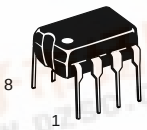
HALF-BRIDGE DRIVER

MPIC2111

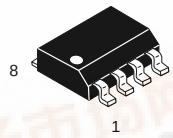
HALF–BRIDGE DRIVER

The MPIC2111 is a high voltage, high speed, power MOSFET and IGBT driver with dependent high and low side referenced output channels designed for half–bridge applications. Proprietary HVIC and latch immune CMOS technologies enable ruggedized monolithic construction. Logic input is compatible with standard CMOS outputs. The output drivers feature a high pulse current buffer stage designed for minimum driver cross–conduction. Internal deadtime is provided to avoid shoot–through in the output half–bridge. The floating channel can be used to drive an N–channel power MOSFET or IGBT in the high side configuration which operates from 10 to 600 volts.

- Floating Channel Designed for Bootstrap Operation
- Fully Operational to +600 V
- Tolerant to Negative Transient Voltage
- dV/dt Immune
- Gate Drive Supply Range from 10 to 20 V
- Undervoltage Lockout for Both Channels
- CMOS Schmitt–triggered Inputs with Pull–down
- Matched Propagation Delay for Both Channels
- Internally Set Deadtime
- High Side Output in Phase with Input



P SUFFIX
PLASTIC PACKAGE
CASE 626–05



D SUFFIX
PLASTIC PACKAGE
CASE 751–05
(SO–8)

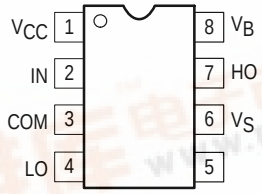
PRODUCT SUMMARY

V_{OFFSET}	600 V MAX
$I_{O+/-}$	200 mA/420 mA
V_{OUT}	10 – 20 V
$t_{on/off}$ (typical)	130 & 90 ns
Deadtime (typical)	700 ns

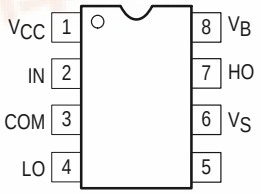
ORDERING INFORMATION

Device	Package
MPIC2111D	SOIC
MPIC2111P	PDIP

PIN CONNECTIONS
(TOP VIEW)



8 LEADS DIP
MPIC2111P

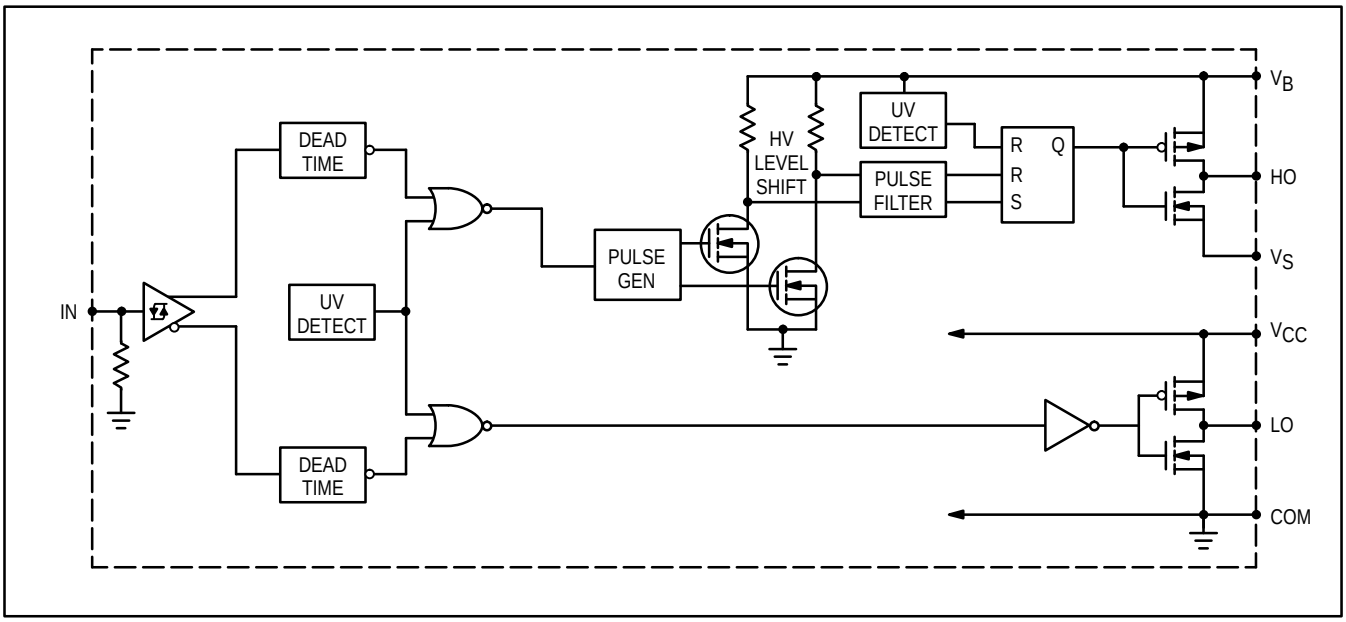


8 LEAD SOIC
MPIC2111D

This document contains information on a new product. Specifications and information herein are subject to change without notice.

REV 1

SIMPLIFIED BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Absolute Maximum Ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM. The Thermal Resistance and Power Dissipation ratings are measured under board mounted and still air conditions.

Rating		Symbol	Min	Max	Unit
High Side Floating Supply Absolute Voltage High Side Floating Supply Offset Voltage High Side Floating Output Voltage Low Side Fixed Supply Voltage Low Side Output Voltage Logic Input Voltage		V_B V_S V_{HO} V_{CC} V_{LO} V_{IN}	–0.3 V_B–25 V_S–0.3 –0.3 –0.3 –0.3	625 V_B+0.3 V_B+0.3 25 V_{CC}+0.3 V_{CC}+0.3	V_{DC}
Allowable Offset Supply Voltage Transient		dV_S/dt	–	50	V/ns
*Package Power Dissipation @ $T_C \leq +25°C$	(8 Lead DIP) (8 Lead SOIC)	P_D –	– –	1.0 0.625	Watt
Thermal Resistance, Junction to Ambient	(8 Lead DIP) (8 Lead SOIC)	$R_{\theta JA}$	– –	125 200	°C/W
Operating and Storage Temperature		T_j, T_{stg}	–55	150	°C
Lead Temperature for Soldering Purposes, 10 seconds		T_L	–	260	°C

RECOMMENDED OPERATING CONDITIONS

The Input/Output logic timing Diagram is shown in Figure 1. For proper operation the device should be used within the recommended conditions. The V_S offset rating is tested with all supplies biased at 15 V differential.

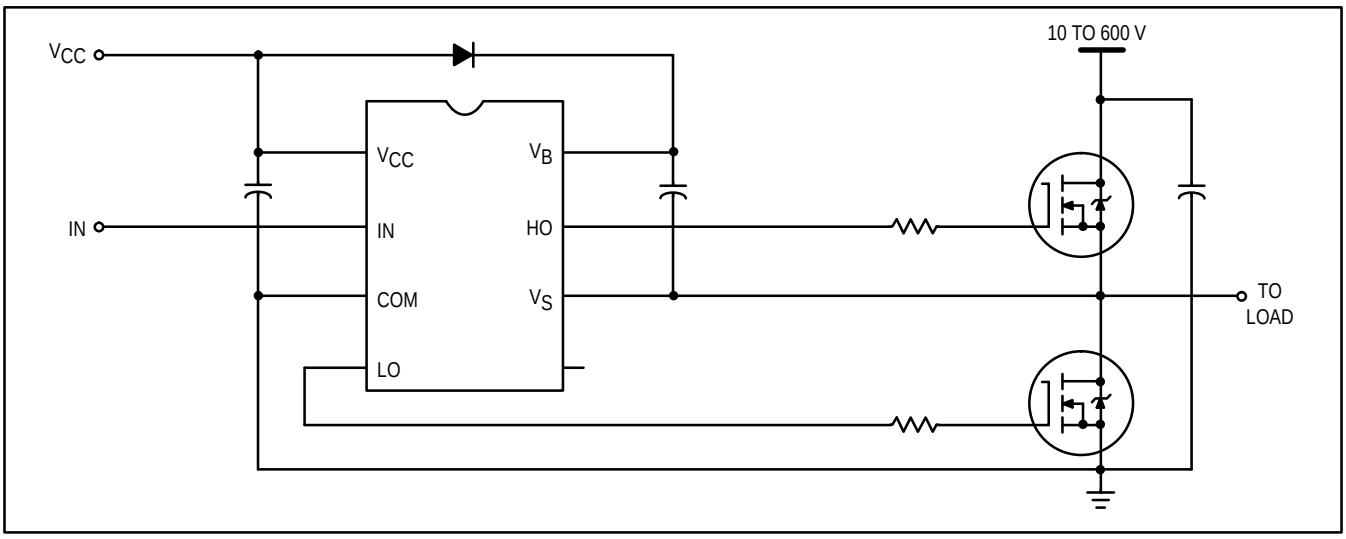
High Side Floating Supply Absolute Voltage	V_B	V_S+10	V_S+20	V
High Side Floating Supply Offset Voltage	V_S	Note 1	600	
High Side Floating Output Voltage	V_{HO}	V_S	V_B	
Low Side Fixed Supply Voltage	V_{CC}	10	20	
Low Side Output Voltage	V_{LO}	0	V_{CC}	mA
Logic Input Voltage	V_{IN}	0	V_{CC}	
Ambient Temperature	T_A	–40	125	°C

Note 1: Logic operational for V_S of –5 to +600 V. Logic state held for V_S of –5 V to $–V_{BS}$.

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise specified)

Characteristic	Symbol	Min	Typ	Max	Unit
STATIC ELECTRICAL CHARACTERISTICS					
V_{BIAS} (V_{CC}, V_{BS}) = 15 V unless otherwise specified. The V_{IN}, V_{TH} and I_{IN} parameters are referenced to COM. The VO and IO parameters are referenced to COM and are applicable to the respective output leads: HO or LO.					
Logic “1” Input Voltage for HO & Logic “0” Input Voltage for LO @ V_{CC} = 10 V	V_{IH}	6.4	–	–	V_{DC}
Logic “1” Input Voltage for HO & Logic “0” Input Voltage for LO @ V_{CC} = 15 V	V_{IH}	9.5	–	–	
Logic “1” Input Voltage for HO & Logic “0” Input Voltage for LO @ V_{CC} = 20 V	V_{IH}	12.6	–	–	
Logic “0” Input Voltage for HO & Logic “1” Input Voltage for LO @ V_{CC} = 10 V	V_{IL}	–	–	3.8	
Logic “0” Input Voltage for HO & Logic “1” Input Voltage for LO @ V_{CC} = 15 V	V_{IL}	–	–	6.0	
Logic “0” Input Voltage for HO & Logic “1” Input Voltage for LO @ V_{CC} = 20 V	V_{IL}	–	–	8.3	
High Level Output Voltage, V_{BIAS}–V_O @ I_O = 0 A	V_{OH}	–	–	100	mV
Low Level Output Voltage, V_O @ I_O = 0 A	V_{OL}	–	–	100	
Offset Supply Leakage Current @ V_B = V_S = 600 V	I_{LK}	–	–	50	µA
Quiescent V_{BS} Supply Current @ V_{IN} = 0 V or V_{CC}	I_{QBS}	–	50	–	
Quiescent V_{CC} Supply Current @ V_{IN} = 0 V or V_{CC}	I_{QCC}	–	70	–	
Logic “1” Input Bias Current @ V_{IN} = 15 V	I_{IN+}	–	20	40	
Logic “0” Input Bias Current @ V_{IN} = 0 V	$I_{IN–}$	–	–	1.0	
V_{BS} Supply Undervoltage Positive Going Threshold	V_{BSUV+}	–	8.5	–	V
V_{BS} Supply Undervoltage Negative Going Threshold	$V_{BSUV–}$	–	8.2	–	
V_{CC} Supply Undervoltage Positive Going Threshold	V_{CCUV+}	–	8.6	–	
V_{CC} Supply Undervoltage Negative Going Threshold	$V_{CCUV–}$	–	8.2	–	
Output High Short Circuit Pulsed Current @ V_{OUT} = 0 V, PW ≤ 10 µs	I_{O+}	200	250	–	mA
Output Low Short Circuit Pulsed Current @ V_{OUT} = 15 V, PW ≤ 10 µs	$I_{O–}$	420	500	–	
DYNAMIC ELECTRICAL CHARACTERISTICS					
V_{BIAS} (V_{CC}, V_{BS}) = 15 V unless otherwise specified					
Turn–On Propagation Delay @ V_S = 0 V	t_{on}	–	850	–	ns
Turn–Off Propagation Delay @ V_S = 600 V	t_{off}	–	150	–	
Turn–On Rise Time @ C_L = 1000 pF	t_r	–	80	–	
Turn–Off Fall Time @ C_L = 1000 pF	t_f	–	40	–	
Deadtime, LS Turn–Off to HS Turn–On & HS Turn–Off to LS Turn–On	DT	–	700	–	
Delay Matching, HS & LS Turn–On/Off	MT	–	30	–	

TYPICAL CONNECTION



LEAD DEFINITIONS

Symbol	Lead Description
IN	Logic Input for High Side and Low Side Gate Driver Outputs (HO & LO), In Phase with HO
V_B	High Side Floating Supply
HO	High Side Gate Drive Output
V_S	High Side Floating Supply Return
V_{CC}	Low Side Supply
L_O	Low Side Gate Drive Output
COM	Logic and Low Side Return

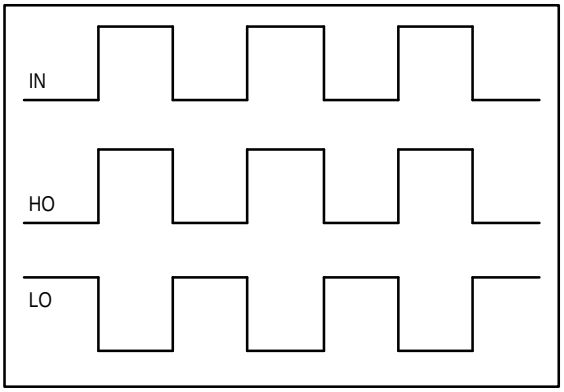


Figure 1. Input / Output Timing Diagram

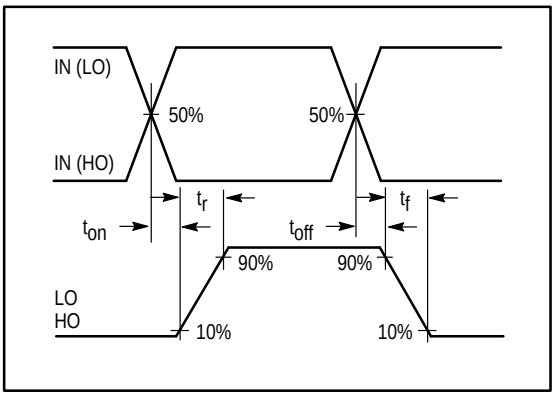


Figure 2. Switching Time Waveform Definitions

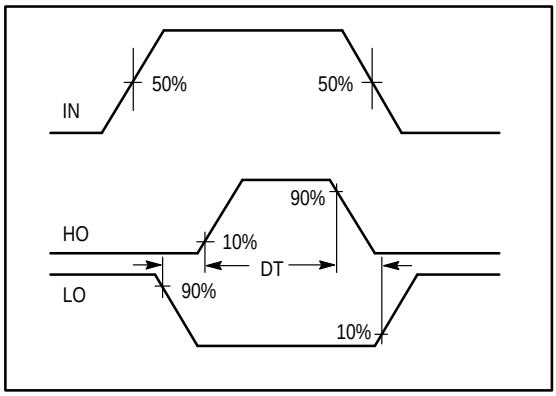
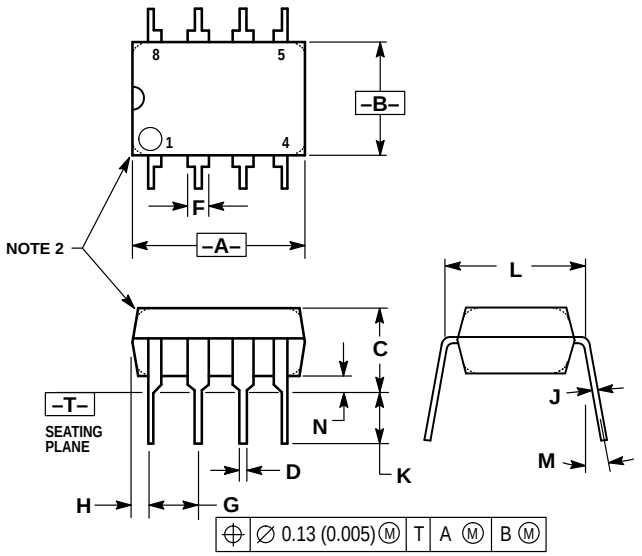


Figure 3. Deadtime Waveform Definitions

PACKAGE DIMENSIONS

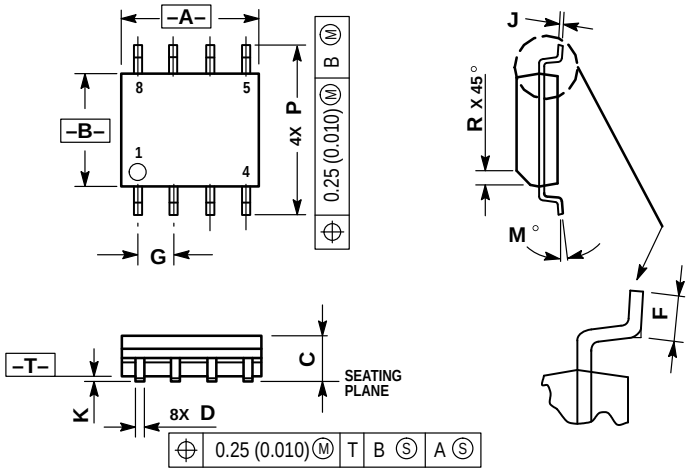


NOTES:
1. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
2. PACKAGE CONTOUR OPTIONAL (ROUND OR SQUARE CORNERS).
3. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	9.40	10.16	0.370	0.400
B	6.10	6.60	0.240	0.260
C	3.94	4.45	0.155	0.175
D	0.38	0.51	0.015	0.020
F	1.02	1.78	0.040	0.070
G	2.54 BSC		0.100 BSC	
H	0.76	1.27	0.030	0.050
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	7.62 BSC		0.300 BSC	
M	—	10°	—	10°
N	0.76	1.01	0.030	0.040

STYLE 1:
PIN 1. AC IN
2. DC + IN
3. DC – IN
4. AC IN
5. GROUND
6. OUTPUT
7. AUXILIARY
8. V_{CC}

CASE 626–05
ISSUE K



NOTES:
1. DIMENSIONS A AND B ARE DATUMS AND T IS A DATUM SURFACE.
2. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
3. DIMENSIONS ARE IN MILLIMETER.
4. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
5. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
6. DIMENSION D DOES NOT INCLUDE MOLD PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS	
DIM	MIN	MAX
A	4.80	5.00
B	3.80	4.00
C	1.35	1.75
D	0.35	0.49
F	0.40	1.25
G	1.27 BSC	
J	0.18	0.25
K	0.10	0.25
M	0°	7°
P	5.80	6.20
R	0.25	0.50

CASE 751–05
ISSUE P

How to reach us:
USA / EUROPE / Locations Not Listed: Motorola Literature Distribution; P.O. Box 20912; Phoenix, Arizona 85036. 1–800–441–2447 or 602–303–5454

MFAX: RMFAX0@email.sps.mot.com – TOUCHTONE 602–244–6609
INTERNET: http://Design–NET.com

JAPAN: Nippon Motorola Ltd.; Tatsumi–SPD–JLDC, 6F Seibu–Butsuryu–Center, 3–14–2 Tatsumi Koto–Ku, Tokyo 135, Japan. 03–81–3521–8315

ASIA / PACIFIC: Motorola Semiconductors H.K. Ltd.; 8B Tai Ping Industrial Park, 51 Ting Kok Road, Tai Po, N.T., Hong Kong. 852–26629298