Power Products Division

Advance Information

HALF-BRIDGE DRIVER

The MPIC2111 is a high voltage, high speed, power MOSFET and IGBT driver with dependent high and low side referenced output channels designed for halfbridge applications. Proprietary HVIC and latch immune CMOS technologies enable ruggedized monolithic construction. Logic input is compatible with standard CMOS outputs. The output drivers feature a high pulse current buffer stage designed for minimum driver cross-conduction. Internal deadtime is provided to avoid shoot-through in the output half-bridge. The floating channel can be used to drive an N-channel power MOSFET or IGBT in the high side configuration which operates from 10 to 600 volts.

- Floating Channel Designed for Bootstrap Operation
- Fully Operational to +600 V
- Tolerant to Negative Transient Voltage
- dV/dt Immune
- Gate Drive Supply Range from 10 to 20 V
- Undervoltage Lockout for Both Channels
- CMOS Schmitt-triggered Inputs with Pull-down
- Matched Propagation Delay for Both Channels
- Internally Set Deadtime
- High Side Output in Phase with Input

PRODUCT SUMMARY

700 ns

VOFFSET **600 V MAX** 10+/-200 mA/420 mA

VOUT 10 - 20 V WW.DZSC.COM ton/off (typical) 130 & 90 ns Deadtime (typical)

HALF-BRIDGE DRIVER

MPIC2111



PLASTIC PACKAGE CASE 626-05



D SUFFIX LASTIC PACKAGE CASE 751-05 (SO-8)

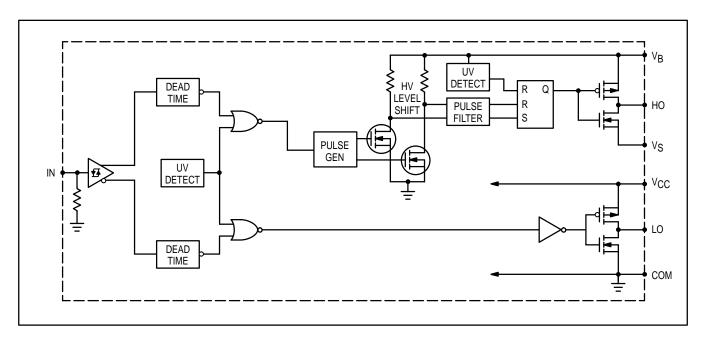
ORDERING INFORMATION

| Device | Package |
|-----------|---------|
| MPIC2111D | SOIC |
| MPIC2111P | PDIP |



This document contains information on a new product. Specifications and information herein are subject o change without notice.

SIMPLIFIED BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Absolute Maximum Ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM. The Thermal Resistance and Power Dissipation ratings are measured under board mounted and still air conditions.

| Rating | | Symbol | Min | Max | Unit |
|---|-------------------------------|--------------------------------------|---|---|-----------------|
| High Side Floating Supply Absolute Voltage High Side Floating Supply Offset Voltage High Side Floating Output Voltage Low Side Fixed Supply Voltage Low Side Output Voltage Logic Input Voltage | | VB VS VHO VCC VLO VIN | -0.3 V _B -25 V _S -0.3 -0.3 -0.3 | 625 VB+0.3 VB+0.3 25 VCC+0.3 VCC+0.3 | ^V DC |
| Allowable Offset Supply Voltage Transient | | dV _S /dt | - | 50 | V/ns |
| *Package Power Dissipation @ T _C ≤ +25°C | (8 Lead DIP) (8 Lead SOIC) | P _D - | - - | 1.0 0.625 | Watt |
| Thermal Resistance, Junction to Ambient | (8 Lead DIP) (8 Lead SOIC) | $R_{	heta JA}$ | - - | 125 200 | °C/W |
| Operating and Storage Temperature | | T _j , T _{stg} | - 55 | 150 | °C |
| Lead Temperature for Soldering Purposes, 10 se | TL | - | 260 | °C | |

RECOMMENDED OPERATING CONDITIONS

The Input/Output logic timing Diagram is shown in Figure 1. For proper operation the device should be used within the recommended conditions. The V_S offset rating is tested with all supplies biased at 15 V differential.

| 9 9 | | | | | |
|--|----------------|--------------------|--------------------|----|--|
| High Side Floating Supply Absolute Voltage | V _B | V _S +10 | V _S +20 | V | |
| High Side Floating Supply Offset Voltage | ٧S | Note 1 | 600 | | |
| High Side Floating Output Voltage | Vно | ٧s | VB | | |
| Low Side Fixed Supply Voltage | Vcc | 10 | 20 | | |
| Low Side Output Voltage | VLO | 0 | VCC | mA | |
| Logic Input Voltage | VIN | 0 | VCC | | |
| Ambient Temperature | TA | -40 | 125 | °C | |

Note 1: Logic operational for V_S of –5 to +600 V. Logic state held for V_S of –5 V to –V_{BS}.

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise specified)

| Characteristic | Symbol | Min | Тур | Max | Unit | |
|--|--------|-----|-----|-----|------|--|
| OTATIO EL FOTDIO AL OLLA DA OTEDIOTICO | | | | | | |

STATIC ELECTRICAL CHARACTERISTICS

 V_{BIAS} (V_{CC} , V_{BS}) = 15 V unless otherwise specified. The V_{IN} , V_{TH} and I_{IN} parameters are referenced to COM. The VO and IO parameters are referenced to COM and are applicable to the respective output leads: HO or LO.

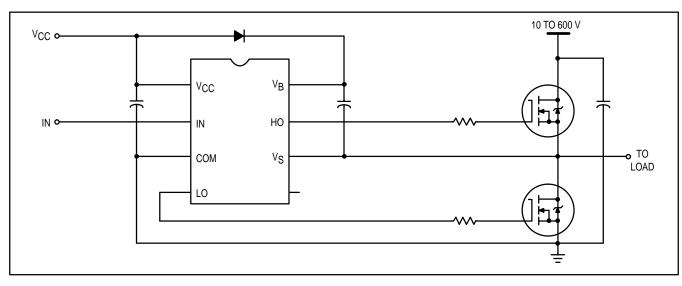
| are received to command are approached to the respective earlier reader re- | | | | | |
|--|---------------------|------|-----|-----|-----|
| Logic "1" Input Voltage for HO & Logic "0" Input Voltage for LO @ V _{CC} = 10 V | V _{IH} | 6.4 | _ | _ | VDC |
| Logic "1" Input Voltage for HO & Logic "0" Input Voltage for LO @ V _{CC} = 15 V | VIH | 9.5 | _ | _ | |
| Logic "1" Input Voltage for HO & Logic "0" Input Voltage for LO @ V _{CC} = 20 V | V _{IH} | 12.6 | - | _ | |
| Logic "0" Input Voltage for HO & Logic "1" Input Voltage for LO @ V _{CC} = 10 V | VIL | - | - | 3.8 | |
| Logic "0" Input Voltage for HO & Logic "1" Input Voltage for LO @ V_{CC} = 15 V | V _{IL} | - | - | 6.0 |] |
| Logic "0" Input Voltage for HO & Logic "1" Input Voltage for LO @ V _{CC} = 20 V | VIL | - | - | 8.3 | |
| High Level Output Voltage, V _{BIAS} -V _O @ I _O = 0 A | Voн | - | - | 100 | mV |
| Low Level Output Voltage, V _O @ I _O = 0 A | VOL | - | - | 100 | |
| Offset Supply Leakage Current @ V _B = V _S = 600 V | llK | - | - | 50 | μΑ |
| Quiescent V _{BS} Supply Current @ V _{IN} = 0 V or V _{CC} | I _{QBS} | - | 50 | _ | |
| Quiescent V _{CC} Supply Current @ V _{IN} = 0 V or V _{CC} | | - | 70 | - | |
| Logic "1" Input Bias Current @ V _{IN} = 15 V | I _{IN+} | - | 20 | 40 | |
| Logic "0" Input Bias Current @ V _{IN} = 0 V | I _{IN} _ | - | - | 1.0 | |
| V _{BS} Supply Undervoltage Positive Going Threshold | V _{BSUV+} | - | 8.5 | _ | V |
| V _{BS} Supply Undervoltage Negative Going Threshold | V _{BSUV} - | - | 8.2 | _ | |
| V _{CC} Supply Undervoltage Positive Going Threshold | VCCUV+ | - | 8.6 | - | |
| V _{CC} Supply Undervoltage Negative Going Threshold | VCCUV- | - | 8.2 | _ | |
| Output High Short Circuit Pulsed Current @ $V_{OUT} = 0 V$, $PW \le 10 \mu s$ | IO+ | 200 | 250 | _ | mA |
| Output Low Short Circuit Pulsed Current @ V_{OUT} = 15 V, PW \leq 10 μs | I _O _ | 420 | 500 | - |] |
| | | • | • | • | • |

DYNAMIC ELECTRICAL CHARACTERISTICS

 V_{BIAS} (V_{CC}, V_{BS}) = 15 V unless otherwise specified

| Turn–On Propagation Delay @ V _S = 0 V | t _{on} | _ | 850 | _ | ns |
|---|-----------------|---|-----|---|----|
| Turn–Off Propagation Delay @ V _S = 600 V | toff | 1 | 150 | ı | |
| Turn–On Rise Time @ C _L = 1000 pF | t _r | - | 80 | - | |
| Turn–Off Fall Time @ C _L = 1000 pF | t _f | 1 | 40 | 1 | |
| Deadtime, LS Turn-Off to HS Turn-On & HS Turn-Off to LS Turn-On | DT | ı | 700 | ı | |
| Delay Matching, HS & LS Turn-On/Off | MT | _ | 30 | _ | |

TYPICAL CONNECTION



MPIC2111

LEAD DEFINITIONS

| Symbol | Lead Description | | |
|----------------|--|--|--|
| IN | Logic Input for High Side and Low Side Gate Driver Outputs (HO & LO), In Phase with HO | | |
| V _B | High Side Floating Supply | | |
| НО | High Side Gate Drive Output | | |
| ٧s | High Side Floating Supply Return | | |
| VCC | Low Side Supply | | |
| LO | Low Side Gate Drive Output | | |
| COM | Logic and Low Side Return | | |

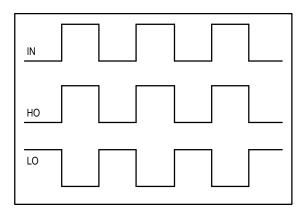


Figure 1. Input / Output Timing Diagram

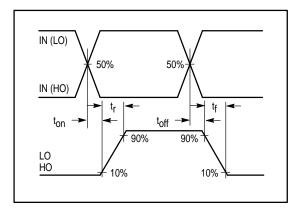


Figure 2. Switching Time Waveform Definitions

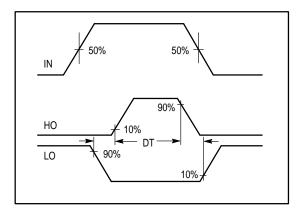
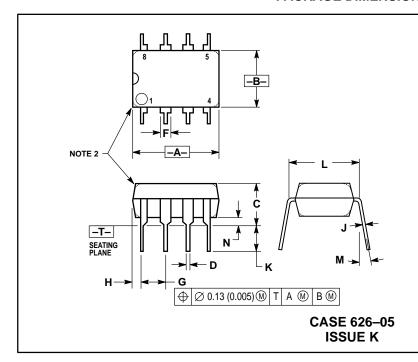


Figure 3. Deadtime Waveform Definitions

PACKAGE DIMENSIONS



- NOTES:

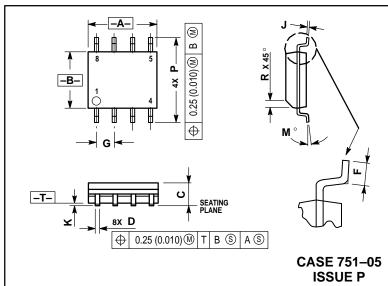
 1. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.

 2. PACKAGE CONTOUR OPTIONAL (ROUND OR CONTOUR OPTIONAL (ROUND O
- 2. PACKAGE CONTOUR OF HUMAL (ROUND OR SQUARE CORNERS).
 3. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.

| | MILLIMETERS | | INC | HES |
|-----|-------------|-------|-----------|-------|
| DIM | MIN | MAX | MIN MAX | |
| Α | 9.40 | 10.16 | 0.370 | 0.400 |
| В | 6.10 | 6.60 | 0.240 | 0.260 |
| С | 3.94 | 4.45 | 0.155 | 0.175 |
| D | 0.38 | 0.51 | 0.015 | 0.020 |
| F | 1.02 | 1.78 | 0.040 | 0.070 |
| G | 2.54 | BSC | 0.100 BSC | |
| Н | 0.76 | 1.27 | 0.030 | 0.050 |
| J | 0.20 | 0.30 | 0.008 | 0.012 |
| K | 2.92 | 3.43 | 0.115 | 0.135 |
| Г | 7.62 | BSC | 0.300 BSC | |
| М | | 10° | | 10° |
| N | 0.76 | 1.01 | 0.030 | 0.040 |

STYLE 1:
PIN 1. AC IN
2. DC + IN
3. DC - IN
4. AC IN
5. GROUND
6. OUTPUT
7. AUXILIARY
8. VCc

8. V_{CC}



- NOTES:

 1. DIMENSIONS A AND B ARE DATUMS AND T IS A DATUM SURFACE.

 2. DIMENSIONING AND TOLERANCING PER ANSI Y14,5M, 1982.

 3. DIMENSIONS ARE IN MILLIMETER.

 4. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.

 5. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
- DIMENSION D DOES NOT INCLUDE MOLD
 PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL

| | MILLIMETERS | | | |
|-----|-------------|------|--|--|
| DIM | MIN MAX | | | |
| Α | 4.80 | 5.00 | | |
| В | 3.80 | 4.00 | | |
| С | 1.35 | 1.75 | | |
| D | 0.35 | 0.49 | | |
| F | 0.40 | 1.25 | | |
| G | 1.27 BSC | | | |
| 7 | 0.18 | 0.25 | | |
| K | 0.10 | 0.25 | | |
| M | 0° | 7° | | |
| Р | 5.80 | 6.20 | | |
| R | 0.25 | 0.50 | | |

MPIC2111

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