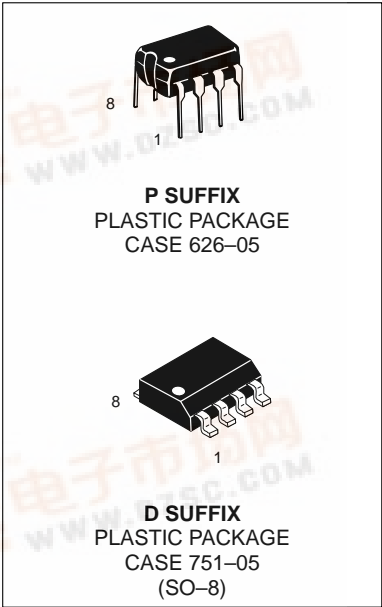


Power Products Division
Advance Information
SINGLE CHANNEL DRIVER



The MPIC2117 is a high voltage, high speed, power MOSFET and IGBT driver. Proprietary HVIC and latch immune CMOS technologies enable ruggedized monolithic construction. The logic input is compatible with standard CMOS outputs. The output drivers feature a high pulse current buffer stage designed for minimum driver cross-conduction. The floating channel can be used to drive an N-channel power MOSFET or IGBT in the high side or low side configuration which operates from 10 to 600 volts.

- Floating Channel Designed for Bootstrap Operation
- Fully Operational to +600 V
- Tolerant to Negative Transient Voltage
- dV/dt Immune
- Gate Drive Supply Range from 10 to 20 V
- Undervoltage Lockout
- CMOS Schmitt-triggered Input with Pull-down
- Output In Phase with Input



PRODUCT SUMMARY

V_{OFFSET}	600 V MAX
I_{O+/-}	200 mA/420 mA
V_{OUT}	10 – 20 V
t_{on/off} (typical)	125 & 105 ns

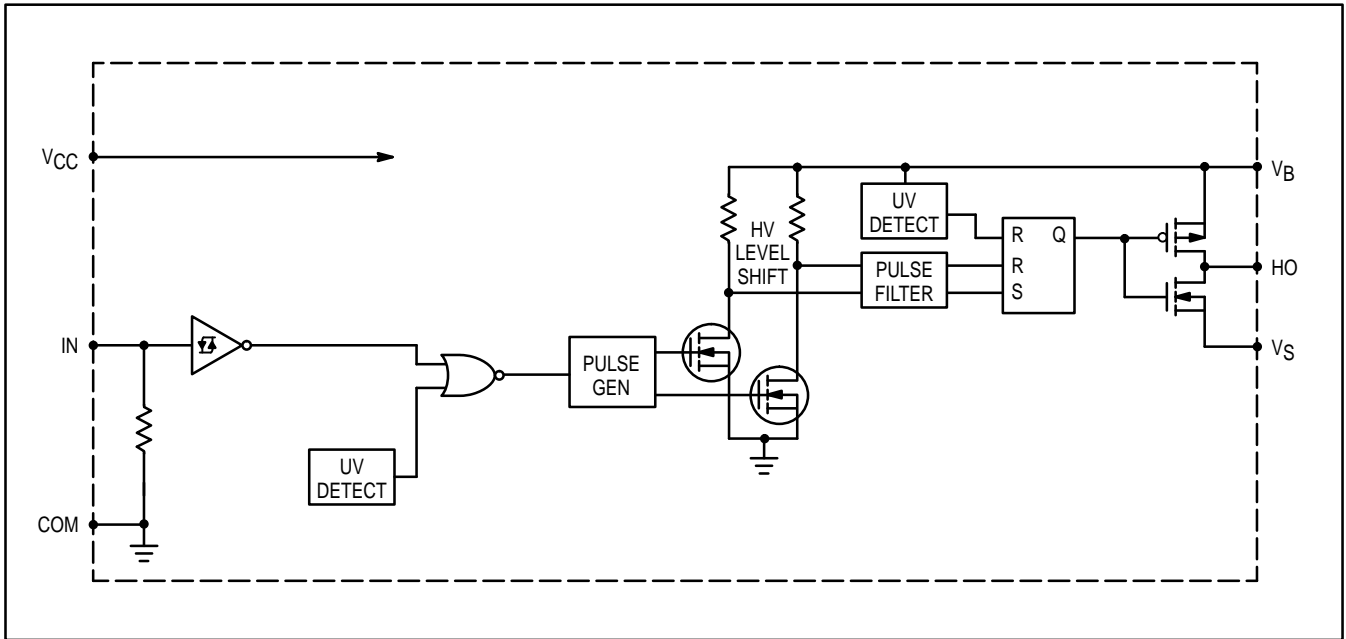
ORDERING INFORMATION

Device	Package
MPIC2117D	SOIC
MPIC2117P	PDIP



MPIC2117

SIMPLIFIED BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Absolute Maximum Ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM. The Thermal Resistance and Power Dissipation ratings are measured under board mounted and still air conditions.

Rating	Symbol	Min	Max	Unit
High Side Floating Supply Absolute Voltage	V_B	-0.3	625	VDC
High Side Floating Supply Offset Voltage	V_S	V_B-25	$V_B+0.3$	
High Side Floating Output Voltage	V_{HO}	$V_S-0.3$	$V_B+0.3$	
Logic Supply Voltage	V_{CC}	-0.3	25	
Logic Input Voltage	V_{IN}	-0.3	$V_{CC}+0.3$	
Allowable Offset Supply Voltage Transient	dV_S/dt	-	50	V/ns
*Package Power Dissipation @ $T_A \leq +25^\circ\text{C}$	(8 Lead DIP) P_D (8 Lead SOIC) -	-	1.0 0.625	Watt
Thermal Resistance, Junction to Ambient	(8 Lead DIP) $R_{\theta JA}$ (8 Lead SOIC)	-	125 200	$^\circ\text{C}/\text{W}$
Operating and Storage Temperature	T_j, T_{stg}	-55	150	$^\circ\text{C}$
Lead Temperature for Soldering Purposes, 10 seconds	T_L	-	260	$^\circ\text{C}$

RECOMMENDED OPERATING CONDITIONS

The Input/Output logic timing Diagram is shown in Figure 1. For proper operation the device should be used within the recommended conditions. The V_S offset rating is tested with all supplies biased at 15 V differential.

High Side Floating Supply Absolute Voltage	V_B	V_S+10	V_S+20	V
High Side Floating Supply Offset Voltage	V_S	Note 1	600	
High Side Floating Output Voltage	V_{HO}	V_S	V_B	
Logic Supply Voltage	V_{CC}	10	20	
Logic Input Voltage	V_{IN}	0	V_{CC}	
Ambient Temperature	T_A	-40	125	$^\circ\text{C}$

Note 1: Logic operational for V_S of -5 to +600 V. Logic state held for V_S of -5 V to $-V_{BS}$.

ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ unless otherwise specified)

Characteristic	Symbol	Min	Typ	Max	Unit
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STATIC ELECTRICAL CHARACTERISTICS

V_{BIAS} (V_{CC} , V_{BS}) = 15 V unless otherwise specified. The V_{IN} , V_{TH} and I_{IN} parameters are referenced to COM. The V_O and I_O parameters are referenced to COM and are applicable to the respective output leads: HO or LO.

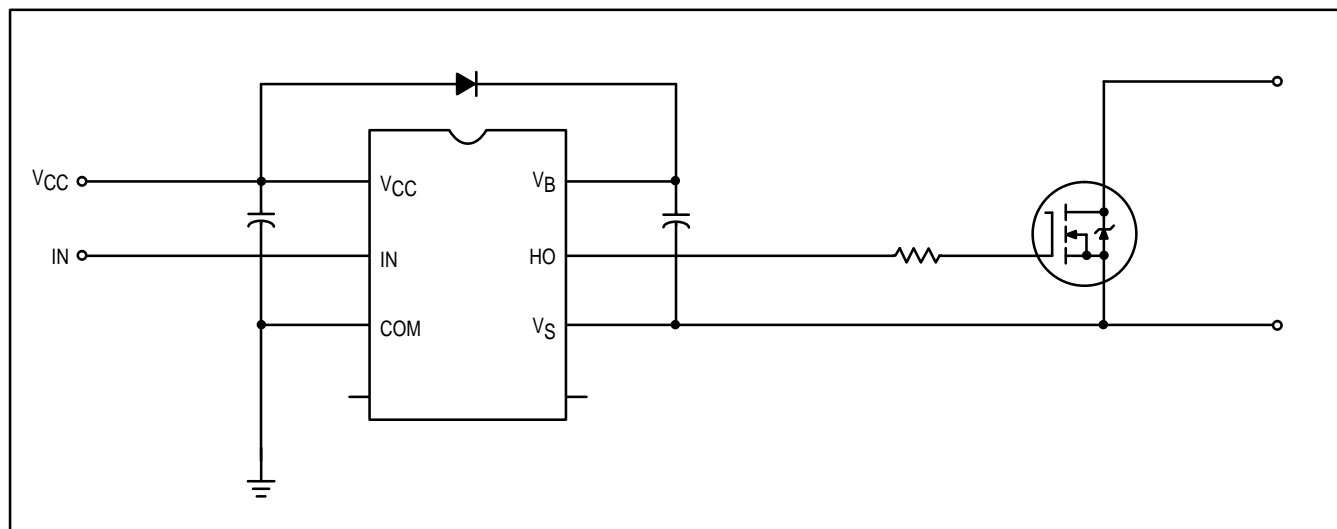
Logic "1" Input Voltage @ $V_{CC} = 10\text{ V}$	V_{IH}	6.4	–	–	V _{DC}
Logic "1" Input Voltage @ $V_{CC} = 15\text{ V}$	V_{IH}	9.5	–	–	
Logic "1" Input Voltage @ $V_{CC} = 20\text{ V}$	V_{IH}	12.6	–	–	
Logic "0" Input Voltage @ $V_{CC} = 10\text{ V}$	V_{IL}	–	–	3.8	
Logic "0" Input Voltage @ $V_{CC} = 15\text{ V}$	V_{IL}	–	–	6.0	
Logic "0" Input Voltage @ $V_{CC} = 20\text{ V}$	V_{IL}	–	–	8.3	
High Level Output Voltage, $V_{BS}-V_O$ @ $V_{IN} = V_{IH}$, $I_O = 0\text{ A}$	V_{OH}	–	–	100	mV
Low Level Output Voltage, V_O @ $V_{IN} = V_{IL}$, $I_O = 0\text{ A}$	V_{OL}	–	–	100	
Offset Supply Leakage Current @ $V_B = V_S = 600\text{ V}$	I_{LK}	–	–	50	μA
Quiescent V_{BS} Supply Current @ $V_{IN} = 0\text{ V}$ or V_{CC}	I_{QBS}	–	50	–	
Quiescent V_{CC} Supply Current @ $V_{IN} = 0\text{ V}$ or V_{CC}	I_{QCC}	–	70	–	
Logic "1" Input Bias Current @ $V_{IN} = 15\text{ V}$	I_{IN+}	–	20	40	
Logic "0" Input Bias Current @ $V_{IN} = 0\text{ V}$	I_{IN-}	–	–	1.0	
V_{BS} Supply Undervoltage Positive Going Threshold	V_{BSUV+}	–	8.5	–	V
V_{BS} Supply Undervoltage Negative Going Threshold	V_{BSUV-}	–	8.2	–	
V_{CC} Supply Undervoltage Positive Going Threshold	V_{CCUV+}	–	8.6	–	
V_{CC} Supply Undervoltage Negative Going Threshold	V_{CCUV-}	–	8.2	–	
Output High Short Circuit Pulsed Current @ $V_{OUT} = 0\text{ V}$, $V_{IN} = 15\text{ V}$, $PW \leq 10\ \mu\text{s}$	I_{O+}	200	250	–	mA
Output Low Short Circuit Pulsed Current @ $V_{OUT} = 15\text{ V}$, $V_{IN} = 0\text{ V}$, $PW \leq 10\ \mu\text{s}$	I_{O-}	420	500	–	

DYNAMIC ELECTRICAL CHARACTERISTICS

V_{BIAS} (V_{CC} , V_{BS}) = 15 V unless otherwise specified

Turn-On Propagation Delay @ $V_S = 0\text{ V}$	t_{on}	–	125	–	ns
Turn-Off Propagation Delay @ $V_S = 600\text{ V}$	t_{off}	–	105	–	
Turn-On Rise Time @ $C_L = 1000\text{ pF}$	t_r	–	80	–	
Turn-Off Fall Time @ $C_L = 1000\text{ pF}$	t_f	–	40	–	

TYPICAL CONNECTION



MPIC2117

LEAD DEFINITIONS

Symbol	Lead Description
V _{CC}	Logic Supply
IN	Logic Input for High Side Gate Driver Outputs (HO), In Phase with HO
COM	Logic Ground
V _B	High Side Floating Supply
HO	High Side Gate Drive Output
V _S	High Side Floating Supply Return

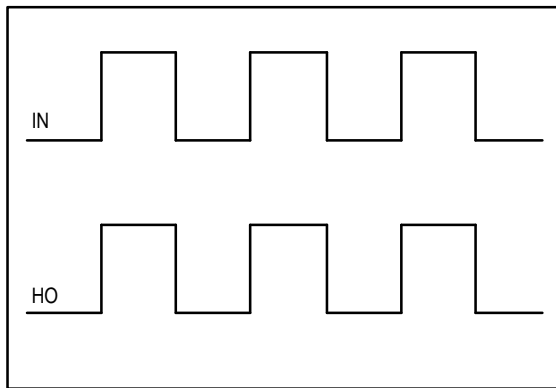


Figure 1. Input / Output Timing Diagram

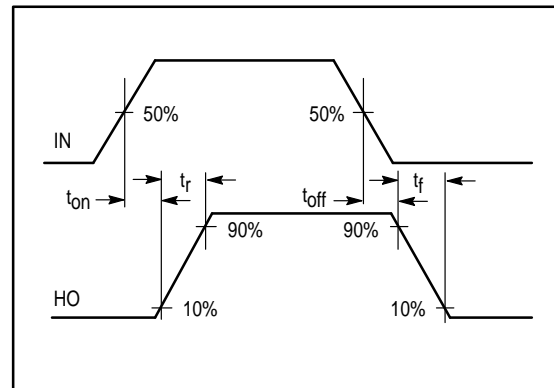
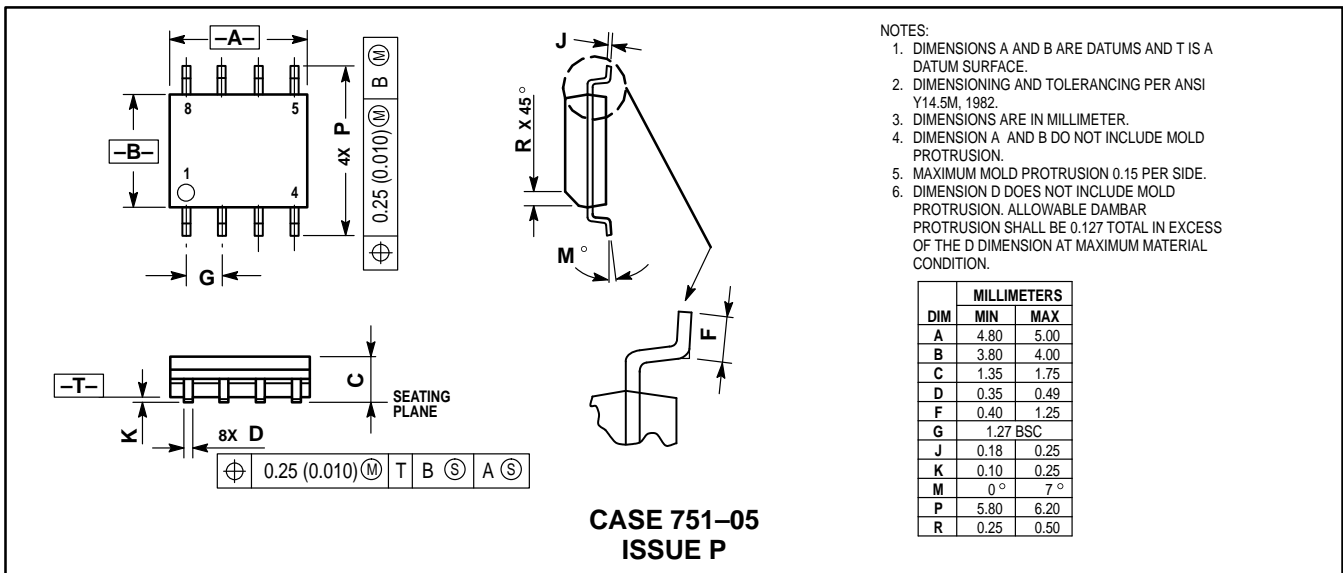
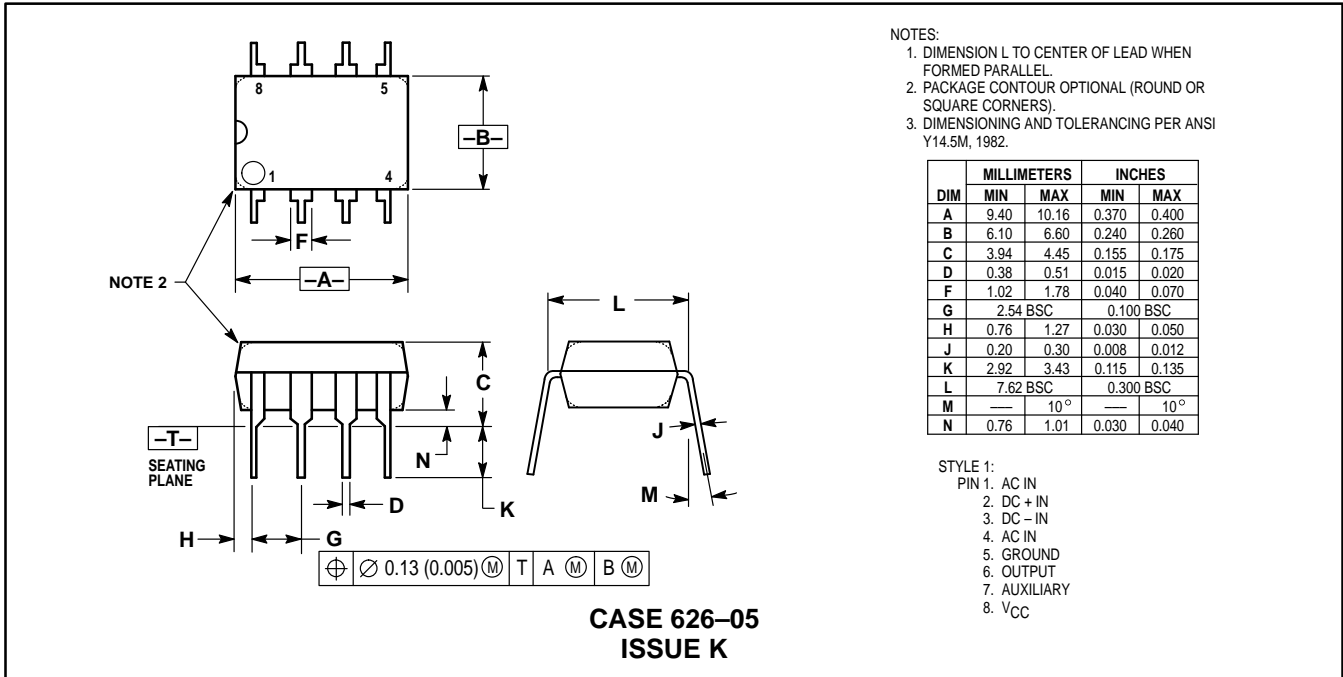


Figure 2. Switching Time Waveform Definitions


PACKAGE DIMENSIONS



- NOTES:
1. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
 2. PACKAGE CONTOUR OPTIONAL (ROUND OR SQUARE CORNERS).
 3. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.

- NOTES:
1. DIMENSIONS A AND B ARE DATUMS AND T IS A DATUM SURFACE.
 2. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 3. DIMENSIONS ARE IN MILLIMETER.
 4. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
 5. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
 6. DIMENSION D DOES NOT INCLUDE MOLD PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

MPIC2117

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