Power Products Division

Advance Information

3-PHASE BRIDGE DRIVER

MPIC2130

3–PHASE BRIDGE DRIVER

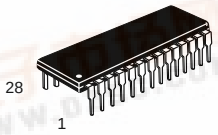
The MPIC2130 is a high voltage, high speed, power MOSFET and IGBT driver with three independent high side and low side referenced output channels for 3–Phase applications. Proprietary HVIC technology enables ruggedized monolithic construction. Logic inputs are compatible with 5 V CMOS or LSTTL outputs. A ground referenced operational amplifier provides an analog feedback of bridge current via an external current sense resistor. A current trip function which terminates all six outputs is also derived from this resistor. An open drain FAULT signal is provided to indicate that an over–current or undervoltage shutdown has occurred. The output drivers feature a high pulse current buffer stage designed for minimum driver cross–conduction. Propagation delays are matched to simplify use in high frequency applications.

The floating channels can be used to drive N–channel power MOSFET or IGBT's in the high side configuration which operate from 10 to 600 volts.

- Floating Channel Designed for Bootstrap Operation
- Fully Operational to +600 V
- Tolerant to Negative Transient Voltage
- dV/dt Immune
- Gate Drive Supply Range from 10 to 20 V
- Undervoltage Lockout for All Channels
- Over–current Shut Down Turns Off All Six Drivers
- Independent Half–bridge Drivers
- Matched Propagation Delay for All Channels
- Outputs Out of Phase with Inputs

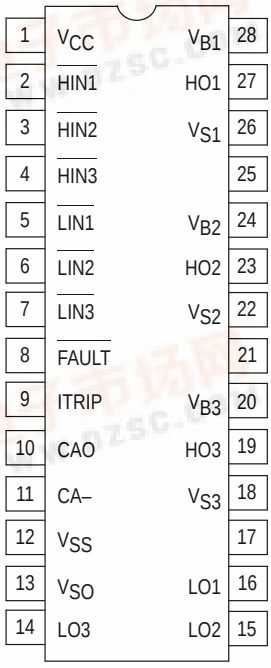
PRODUCT SUMMARY

V_{OFFSET}	600 V MAX
$I_{O+/-}$	200 mA/420 mA
V_{OUT}	10 – 20 V
$t_{on/off}$ (typical)	675 & 425 ns
Deadtime (typical)	2.5 µs



P SUFFIX
PLASTIC PACKAGE
CASE 710–02

PIN CONNECTIONS



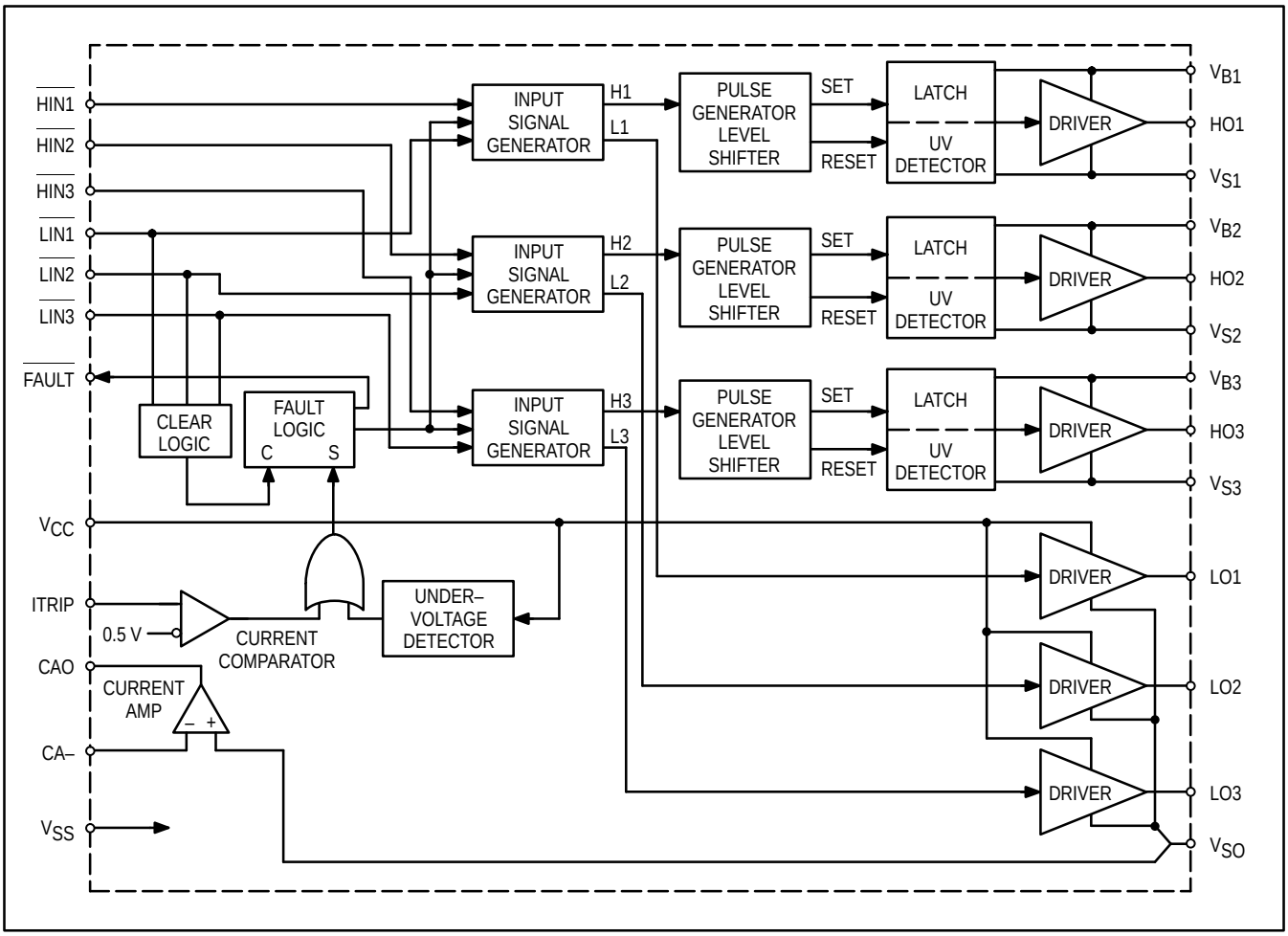
(TOP VIEW)

ORDERING INFORMATION

Device	Package
MPIC2130P	PDIP

This document contains information on a new product. Specifications and information herein are subject to change without notice.

SIMPLIFIED BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Absolute Maximum Ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to V_{SS}. The Thermal Resistance and Power Dissipation ratings are measured under board mounted and still air conditions.

Rating	Symbol	Min	Max	Unit
High Side Floating Absolute Voltage	$V_{B1,2,3}$	–0.3	625	V_{DC}
High Side Floating Supply Offset Voltage	$V_{S1,2,3}$	$V_{B1,2,3}$–25	$V_{B1,2,3}$+0.3	
High Side Floating Output Voltage	$V_{HO1,2,3}$	$V_{S1,2,3}$–0.3	$V_{B1,2,3}$+0.3	
Fixed Supply Voltage	V_{CC}	–0.3	25	
Low Side Driver Return	V_{SO}	V_{CC}–0.3	V_{CC}+0.3	
Low Side Output Voltage	$V_{LO1,2,3}$	V_{SO}–0.3	V_{CC}+0.3	
Logic Input Voltage (HIN–, LIN–, & ITRIP)	V_{IN}	–0.3	V_{CC}+0.3	
Fault Output Voltage	FAULT–	–0.3	V_{CC}+0.3	
Amplifier Output Voltage	CAO	–0.3	V_{CC}+0.3	
Amplifier Inverting Input Voltage	CA–	–0.3	V_{CC}+0.3	
Allowable Offset Supply Voltage Transient	dV_S/dt	–	50	V/ns
*Package Power Dissipation @ $T_A \leq +25°C$	P_D	–	1.5	Watt
Operating and Storage Temperature	T_j, T_{stg}	–55	150	°C
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	–	83	°C/W
Lead Temperature for Soldering Purposes, 10 seconds	T_L	–	260	°C

RECOMMENDED OPERATING CONDITIONS

The Input/Output logic timing Diagram is shown in Figure 1. For proper operation the device should be used within the recommended conditions. The V_S offset rating is tested with all supplies biased at 15 V differential.

High Side Floating Supply Absolute Voltage	$V_{B1,2,3}$	$V_{S1,2,3}$+10	$V_{S1,2,3}$+20	V
High Side Floating Supply Offset Voltage	$V_{S1,2,3}$	Note 1	V_{SO}+600	V
High Side Floating Output Voltage	$V_{HO1,2,3}$	$V_{S1,2,3}$	$V_{B1,2,3}$	V
Fixed Supply Voltage	V_{CC}	10	20	V
Low Side Driver Return	V_{SO}	–5	5	V
Low Side Output Voltage	$V_{LO1,2,3}$	V_{SO}	V_{CC}	V
Logic Input Voltage (HIN–, LIN–, & ITRIP)	V_{IN}	V_{SS}	5	V
Fault Output Voltage	FAULT–	V_{SS}	V_{CC}	V
Amplifier Output Voltage	CAO	V_{SS}	5	V
Amplifier Inverting Input Voltage	CA–	V_{SS}	5	V
Ambient Temperature	T_A	–40	125	°C

Note 1: Logic operational for V_S of –5 V to +600 V. Logic state held for V_S of V_{SO}–5 V to V_{SO}–V_{BS}.

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise specified)

Characteristic	Symbol	Min	Typ	Max	Unit
STATIC ELECTRICAL CHARACTERISTICS					
V_{BIAS} (V_{CC}, $V_{BS1,2,3}$) = 15 V and V_{SO} = V_{SS} unless otherwise specified. The V_{IN}, V_{TH} and I_{IN} parameters are referenced to V_{SS} and are applicable to all six channels (HS1,2,3 & LS1,2,3). The VO and IO parameters are referenced to $V_{SO1,2,3}$ and are applicable to the respective output leads: HO1,2,3 or LO1,2,3.					
Logic “0” Input Voltage (OUT = LO)	V_{IH}	2.2	–	–	V
Logic “1” Input Voltage (OUT = HI)	V_{IL}	–	–	0.8	V
ITRIP Input Positive Going Threshold	$V_{IT,TH+}$	400	–	580	mV
High Level Output Voltage, V_{BIAS}–V_O @ V_{IN} = 0 V, I_O = 0 A	V_{OH}	–	–	100	mV
Low Level Output Voltage, V_O @ V_{IN} = 5 V, I_O = 0 A	V_{OL}	–	–	100	mV
Offset Supply Leakage Current @ $V_{B1,2,3}$ = $V_{S1,2,3}$ = 600 V	I_{LK}	–	–	50	µA
Quiescent V_{BS} Supply Current @ V_{IN} = 0 V or 5 V	I_{QBS}	–	15	30	µA
Quiescent V_{CC} Supply Current @ V_{IN} = 0 V or 5 V	I_{QCC}	–	3.0	4.0	mA
Logic “1” Input Bias Current (OUT = HI) @ V_{IN} = 0 V	I_{IN+}	–	400	500	µA
Logic “0” Input Bias Current (OUT = LO) @ V_{IN} = 5 V	$I_{IN–}$	–	200	320	µA
“High” ITRIP Bias Current @ ITRIP = 5 V	I_{TRIP+}	–	75	150	µA
“Low” ITRIP Bias Current @ ITRIP = 0 V	$I_{TRIP–}$	–	–	100	nA
V_{BS} Supply Undervoltage Positive Going Threshold	V_{BSUV+}	8.0	–	9.2	V
V_{BS} Supply Undervoltage Negative Going Threshold	$V_{BSUV–}$	7.6	–	8.8	V
V_{CC} Supply Undervoltage Positive Going Threshold	V_{CCUV+}	8.3	–	9.7	V
V_{CC} Supply Undervoltage Negative Going Threshold	$V_{CCUV–}$	8.0	–	9.4	V
FAULT – Low On Resistance	$R_{on,FLT}$	–	55	75	Ω
Output High Short Circuit Pulsed Current @ V_{out} = 0 V, V_{in} = 0 V, PW ≤ 10 µs	I_{O+}	200	250	–	mA
Output Low Short Circuit Pulsed Current @ V_{out} = 15 V, V_{in} = 5 V, PW ≤ 10 µs	$I_{O–}$	420	500	–	mA
Amplifier Input Offset Voltage @ V_{SO} = CA– = 0.2	V_{OS}	–	–	30	mV
CA– Input Bias Current @ CA– = 2.5 V	$I_{CA–}$	–	–	4.0	nA
Amplifier Common Mode Rejection Ratio @ V_{SO} = CA– = 0.1 V & 5 V	CMRR	60	80	–	dB

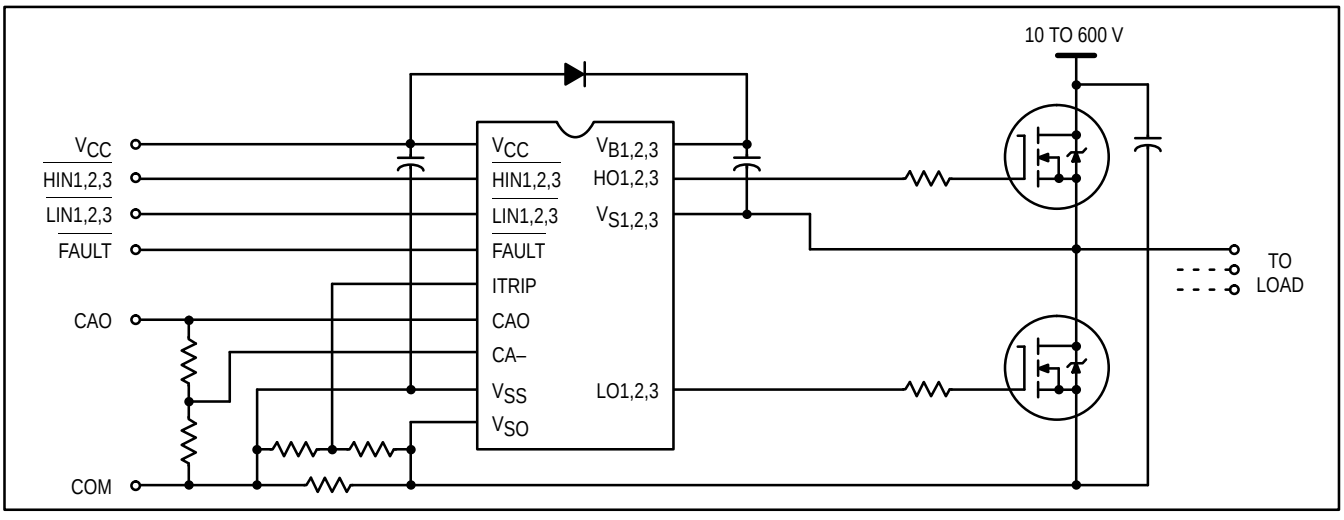
ELECTRICAL CHARACTERISTICS (continued) (T_A = 25°C unless otherwise specified)

Characteristic	Symbol	Min	Typ	Max	Unit
STATIC ELECTRICAL CHARACTERISTICS V_{BIAS} (V_{CC}, $V_{BS1,2,3}$) = 15 V and V_{SO} = V_{SS} unless otherwise specified. The V_{IN}, V_{TH} and I_{IN} parameters are referenced to V_{SS} and are applicable to all six channels (HS1,2,3 & LS1,2,3). The VO and IO parameters are referenced to $V_{SO1,2,3}$ and are applicable to the respective output leads: HO1,2,3 or LO1,2,3.					
Amplifier Power Supply Rejection Ratio @ V_{SO} = CA–=0.2 V, V_{CC} = 10 & 20 V	PSRR	55	75	–	dB
Amplifier High Level Output Voltage @ CA– = 0 V, V_{SO} = 1 V	$V_{OH,Amp}$	5.0	–	5.4	V
Amplifier Low Level Output Voltage @ CA– = 1 V, V_{SO} = 0 V	$V_{OL,Amp}$	–	–	20	mV
Amplifier Output Source Current @ CA– = 0 V, V_{SO} = 1 V, CAO = 4 V	$I_{SRC,Amp}$	2.3	4.0	–	mA
Amplifier Output Sink Current @ CA– = 1 V, V_{SO} = 0 V, CAO = 2 V	$I_{SNK,Amp}$	1.0	2.1	–	mA
Amplifier Output High Short Circuit Current @ CA– = 1 V, V_{SO} = 5 V, CAO = 0 V	$I_{O+,Amp}$	–	4.5	6.5	mA
Amplifier Output Low Short Circuit Current @ CA– = 5 V, V_{SO} = 0 V, CAO = 5 V	$I_{O–,Amp}$	–	3.2	5.2	mA

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise specified)

Characteristic	Symbol	Min	Typ	Max	Unit
DYNAMIC ELECTRICAL CHARACTERISTICS V_{BIAS} (V_{CC}, $V_{BS1,2,3}$) = 15 V, $V_{SO1,2,3}$ = V_{SS} and C_L = 1000 pF unless otherwise specified. T_A = 25°C.					
Turn–On Propagation Delay @ V_{IN} = 0 & 5 V, $V_{S1,2,3}$ = 0 V to 600 V	t_{on}	500	–	850	ns
Turn–Off Propagation Delay @ V_{IN} = 0 & 5 V, $V_{S1,2,3}$ = 0 V to 600 V	t_{off}	300	–	550	ns
Turn–On Rise Time @ V_{IN} = 0 & 5 V, $V_{S1,2,3}$ = 0 V to 600 V	t_r	–	80	125	ns
Turn–Off Fall Time @ V_{IN} = 0 & 5 V, $V_{S1,2,3}$ = 0 V to 600 V	t_f	–	35	55	ns
ITRIP to Output Shutdown Propagation Delay @ V_{IN}, V_{ITRIP} = 0 & 5 V	t_{itrip}	400	–	920	ns
ITRIP Blanking Time @ ITRIP = 1 V	t_{bl}	–	400	–	ns
ITRIP to FAULT– Propagation Delay @ V_{IN}, V_{ITRIP} = 0 & 5 V	t_{flt}	335	–	845	ns
Input Filter Time (all six inputs) @ V_{IN} = 0 & 5 V	$t_{flt,in}$	–	310	–	ns
LIN1,2,3 to FAULT Clear Time @ V_{IN}, V_{ITRIP} = 0 & 5 V	t_{fltclr}	6.0	–	12	µs
Deadtime, LS Turn–Off to HS Turn–On & HS Turn–Off to LS Turn–On @ V_{IN} = 0 & 5 V	DT	1.3	–	3.7	µs
Amplifier Slew Rate (Positive)	SR+	4.4	6.2	–	V/µs
Amplifier Slew Rate (Negative)	SR–	2.4	3.2	–	V/µs

TYPICAL CONNECTION



LEAD DEFINITIONS

Symbol	Lead Description
HIN1,2,3	Logic Inputs for High Side Gate Driver Outputs (HO1,2,3), Out of Phase
LIN1,2,3	Logic Inputs for Low Side Gate Driver Outputs (LO1,2,3), Out of Phase
FAULT–	Indicates Over–current, or Undervoltage Lockout (Low Side) has Occurent, Negative Logic
V_{CC}	Logic and Low Side Fixed Supply
ITRIP	Input for Over–current Shut Down
CAO	Output of Current Amplifier
CA–	Negative Input of Current Amplifier
V_{SS}	Logic Ground
$V_{B1,2,3}$	High Side Floating Supplies
HO1,2,3	High Side Gate Drive Outputs
$V_{S1,2,3}$	High Side Floating Supply Returns
LO1,2,3	Low Side Gate Drive Outputs
V_{SO}	Low Side Return, Positive Input of Current Amplifier

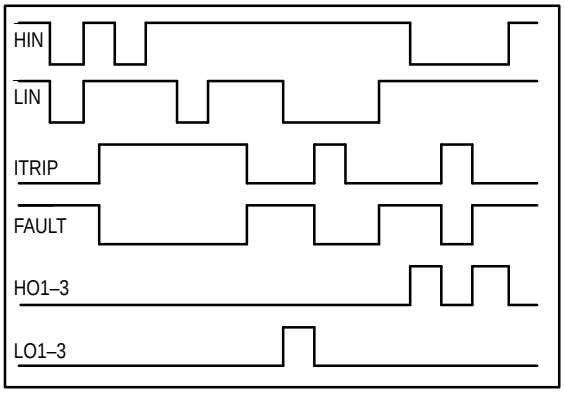


Figure 1. Input / Output Timing Diagram

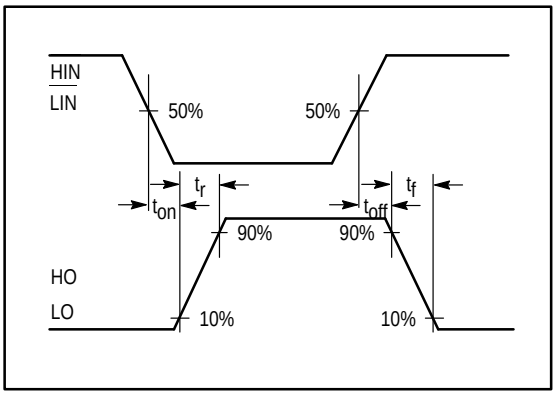


Figure 2. Switching Time Waveform Definitions

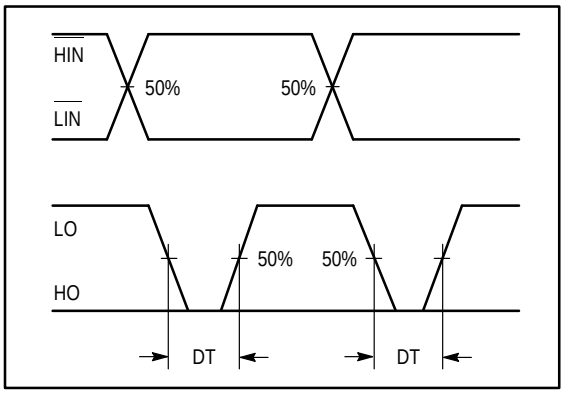


Figure 3. Deadtime Waveform Definitions

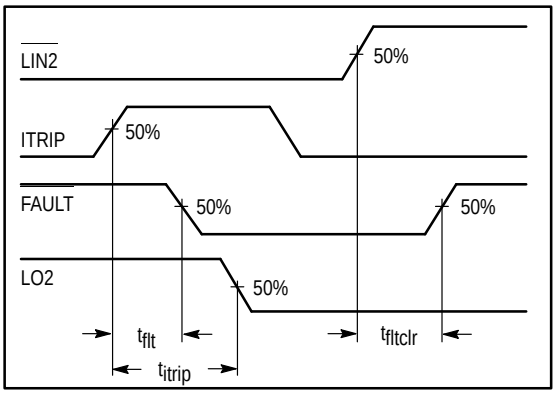
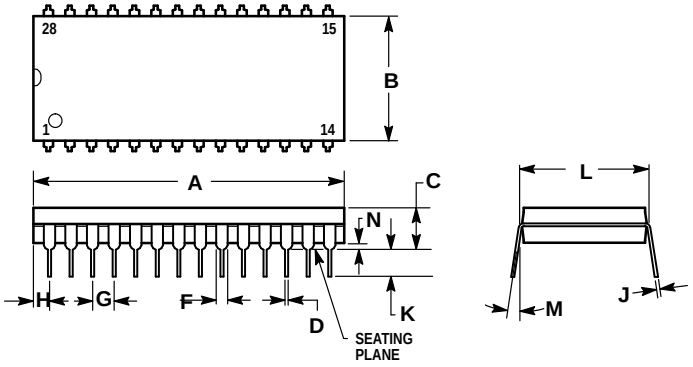


Figure 4. Overcurrent Shutdown Waveform Definitions

PACKAGE DIMENSIONS



NOTES:
1. POSITIONAL TOLERANCE OF LEADS (D), SHALL BE WITHIN 0.25 (0.010) AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	36.45	37.21	1.435	1.465
B	13.72	14.22	0.540	0.560
C	3.94	5.08	0.155	0.200
D	0.36	0.56	0.014	0.022
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.65	2.16	0.065	0.085
J	0.20	0.38	0.008	0.015
K	2.92	3.43	0.115	0.135
L	15.24 BSC		0.600 BSC	
M	0°	15°	0°	15°
N	0.51	1.02	0.020	0.040

CASE 710–02
ISSUE B

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