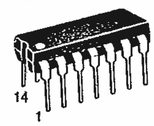
T-43-25

MPQ2906, 2907

For Specifications, See MHQ2906 Data.

MPQ3303

CASE 646-06, STYLE 1
TO-116



QUAD
SWITCHING TRANSISTOR

NPN SILICON

5

MAXIMUM RATINGS

Rating	Symbol	Value		Unit
Collector-Emitter Voltage	V_{CEO}	12		Vdc
Collector-Base Voltage	V_{CBO}	25		Vdc
Emitter-Base Voltage	V_{EBO}	4.0		Vdc
Collector Current — Continuous	I_C	1.0		Adc
		Each Transistor	Four Transistors Equal Power	
Total Device Dissipation @ $T_A = 25°C$ Derate above 25°C	P_D	650 5.2	1250 10	mW mW/°C
Total Device Dissipation @ $T_C = 25°C$ Derate above 25°C	P_D'	1.0 8.0	3.0 24	Watts mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−55 to +150		°C

THERMAL CHARACTERISTICS

Characteristic		Junction to Case	Junction to Ambient	Unit
Thermal Resistance	Each Die Effective, 4 Die	125 41.6	193* 100*	°C/W °C/W
Coupling Factors	Q1-Q4 or Q2-Q3 Q1-Q2 or Q3-Q4	30 2.0	60 25	% %

(1) $R_{\theta JA}$ is measured with the device soldered into a typical printed circuit board.

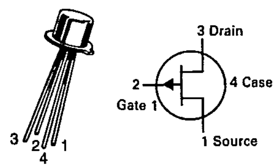
ELECTRICAL CHARACTERISTICS ($T_A = 25°C$ unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage ($I_C = 10$ mAdc, $I_B = 0$)	$V_{(BR)CEO}$	12	—	—	Vdc
Collector-Base Breakdown Voltage ($I_C = 100$ μAdc, $I_E = 0$)	$V_{(BR)CBO}$	25	—	—	Vdc
Emitter-Base Breakdown Voltage ($I_E = 100$ μAdc, $I_C = 0$)	$V_{(BR)EBO}$	4.0	—	—	Vdc
Collector Cutoff Current ($V_{CE} = 15$ Vdc, $V_{BE} = 0$)	I_{CES}	—	—	100	μAdc
ON CHARACTERISTICS					
DC Current Gain ($I_C = 100$ mAdc, $V_{CE} = 0.5$ Vdc) ($I_C = 300$ mAdc, $V_{CE} = 0.5$ Vdc)	h_{FE}	 30 40	 45 55	 — 200	—
Collector-Emitter Saturation Voltage ($I_C = 300$ mAdc, $I_B = 30$ mAdc) ($I_C = 1.0$ Adc, $I_B = 0.1$ Adc)	$V_{CE(sat)}$	 — —	 0.22 0.52	 0.33 0.7	Vdc
Base-Emitter Saturation Voltage ($I_C = 300$ mAdc, $I_B = 30$ mAdc) ($I_C = 1.0$ Adc, $I_B = 0.1$ Adc)	$V_{BE(sat)}$	 — —	 0.87 1.04	 1.1 1.4	Vdc
SMALL-SIGNAL CHARACTERISTICS					
Current-Gain — Bandwidth Product ($I_C = 100$ mAdc, $V_{CE} = 5.0$ Vdc, f = 100 MHz)	f_T	400	500	—	MHz
Output Capacitance ($V_{CB} = 5.0$ Vdc, $I_E = 0$, f = 1 MHz)	C_{obo}	—	5.0	10	pF
Input Capacitance ($V_{BE} = 0.5$ Vdc, $I_C = 0$, f = 1 MHz)	C_{ibo}	—	22	30	pF
SWITCHING CHARACTERISTICS					
Turn-On Time ($V_{CC} = 12$ Vdc, $I_C = 1.0$ Adc, $V_{BE(off)} = 4.0$ Vdc, $I_{B1} = 100$ mAdc)	t_{on}	—	12	15	ns
Turn-Off Time ($V_{CC} = 12$ Vdc, $I_C = 1.0$ Adc, $I_{B1} = I_{B2} = 100$ mAdc)	t_{off}	—	18	25	ns

T-35-25

2N3993,A
2N3994

CASE 20-03, STYLE 5
TO-72 (TO-206AF)



JFET
SWITCHING

P-CHANNEL — DEPLETION

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DS}	−25	Vdc
Drain-Gate Voltage	V_{DG}	−25	Vdc
Reverse Gate-Source Voltage	V_{GSR}	25	Vdc
Forward Gate Current	I_{GF}	10	mAdc
Total Device Dissipation @ T_A = 25°C Derate above 25°C	P_D	300 2.0	mW mW/°C
Storage Temperature Range	T_{stg}	−65 to +200	°C

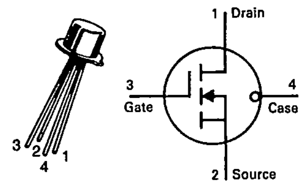
ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted.)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Gate-Source Breakdown Voltage (I_G = 1.0 μAdc, V_{DS} = 0)		$V_{(BR)GSS}$	25	—	Vdc
Drain Reverse Current (V_{DG} = −15 Vdc, I_S = 0) (V_{DG} = −15 Vdc, I_S = 0, T_A = 150°C)		I_{DGO}	— —	1.2 1.2	nAdc μAdc
Drain Cutoff Current (V_{DS} = −10 Vdc, V_{GS} = 10 Vdc) (V_{DS} = −10 Vdc, V_{GS} = 6.0 Vdc) (V_{DS} = −10 Vdc, V_{GS} = 10 Vdc, T_A = 150°) (V_{DS} = −10 Vdc, V_{GS} = 6.0 Vdc, T_A = 150°)	2N3993, 2N3993A 2N3994 2N3993, 2N3993A 2N3994	$I_{D(off)}$	— — — —	1.2 1.2 1.0 1.0	nAdc μAdc
Gate Source Voltage (V_{DS} = −10 Vdc, I_D = −1.0 μAdc)	2N3993, 2N3993A 2N3994	V_{GS}	4.0 1.0	9.5 5.5	Vdc
ON CHARACTERISTICS					
Zero-Gate-Voltage Drain Current(1) (V_{DS} = −10 Vdc, V_{GS} = 0)	2N3993, 2N3993A 2N3994	I_{DSS}	10 2.0	— —	mAdc
SMALL-SIGNAL CHARACTERISTICS					
Drain-Source "ON" Resistance (V_{GS} = 0, I_D = 0, f = 1.0 kHz)	2N3993, 2N3993A 2N3994	$r_{ds(on)}$	— —	150 300	Ohms
Forward Transfer Admittance(1) (V_{DS} = −10 Vdc, V_{GS} = 0, f = 1.0 kHz)	2N3993 2N3993A 2N3994	$\|y_{fs}\|$	6.0 7.0 4.0	12 12 10	mmhos
Input Capacitance (V_{DS} = −10 Vdc, V_{GS} = 0, f = 1.0 MHz)	2N3993, 2N3994 2N3993A	C_{iss}	— —	16 12	pF
Reverse Transfer Capacitance (V_{DS} = 0, V_{GS} = 10 Vdc, f = 1.0 MHz) (V_{DS} = 0, V_{GS} = 6.0 Vdc, f = 1.0 MHz)	2N3993 2N3993A 2N3994	C_{rss}	— — —	4.5 3.0 5.0	pF

(1) Pulse Test: Pulse Width = 100 ms, Duty Cycle ≤ 10%.

3N157
3N158

CASE 20-03, STYLE 2
TO-72 (TO-206AF)



MOSFET
AMPLIFIER AND SWITCHING

P-CHANNEL — ENHANCEMENT

6

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-Source Voltage*	V_{DS}	±35	Vdc
Drain-Gate Voltage*	V_{DG}	±50	Vdc
Gate-Source Voltage*	V_{GS}	±50	Vdc
Drain Current*	I_D	30	mAdc
Total Device Dissipation @ T_A = 25°C Derate above 25°C*	P_D	300 1.7	mW mW/°C
Junction Temperature Range*	T_J	−65 to +175	°C
Storage Channel Temperature Range*	T_{stg}	−65 to +175	°C

*JEDEC Registered Limits

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Drain-Source Breakdown Voltage (I_D = −10 μAdc, V_G = V_S = 0)	$V_{(BR)DSX}$	−35	—	—	Vdc
Zero-Gate-Voltage Drain Current (V_{DS} = −15 Vdc, V_{GS} = 0) (V_{DS} = −35 Vdc, V_{GS} = 0)	I_{DSS}	— —	— —	−1.0 −10	nAdc μAdc
Gate Reverse Current* (V_{GS} = +25 Vdc, V_{DS} = 0) (V_{GS} = +50 Vdc, V_{DS} = 0)	I_{GSS}	— —	— —	+10 +10	pAdc nAdc
Input Resistance (V_{GS} = −25 Vdc)	R_{GS}	—	1 x 10^{+12}	—	Ohms
Gate Source Voltage* (V_{DS} = −15 Vdc, I_D = −0.5 mAdc) 3N157 3N158	V_{GS}	 −1.5 −3.0	 — —	 −5.5 −7.0	Vdc
Gate Forward Current* (V_{GS} = −25 Vdc, V_{DS} = 0) (V_{GS} = −50 Vdc, V_{DS} = 0) (V_{GS} = −25 Vdc, V_{DS} = 0, T_A = +55°C) (V_{GS} = −50 Vdc, V_{DS} = 0, T_A = +55°C)	$I_{G(f)}$	— — — —	— — — —	−10 −1.0 −10 −1.0	pAdc nAdc nAdc μAdc
ON CHARACTERISTICS					
Gate Threshold Voltage* (V_{DS} = −15 Vdc, I_D = −10 μAdc) 3N157 3N158	$V_{GS(Th)}$	 −1.5 −3.0	 — —	 −3.2 −5.0	Vdc
On-State Drain Current* (V_{DS} = −15 Vdc, V_{GS} = −10 Vdc)	$I_{D(on)}$	−5.0	—	—	mAdc
SMALL-SIGNAL CHARACTERISTICS					
Forward Transfer Admittance* (V_{DS} = −15 Vdc, I_D = −2.0 mAdc, f = 1.0 kHz)	$\|y_{fs}\|$	1000	—	4000	μmhos
Output Admittance* (V_{DS} = −15 Vdc, I_D = −2.0 mAdc, f = 1.0 kHz)	$\|y_{os}\|$	—	—	60	μmhos
Input Capacitance* (V_{DS} = −15 Vdc, V_{GS} = 0, f = 140 kHz)	C_{iss}	—	—	5.0	pF
Reverse Transfer Capacitance* (V_{DS} = −15 Vdc, V_{GS} = 0, f = 140 kHz)	C_{rss}	—	—	1.3	pF
Drain-Substrate Capacitance ($V_{D(SUB)}$ = −10 Vdc, f = 140 kHz)	$C_{d(sub)}$	—	—	4.0	pF
Noise Voltage (R_S = 0, BW = 1.0 Hz, V_{DS} = −15 Vdc, I_D = −2.0 mAdc, f = 100 Hz) (R_S = 0, BW = 1.0 Hz, V_{DS} = −15 Vdc, I_D = −2.0 mAdc, f = 1.0 kHz)	e_n	 — —	 300 120	 — 500	NV/√Hz

*JEDEC Registered Limits

FIGURE 1 – FORWARD TRANSCONDUCTANCE

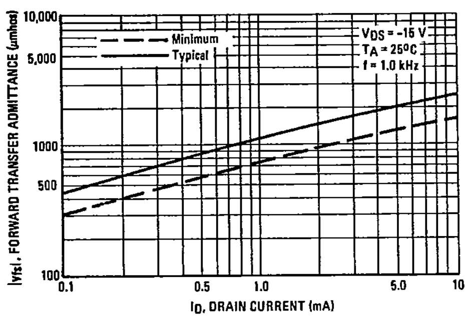


FIGURE 2 – OUTPUT TRANSCONDUCTANCE

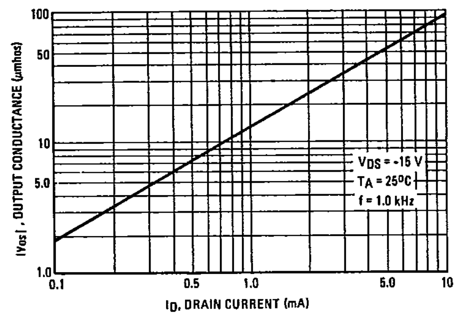


FIGURE 3 – FORWARD TRANSCONDUCTANCE versus TEMPERATURE

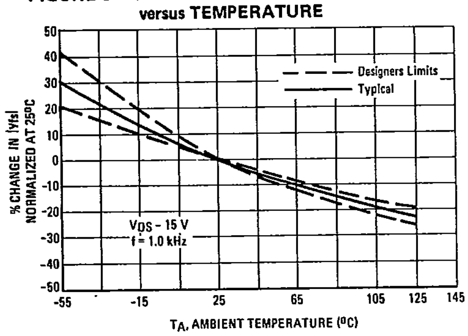


FIGURE 4 – BIAS CURVE

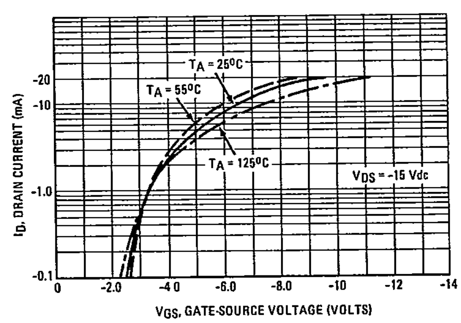


FIGURE 5 – "ON" DRAIN-SOURCE VOLTAGE

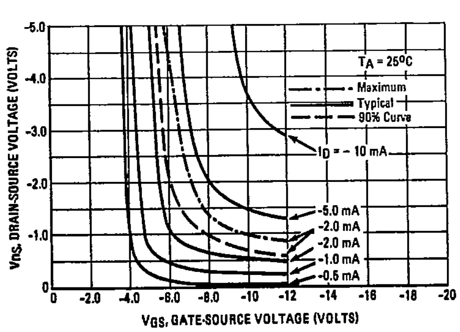
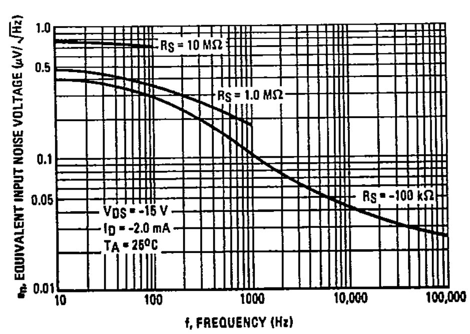


FIGURE 6 – EQUIVALENT INPUT NOISE VOLTAGE



T-37-25

SWITCHING CHARACTERISTICS

($T_A = 25^oC$)

FIGURE 7 – TURN-ON DELAY TIME

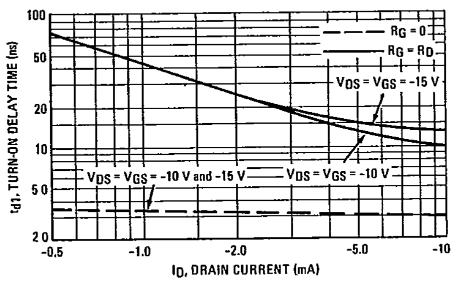


FIGURE 8 – RISE TIME

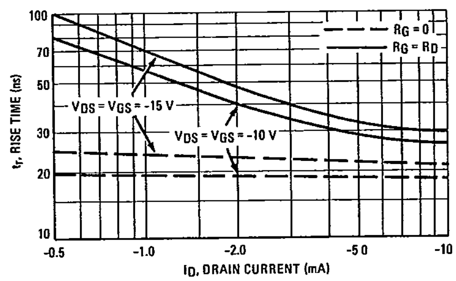


FIGURE 9 – TURN-OFF DELAY TIME

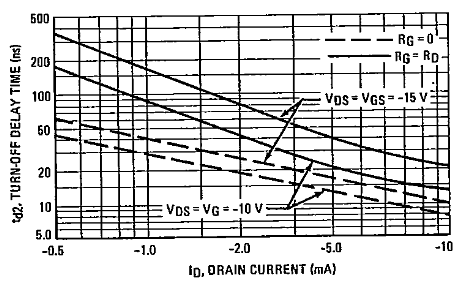


FIGURE 10 – FALL TIME

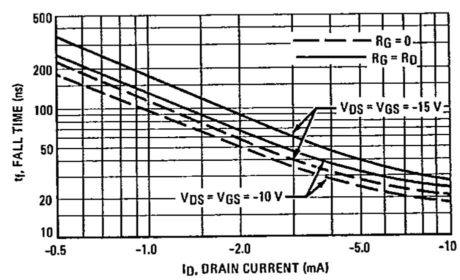


FIGURE 11 – SWITCHING CIRCUIT and WAVEFORMS

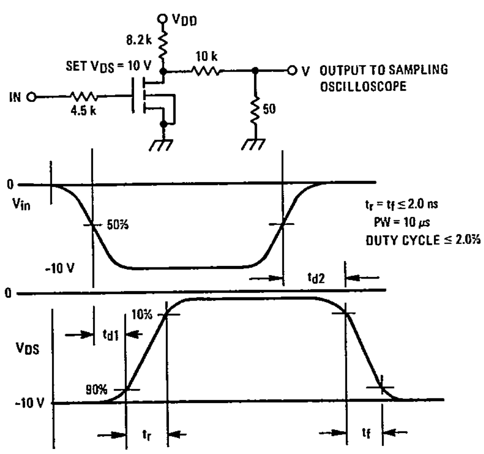
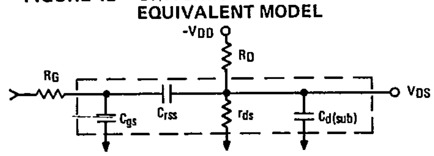


FIGURE 12 – SWITCHING CIRCUIT with MOSFET EQUIVALENT MODEL



The switching characteristics shown above were measured in a test circuit similar to Figure 11. At the beginning of the switching interval, the gate voltage is at ground and the gate source capacitance (C_{gs} • C_{rss} • C_{rss}) has no charge. The drain voltage is at V_{DD} and thus the feedback capacitance (C_{rss}) is charged to V_{DD}. Similarly, the drain substrate capacitance ($C_{d(sub)}$) is charged to V_{DD} since the substrate and source are connected to ground.

During the turn-on interval C_{gs} is charged to V_{GS} (the input voltage) through R_G (generator impedance) (Figure 12). C_{rss} must be discharged to V_{GS} • $V_{D(on)}$ through R_G and the parallel combination of the load resistor (R_D) and the channel resistance (r_{ds}). In addition, $C_{d(sub)}$ is discharged to a low value ($V_{D(on)}$) through R_D in parallel with r_{ds}. During turn-off this charge flow is reversed.

Predicting turn-on time proves to be somewhat difficult since the channel resistance (r_{ds}) is a function of the gate source voltage (V_{GS}). As C_{gs} becomes charged V_{GS} is approaching V_{in} and r_{ds} decreases (see Figure 5) and since C_{rss} and $C_{d(sub)}$ are charged through r_{ds}, turn-on time is quite non-linear.

If the charging time of C_{gs} is short compared to that of C_{rss} and $C_{d(sub)}$, then r_{ds} (which is in parallel with R_D) will be low compared to R_D during the switching interval and will largely determine the turn-on time. On the other hand, during turn-off r_{ds} will be almost an open circuit requiring C_{rss} and $C_{d(sub)}$ to be charged through R_D and resulting in a turn-off time that is long compared to the turn-on time. This is especially noticeable for the curves where R_G • 0 and C_{gs} is charged through the pulse generator impedance only.

The switching curves shown with R_G • R_D simulate the switching behavior of cascaded stages where the driving source impedance is normally the same as the load impedance. The set of curves with R_G • 0 simulates a low source impedance drive such as might occur in complementary logic circuits.

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