

# The RF MOSFET Line

## Power Field Effect Transistor

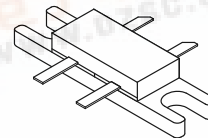
### N-Channel Enhancement-Mode MOSFET

Designed primarily for wideband large-signal output and driver stages to 500 MHz.

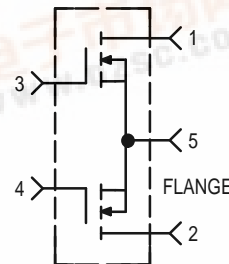
- Push-Pull Configuration Reduces Even Numbered Harmonics
- Typical Performance at 400 MHz, 28 Vdc
  - Output Power = 40 Watts
  - Gain = 13 dB
  - Efficiency = 50%
- Typical Performance at 175 MHz, 28 Vdc
  - Output Power = 40 Watts
  - Gain = 17 dB
  - Efficiency = 60%
- Excellent Thermal Stability, Ideally Suited for Class A Operation
- Facilitates Manual Gain Control, ALC and Modulation Techniques
- 100% Tested for Load Mismatch at All Phase Angles with 30:1 VSWR
- Low  $C_{RSS}$  — 4.5 pF @  $V_{DS} = 28$  Volts
- Circuit board photomaster available upon request by contacting RF Tactical Marketing in Phoenix, AZ.

**MRF166W**

**40 W, 500 MHz  
 TMOS BROADBAND  
 RF POWER FET**



**CASE 412-01, Style 1**



**MAXIMUM RATINGS** ( $T_J = 25^\circ\text{C}$  unless otherwise noted)

Rating	Symbol	Value	Unit
Drain-Gate Voltage	$V_{DSS}$	65	Vdc
Drain-Gate Voltage ( $R_{GS} = 1.0 \text{ M}\Omega$ )	$V_{DGR}$	65	Vdc
Gate-Source Voltage	$V_{GS}$	$\pm 40$	Adc
Drain Current — Continuous	$I_D$	8.0	ADC
Total Device Dissipation @ $T_C = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$	$P_D$	175 1.0	Watts $^\circ\text{C/W}$
Storage Temperature Range	$T_{stg}$	-65 to +150	$^\circ\text{C}$
Operating Junction Temperature	$T_J$	200	$^\circ\text{C}$

**THERMAL CHARACTERISTICS**

Thermal Resistance — Junction to Case	$R_{\theta JC}$	1.0	$^\circ\text{C/W}$
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NOTE: Handling and Packaging — MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.



**ELECTRICAL CHARACTERISTICS** ( $T_C = 25^\circ\text{C}$  unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
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**OFF CHARACTERISTICS (1)**

Drain–Source Breakdown Voltage ( $V_{GS} = 0\text{ Vdc}$ , $I_D = 5.0\text{ mA}$ )	$V_{(BR)DSS}$	65	—	—	Vdc
Zero Gate Voltage Drain Current ( $V_{DS} = 28\text{ Vdc}$ , $V_{GS} = 0\text{ Vdc}$ )	$I_{DSS}$	—	—	1.0	mA
Gate–Source Leakage Current ( $V_{GS} = 40\text{ Vdc}$ , $V_{DS} = 0\text{ Vdc}$ )	$I_{GSS}$	—	—	1.0	$\mu\text{A}$

**ON CHARACTERISTICS (1)**

Gate Threshold Voltage ( $V_{DS} = 10\text{ Vdc}$ , $I_D = 25\text{ mA}$ )	$V_{GS(th)}$	1.0	3.0	6.0	Vdc
Forward Transconductance ( $V_{DS} = 10\text{ Vdc}$ , $I_D = 1.5\text{ A}$ )	$g_{fs}$	600	800	—	mS

**DYNAMIC CHARACTERISTICS (1)**

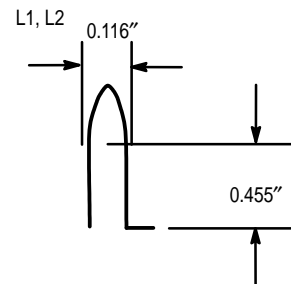
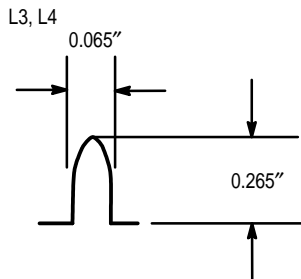
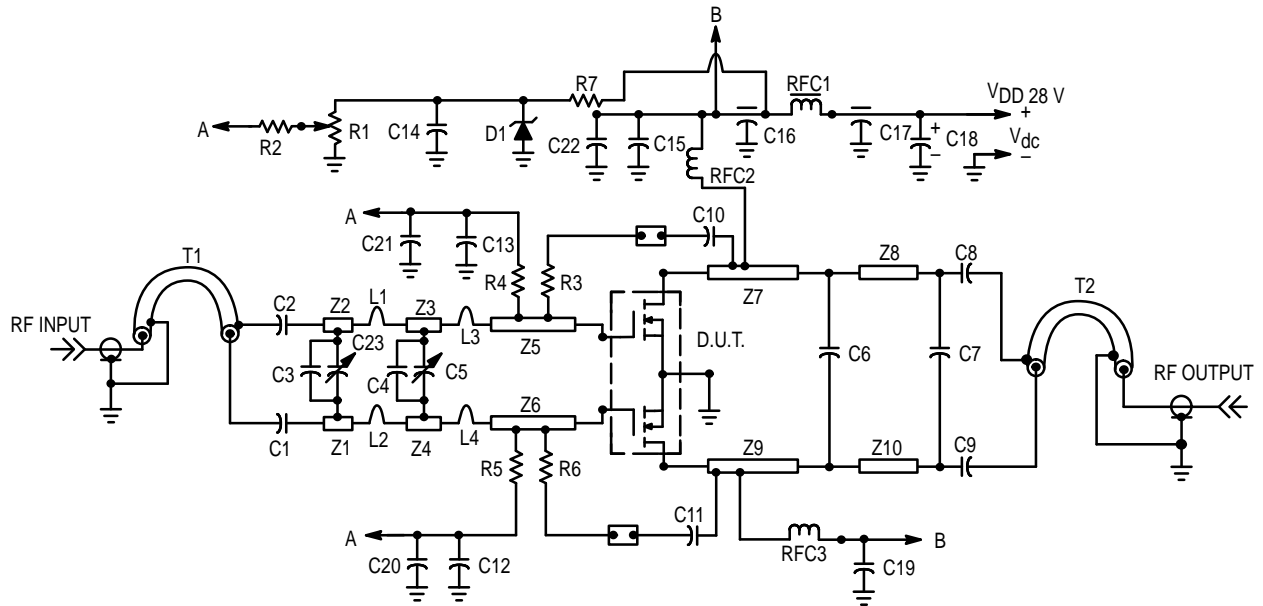
Input Capacitance ( $V_{DS} = 28\text{ Vdc}$ , $V_{GS} = 0\text{ Vdc}$ , $f = 1.0\text{ MHz}$ )	$C_{iss}$	—	30	—	pF
Output Capacitance ( $V_{DS} = 28\text{ Vdc}$ , $V_{GS} = 0\text{ Vdc}$ , $f = 1.0\text{ MHz}$ )	$C_{oss}$	—	35	—	pF
Reverse Transfer Capacitance ( $V_{DS} = 28\text{ Vdc}$ , $V_{GS} = 0\text{ Vdc}$ , $f = 1.0\text{ MHz}$ )	$C_{rss}$	—	4.5	—	pF

**FUNCTIONAL CHARACTERISTICS (2)**

Common Source Power Gain ( $V_{DD} = 28\text{ Vdc}$ , $P_{out} = 40\text{ W}$ , $f = 400\text{ MHz}$ , $I_{DG} = 100\text{ mA}$ )	$G_{ps}$	11	13	—	dB
Drain Efficiency ( $V_{DD} = 28\text{ Vdc}$ , $P_{out} = 40\text{ W}$ , $f = 400\text{ MHz}$ , $I_{DG} = 100\text{ mA}$ )	$\eta$	45	50	—	%
Electrical Ruggedness ( $V_{DD} = 28\text{ Vdc}$ , $P_{out} = 40\text{ W}$ , $f = 400\text{ MHz}$ , $I_{DG} = 100\text{ mA}$ ) Load VSWR = 30:1, All phase angles at frequency of test	$\Psi$	No Degradation in Output Power			

(1) Each transistor chip measured separately.

(2) Both transistor chips operating in a push–pull amplifier.



C1, C2, C8, C9,	270 pF, Chip Cap	RFC1	Ferroxcube VK-200-19/4B
C12, C13, C15		RFC2, RFC3	10T, ID = 1/4", 18 AWG
C3	5.6 pF, Chip Cap	R1	10 kΩ, 10T
C4	20 pF, Chip Cap	R2	9.2 kΩ, 1/2 W
C5	0 – 20 pF, Johanson*	R3, R6	330 Ω, 1.0 W
C6	8.2 pF, Chip Cap	R4 R5	520 Ω, 1/4 W
C7	15 pF, Chip Cap	R7	1.5 kΩ, 1/2 W
C10, C11, C14, C19,	0.01 μF	T1, T2	Balun 2.0", 50 Ω Semi-Rigid Coax
C20, C21, C22		Z1, Z2	0.120 x 0.467"
C16, C17	680 pF, Feedthru	Z3, Z4	0.120 x 0.55" *
C18	10 μF, 50 V	Z5, Z6	0.120 x 0.49"
C23	0 – 10 pF, Johanson*	Z7, Z9	0.120 x 0.85"
D1	IN5343 – Motorola Zener	Z8, Z10	0.120 x 0.6" for C6
L1, L2	Hair Pin Inductor #18 AWG, 0.065 W x 0.265 H		
L3, L4	Hair Pin Inductor #18 AWG, 0.116 W x 0.445 H		

\* C4, C5 Center of Z3 and Z4

Board Material – Teflon® Fiberglass

Dielectric Thickness = 0.030",  $\epsilon_r = 2.55$  Copper Clad, 2.0 oz. Copper

Figure 1. MRF166 400 MHz Test Circuit Schematic

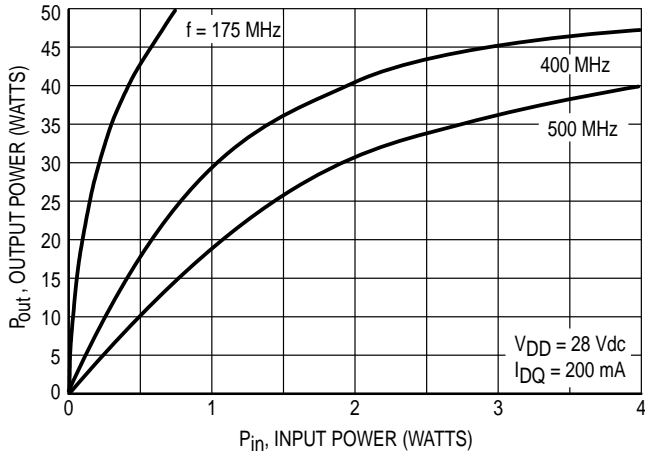


Figure 2. Output Power versus Input Power

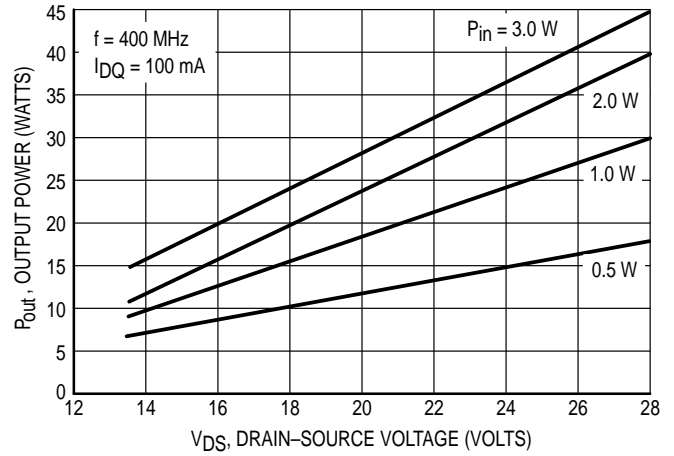


Figure 3. Output Power versus Voltage

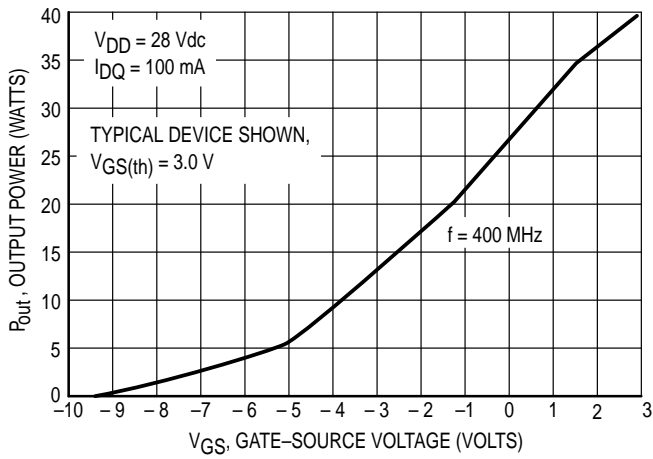


Figure 4. Output Power versus Gate Voltage

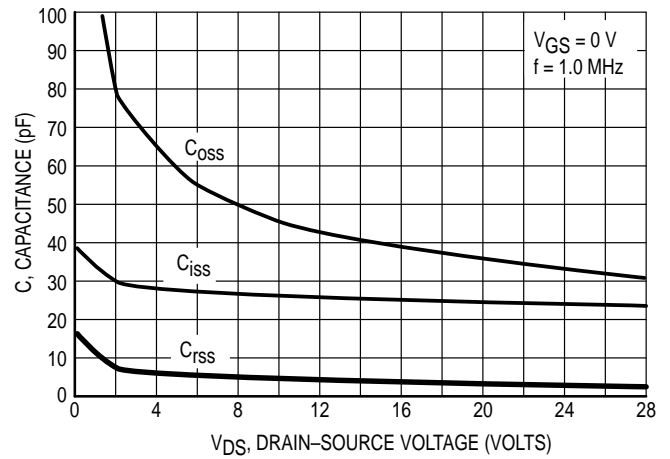
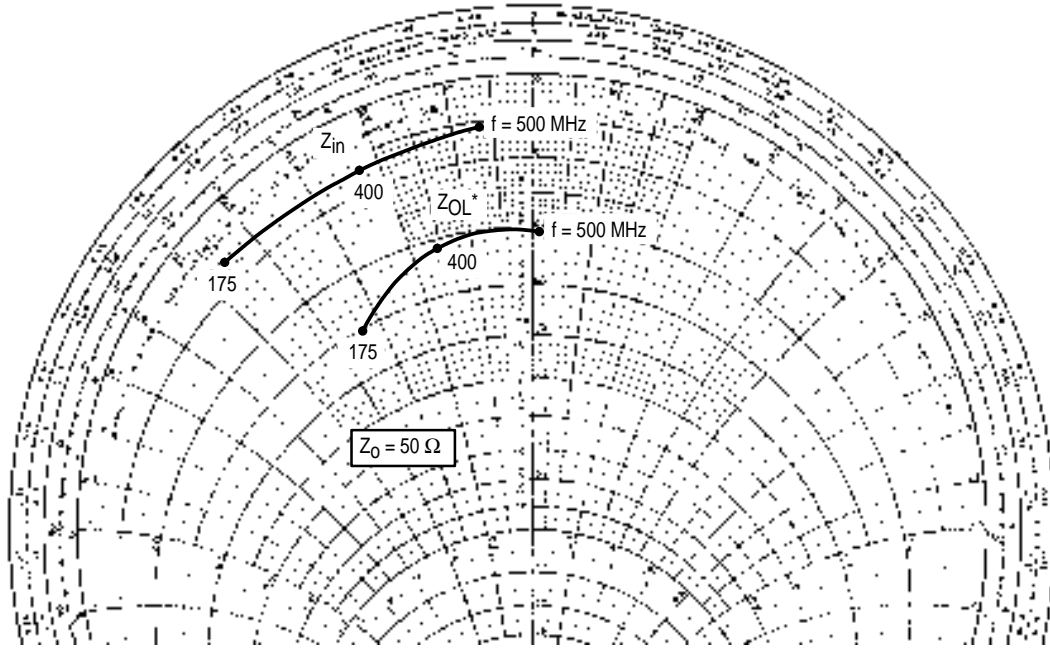


Figure 5. Capacitance versus Voltage



$V_{DD} = 28 \text{ Vdc}$ ,  $I_{DQ} = 100 \text{ mA}$ ,  $P_{out} = 40 \text{ W}$

f MHz	$Z_{in}$ Ohms	$Z_{OL}^*$ Ohms
175	$3.7 - j 22.4$	$15.2 - j 16.6$
400	$3.6 - j 10.99$	$10.3 - j 7.99$
500	$2.6 - j 3.2$	$10.2 + j 0.5$

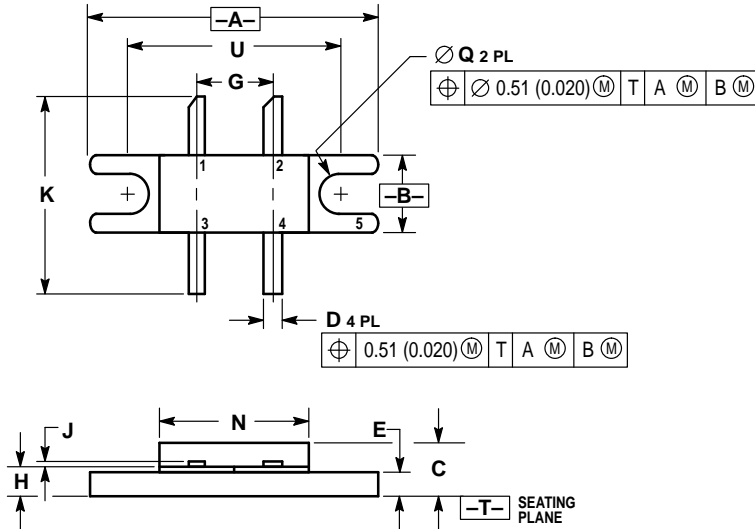
$Z_{OL}^*$  = Conjugate of the optimum load impedance into which the device output operates at a given output power, voltage and frequency.

NOTE: Input and output impedance values given are measured from gate to gate and drain to drain respectively.

**Table 1. Input and Output Impedances**

**Figure 6. Series Equivalent Input/Output Impedance**

## PACKAGE DIMENSIONS



- NOTES:  
 1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.  
 2. CONTROLLING DIMENSION: INCH.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.965	0.985	24.52	25.01
B	0.245	0.265	6.23	6.73
C	0.165	0.185	4.20	4.69
D	0.050	0.070	1.27	1.77
E	0.070	0.080	1.78	2.03
G	0.254 BSC		6.45 BSC	
H	0.095	0.105	2.42	2.66
J	0.003	0.006	0.08	0.15
K	0.625	0.675	15.88	17.14
N	0.495	0.520	12.58	13.20
Q	0.120	0.140	3.05	3.55
U	0.725 BSC		18.42 BSC	

- STYLE 1:  
 PIN 1. DRAIN  
 2. DRAIN  
 3. GATE  
 4. GATE  
 5. SOURCE

### CASE 412-01 ISSUE O

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