

## The RF Line NPN Silicon RF Power Transistor

... designed primarily for wideband large-signal output amplifier stages in the 100 to 500 MHz frequency range.

- Guaranteed Performance @ 400 MHz, 28 Vdc  
Output Power = 80 Watts over 225 to 400 MHz Band  
Minimum Gain = 7.3 dB @ 400 MHz
- Built-In Matching Network for Broadband Operation Using Double Match Technique
- 100% Tested for Load Mismatch at all Phase Angles with 30:1 VSWR
- Gold Metallization System for High Reliability Applications
- Characterized for 100 to 500 MHz

### MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	$V_{CEO}$	33	Vdc
Collector-Base Voltage	$V_{CBO}$	60	Vdc
Emitter-Base Voltage	$V_{EBO}$	4.0	Vdc
Collector Current — Continuous — Peak	$I_C$	9.0 12	Adc
Total Device Dissipation @ $T_C = 25^\circ\text{C}$ (1) Derate above $25^\circ\text{C}$	$P_D$	250 1.43	Watts W/ $^\circ\text{C}$
Storage Temperature Range	$T_{stg}$	-65 to +150	$^\circ\text{C}$

### THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.7	$^\circ\text{C/W}$

### ELECTRICAL CHARACTERISTICS ( $T_C = 25^\circ\text{C}$ unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
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### OFF CHARACTERISTICS

Collector-Emitter Breakdown Voltage ( $I_C = 80$ mAdc, $I_B = 0$ )	$V_{(BR)CEO}$	33	—	—	Vdc
Collector-Emitter Breakdown Voltage ( $I_C = 80$ mAdc, $V_{BE} = 0$ )	$V_{(BR)CES}$	60	—	—	Vdc
Emitter-Base Breakdown Voltage ( $I_E = 8.0$ mAdc, $I_C = 0$ )	$V_{(BR)EBO}$	4.0	—	—	Vdc
Collector-Base Breakdown Voltage ( $I_C = 80$ mAdc, $I_C = 0$ )	$V_{(BR)CBO}$	60	—	—	Vdc
Collector Cutoff Current ( $V_{CB} = 30$ Vdc, $I_E = 0$ )	$I_{CBO}$	—	—	5.0	mAdc

### ON CHARACTERISTICS

DC Current Gain ( $I_C = 4.0$ Adc, $V_{CE} = 5.0$ Vdc)	$h_{FE}$	20	—	80	—
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### DYNAMIC CHARACTERISTICS

Output Capacitance ( $V_{CB} = 28$ Vdc, $I_E = 0$ , $f = 1.0$ MHz)	$C_{ob}$	—	95	125	pF
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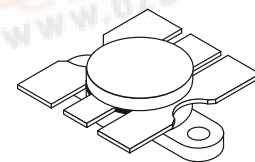
NOTE:

This device is designed for RF operation. The total device dissipation rating applies only when the device is operated as an RF amplifier.

(continued)

**MRF327**

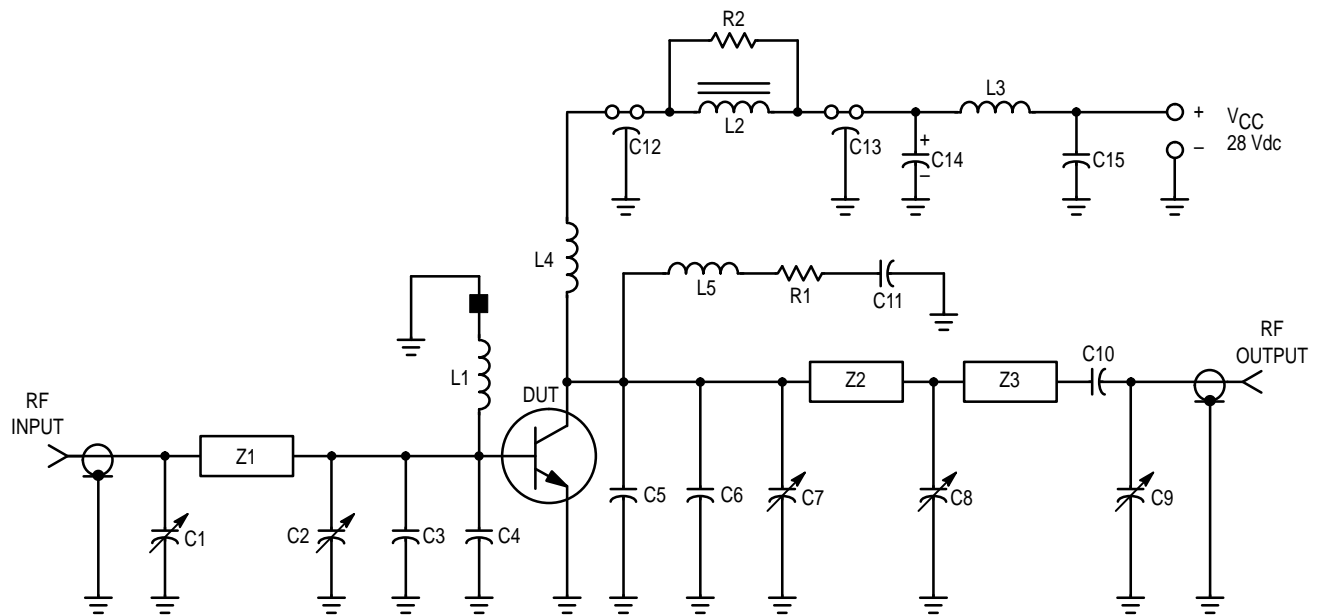
80 W, 100 to 500 MHz  
CONTROLLED "Q"  
BROADBAND RF POWER  
TRANSISTOR  
NPN SILICON



CASE 316-01, STYLE 1

# **ELECTRICAL CHARACTERISTICS – continued** ( $T_C = 25^\circ\text{C}$ unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
<b>FUNCTIONAL TESTS</b> (Figure 1)					
Common–Emitter Amplifier Power Gain ( $V_{CC} = 28\text{ Vdc}$ , $P_{out} = 80\text{ W}$ , $f = 400\text{ MHz}$ )	$G_{PE}$	7.3	9.0	—	dB
Collector Efficiency ( $V_{CC} = 28\text{ Vdc}$ , $P_{out} = 80\text{ W}$ , $f = 400\text{ MHz}$ )	$\eta$	50	60	—	%
Load Mismatch ( $V_{CC} = 28\text{ Vdc}$ , $P_{out} = 80\text{ W}$ , $f = 400\text{ MHz}$ , VSWR = 30:1 All Phase Angles)	$\psi$	No Degradation in Output Power			



C1, C2, C7, C8, C9 — 1.0–20 pF Piston Trimmer (Johanson JMC 5501)  
 C3, C4 — 36 pF ATC 100 mil Chip Capacitor  
 C5, C6 — 43 pF ATC 100 mil Chip Capacitor  
 C10 — 100 pF UNELCO  
 C11, C15 — 0.1  $\mu\text{F}$  Erie Redcap  
 C12, C13 — 680 pF Feedthru  
 C14 — 1.0  $\mu\text{F}$  50 V Tantalum  
 L1 — 4 Turns #22 AWG Enameled, 3/16" ID Closewound with Ferroxcube Bead (#56–590–65/4B) on Ground End of Coil  
 L2 — Ferroxcube VK200–19/4B Ferrite Choke  
 L3 — 7 Turns #18 AWG, 11/16" Long, Wound on a 100 k $\Omega$  2.0 Watt Resistor

L4 — 6 Turns #20 AWG Enameled, 3/16" ID Closewound  
 L5 — 4 Turns #22 AWG Enameled, 1/8" ID Closewound  
 Z1 — Microstrip 0.2" W x 1.5" L  
 Z2 — Microstrip 0.17" W x 1.16" L  
 Z3 — Microstrip 0.17" W x 0.63" L  
 R1, R2 — 10  $\Omega$  2.0 Watt  
 Board — Glass Teflon  $\epsilon_r = 2.56$ ,  $t = 0.062"$   
 Input/Output Connectors Type N  
 DUT Socket Lead Frame Etched from 80–mil–Thick Copper

**Figure 1. 400 MHz Test Circuit**

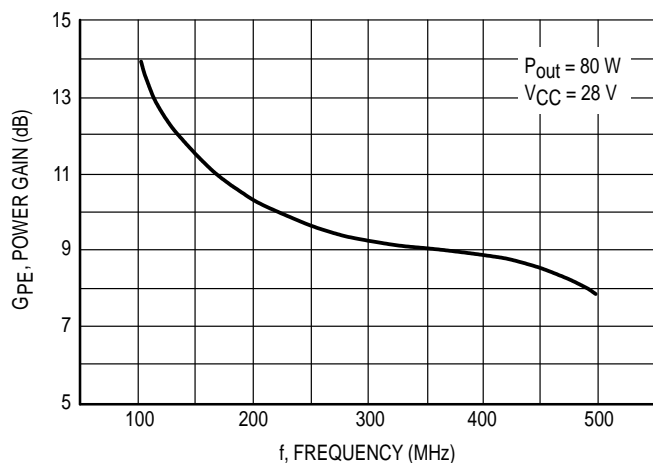


Figure 2. Power Gain versus Frequency

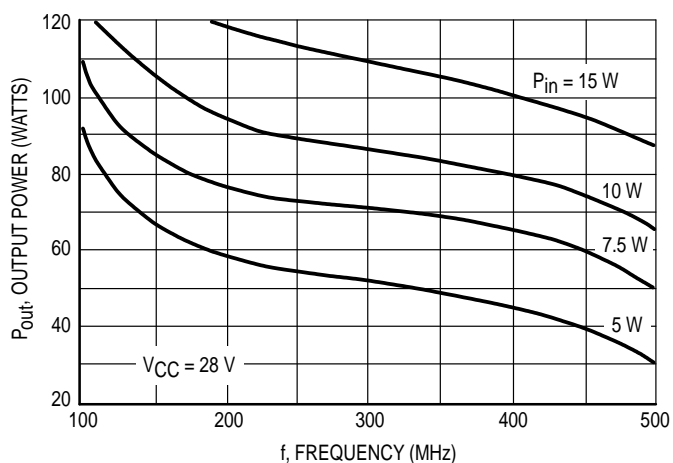


Figure 3. Output Power versus Frequency

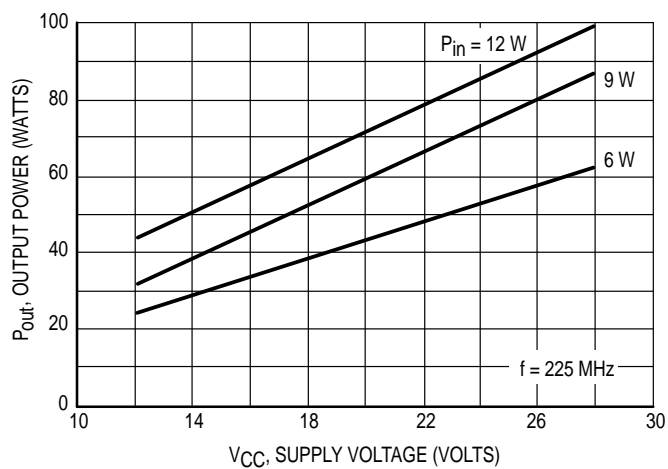


Figure 4. Output Power versus Supply Voltage

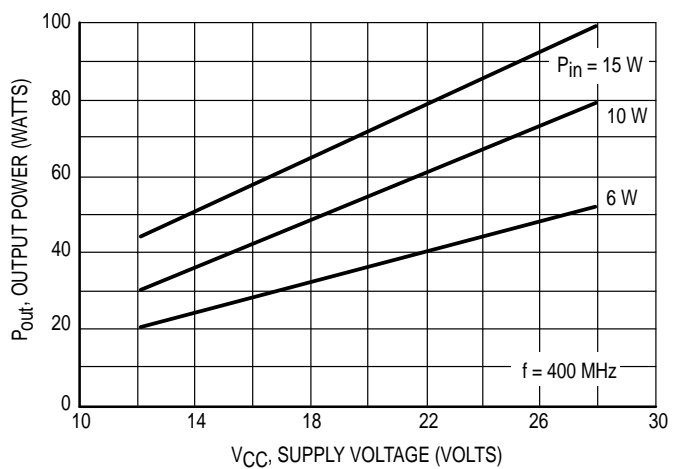


Figure 5. Output Power versus Supply Voltage

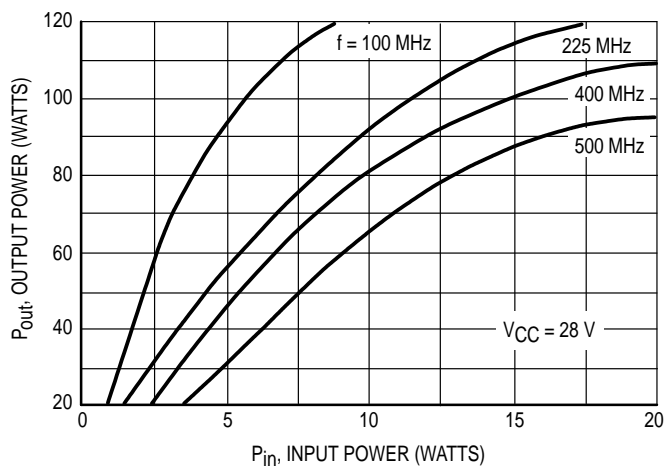
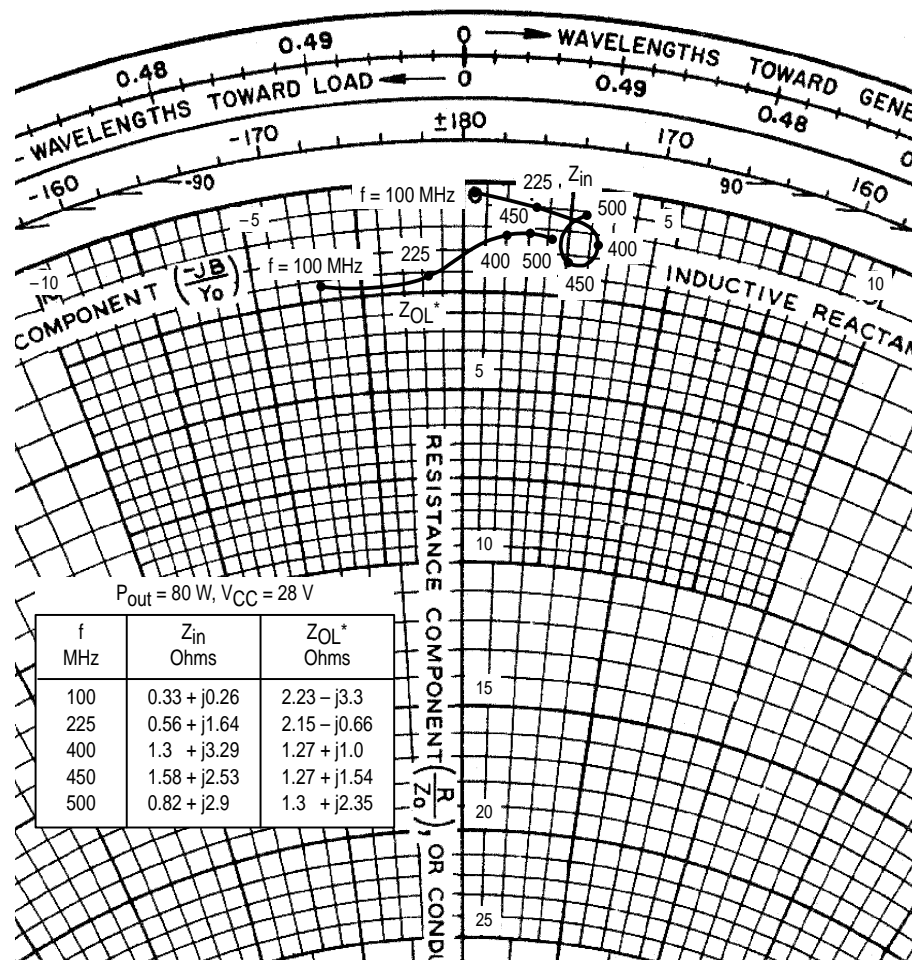


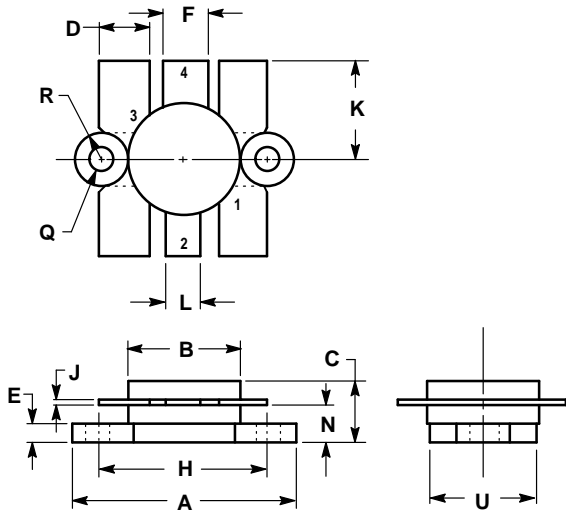
Figure 6. Output Power versus Input Power



$Z_{OL}^*$  = Conjugate of the optimum load impedance into which the device output operates at a given output power, voltage and frequency.

**Figure 7. Series Equivalent Input–Output Impedance**

PACKAGE DIMENSIONS




NOTES:  
1. FLANGE IS ISOLATED IN ALL STYLES.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	24.38	25.14	0.960	0.990
B	12.45	12.95	0.490	0.510
C	5.97	7.62	0.235	0.300
D	5.33	5.58	0.210	0.220
E	2.16	3.04	0.085	0.120
F	5.08	5.33	0.200	0.210
H	18.29	18.54	0.720	0.730
J	0.10	0.15	0.004	0.006
K	10.29	11.17	0.405	0.440
L	3.81	4.06	0.150	0.160
N	3.81	4.31	0.150	0.170
Q	2.92	3.30	0.115	0.130
R	3.05	3.30	0.120	0.130
U	11.94	12.57	0.470	0.495

STYLE 1:  
PIN 1. EMITTER  
2. COLLECTOR  
3. EMITTER  
4. BASE

CASE 316-01  
ISSUE D

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