

6-Channel Volume Controller

Gain and Attenuation 16~-79dB

Low voltage, High Channel Separation

FEATURES

- Operation range: 2.7V~5.5V
- Low power consumption
- Gain/Attenuation: 16dB to -79dB at 1dB/step
- Good PSRR
- I²C interface
- Pop noise free
- Housed in SSOP20, SOP20

APPLICATIONS

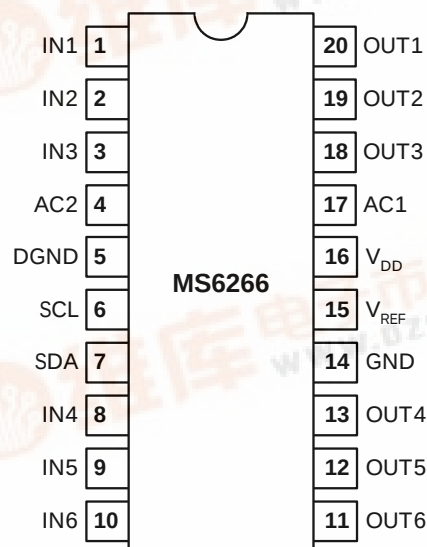
- Multimedia system
- Hi-Fi audio system
- Car audio
- Portable audio equipment

DESCRIPTION

The MS6266 is a 6-channel volume controller IC with gain and attenuation. It uses CMOS technology specially for the low voltage application with low noise, rail-to-rail output. The MS6266 provide an I²C control interface with gain / attenuation range of 16dB to -79dB, 1dB/step. The initial condition is set to be maximum attenuation -79dB and mute on mode when the power is on.

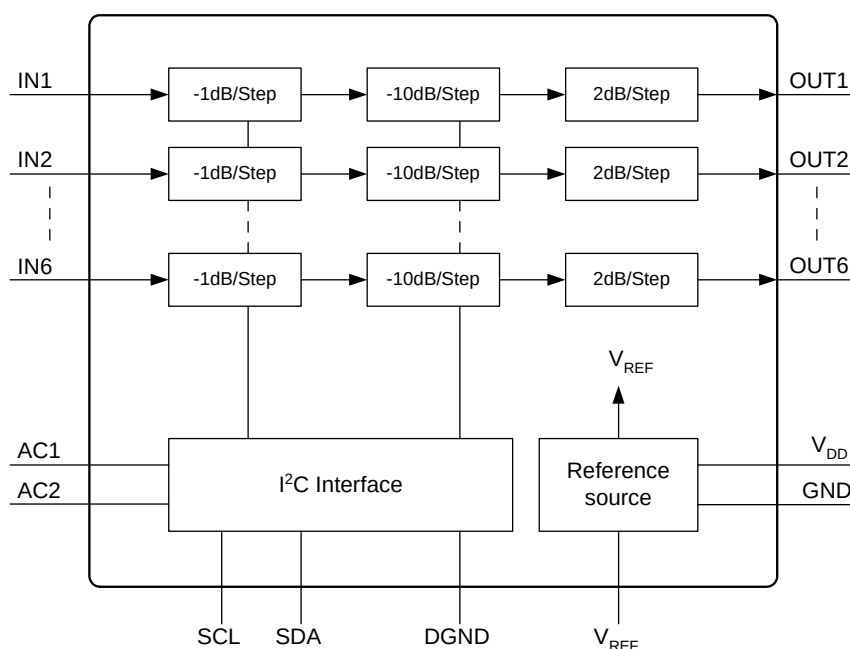
PIN CONFIGURATION

Symbol	Pin	Description
IN1	1	1 st channel input
IN2	2	2 nd channel input
IN3	3	3 rd channel input
AC2	4	Address code 2
DGND	5	Digital Ground
SCL	6	I ² C clock input
SDA	7	I ² C data input
IN4	8	4 th channel input
IN5	9	5 th channel input
IN6	10	6 th channel input
OUT6	11	6 th channel output
OUT5	12	5 th channel output
OUT4	13	4 th channel output
GND	14	Analog ground
V _{REF}	15	Reference voltage = 1/2V _{DD}
V _{DD}	16	Positive supply voltage
AC1	17	Address code 1
OUT3	18	3 rd channel output
OUT2	19	2 nd channel output
OUT1	20	1 st channel output



Note: 1. The address codes have four types, selected by AC1 and AC2.

BLOCK DIAGRAM



ORDERING INFORMATION

Package	Part number	Packaging Marking	Transport Media
20-Pin SOP	MS6266TR	MS6266	1k Units Tape and Reel
20-Pin SOP	MS6266U	MS6266	35 Units Tube
20-Pin SOP (lead free)	MS6266GTR	MS6266G	1k Units Tape and Reel
20-Pin SOP (lead free)	MS6266GU	MS6266G	35 Units Tube
20-Pin SSOP	MS6266SSTR	MS6266	2.5k Units Tape and Reel
20-Pin SSOP	MS6266SSU	MS6266	50 Units Tube
20-Pin SSOP (lead free)	MS6266SSGTR	MS6266G	2.5k Units Tape and Reel
20-Pin SSOP (lead free)	MS6266SSGU	MS6266G	50 Units Tube

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Rating	Unit
V _{DD}	Supply Voltage	6	V
V _{ESD}	Electrostatic Handling	-3000 to 3000	V
T _{STG}	Storage Temperature Range	-65 to 150	°C
T _A	Operating Ambient Temperature Range	-40 to 85	°C
T _J	Maximum Junction Temperature	150	°C
T _S	Soldering Temperature, 10 seconds	260	°C
R _{THJA}	Thermal Resistance from Junction to Ambient in Free Air SOP20 SSOP20	210 210	°C/W

OPERATING RATINGS

Symbol	Parameter	Min	Typ	Max	Unit
V _{DD}	Supply Voltage	2.7	-	5.5	V

5V ELECTRICAL CHARACTERISTICS

(V_{DD}=5.0V, V_{SS}=0V, Attenuation=0dB, Gain=0dB, f=1kHz, V_O=0dBV, V_{REF} Cap=10uF; unless otherwise specified)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
DC Characteristics						
I _Q	Quiescent current		-	10.4	11	mA
A _{GA}	Gain/Attenuation	Max gain	-	16	-	dB
		Max attenuation	-	-79	-	dB
A _{STEP}	Gain/Attenuation step		-	1	-	dB
E _{GA}	Gain/Attenuation step error		-	0.3	-	dB
E _{IGA}	Interchannel gain/attenuation error		-	0.3	-	dB
CS	Channel separation		95	105	-	dB
PSRR	Power supply rejection ratio	Cap = 10uF (100Hz)	-	53	-	dB
MUTE	Mute Attenuation	V _{in} =0dBV	-	85	-	dB
R _{in}	Input Impedance		18	20	-	kΩ
R _{out}	Output Impedance		-	50	100	Ω
AC Characteristics						
V _O	Maximum output voltage swing	(THD+N)/S < 0.1%	-	4.8	-	V _{pp}
THD+N	Total harmonic distortion plus noise		-	-69	-64	dB
S/N	Signal-to-noise ratio	V _O =4.8V _{pp}	95	100	-	dB
Bus Characteristics						
V _{IH}	Bus high input level		-	-	0.7V _{DD}	V
V _{IL}	Bus low input level		0.3V _{DD}	-	-	V

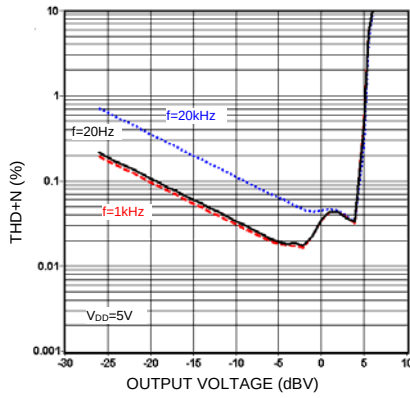
2.7V ELECTRICAL CHARACTERISTICS

(V_{DD}=2.7V, V_{SS}=0V, Attenuation=0dB, Gain=0dB, f=1kHz, V_O=-3dBV, V_{REF} Cap=10uF; unless otherwise specified)

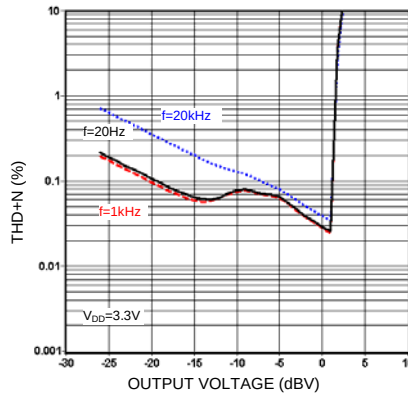
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
DC Characteristics						
I _Q	Quiescent current		-	8.2	8.8	mA
CS	Channel separation		90	100	-	dB
PSRR	Power supply rejection ratio	Cap = 10uF (100Hz)	-	51	-	dB
MUTE	Mute Attenuation	V _{in} =-3dBV	-	80	-	dB
AC Characteristics						
V _O	Maximum output voltage swing	(THD+N)/S < 0.1%	-	2.6	-	V _{pp}
THD+N	Total harmonic distortion plus noise		-	-69	-64	dB
S/N	Signal-to-noise ratio	V _O =2.6V _{pp}	85	90	-	dB

TYPICAL PERFORMANCE CHARACTERISTICS

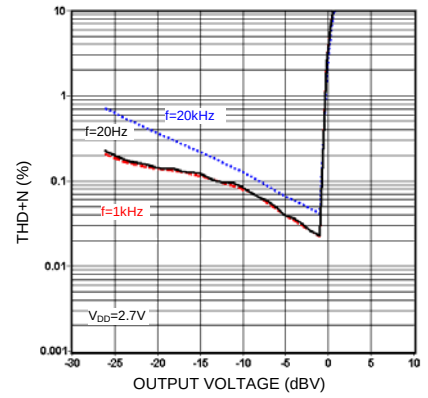
($T_a=25^{\circ}\text{C}$, $R_L=100\text{k}\Omega$, V_{REF} Cap=10 μF ; unless otherwise specified)



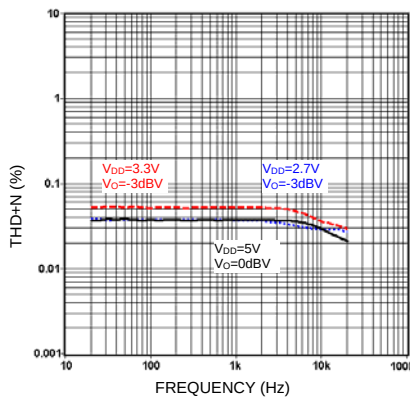
THD+N vs. output voltage



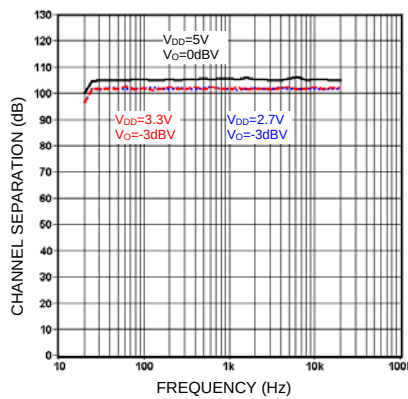
THD+N vs. output voltage



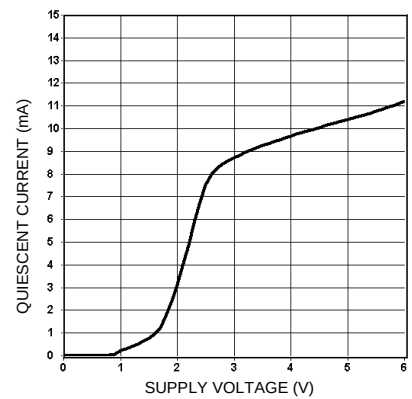
THD+N vs. output voltage



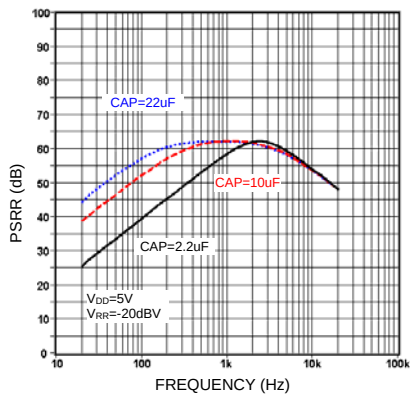
THD+N vs. frequency



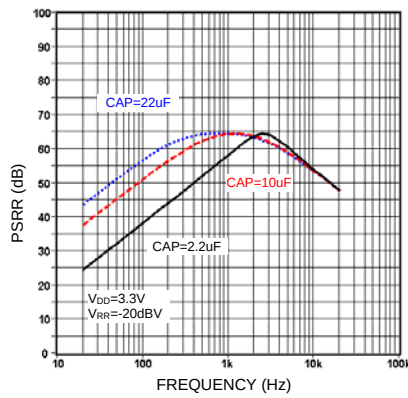
Channel separation vs. frequency



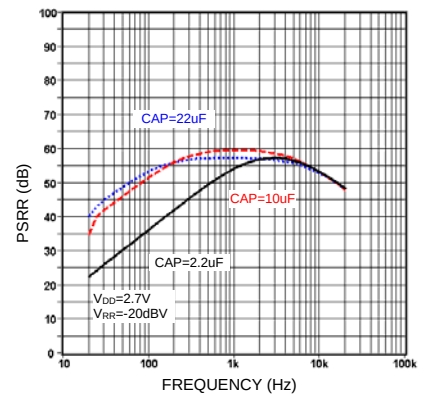
Quiescent current vs. supply voltage



PSRR vs. frequency



PSRR vs. frequency

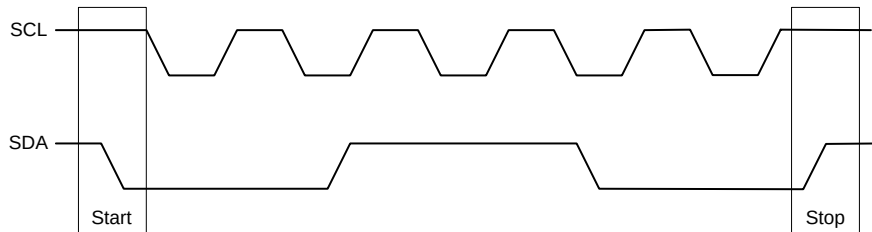


PSRR vs. frequency

I²C BUS DESCRIPTION

Start and stop conditions

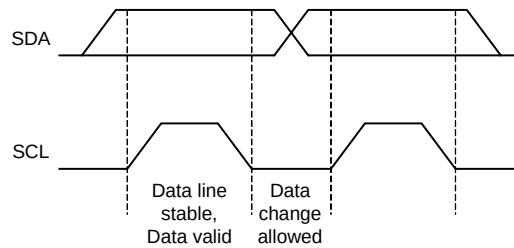
A start condition is activated when the SCL is set to HIGH and SDA shifts from HIGH to LOW state. The stop condition is activated when SCL is set to HIGH and SDA shifts from LOW to HIGH state. Please refer to the timing diagram below.



SCL : Serial Clock Line, SDA : Serial Data Line

Data validity

A data on the SDA line is considered valid and stable only when the SCL signal is in HIGH state. The HIGH and LOW states of the SDA line can only change when the SCL signal is LOW. Please refer to the figure below.

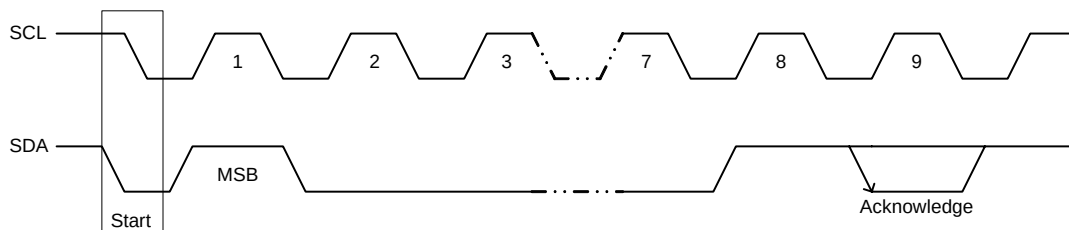


Byte format

Every byte transmitted to the SDA line consists of 8 bits. Each byte must be followed by an acknowledge bit. The MSB is transmitted first.

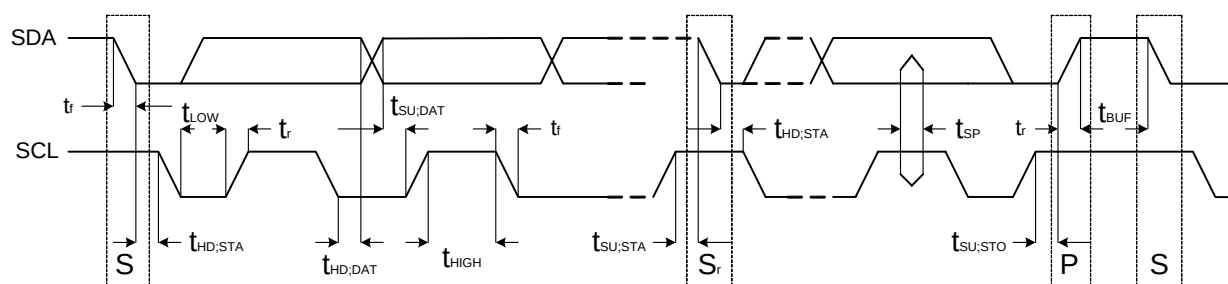
Acknowledge

During the Acknowledge clock pulse, the master (up) put a resistive HIGH level on the SDA line. The peripheral (audio processor) that acknowledges has to pull-down (LOW) the SDA line during the Acknowledge clock pulse so that the SDA line is in a stable LOW state during this clock pulse. Please refer to the diagram below.



The audio processor that has been addressed has to generate an Acknowledge after receiving each byte, otherwise, the SDA line will remain at the HIGH level during the ninth (9th) clock pulse. In this case, the master transmitter can generate the STOP information in order to abort the transfer.

Timing of SDA and SCL bus lines

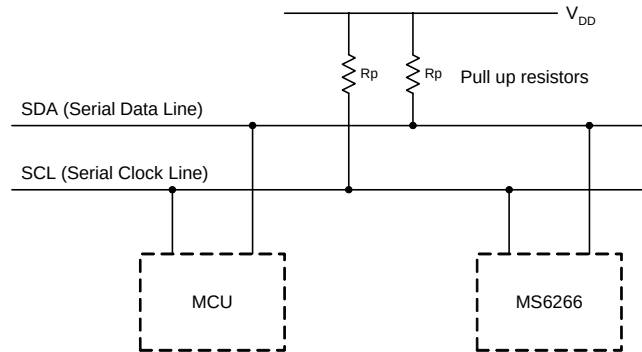


Standard mode

Symbol	Parameter	Min	Max	Unit
f_{SCL}	SCL clock frequency	0	100	kHz
$t_{HD:STA}$	Hold time (repeated) START condition. After this period, the first clock pulse is generated	4.0	-	us
t_{LOW}	LOW period of the SCL clock	4.7	-	us
t_{HIGH}	HIGH period of the SCL clock	4.0	-	us
$t_{SU:STA}$	Set-up time for a repeated START condition	4.7	-	us
$t_{HD:DAT}$	Data hold time; For I ² C-bus devices	0	3.45	us
$t_{SU:DAT}$	Data-set-up time	250	-	ns
t_r	Rise time of both SDA and SCL signals	-	1000	ns
t_f	Fall time of both SDA and SCL signals	-	300	ns
$t_{SU:STO}$	Set-up time for STOP condition	4.0	-	us
t_{BUF}	Bus free time between a STOP and START condition	4.7	-	us
C_b	Capacitive load for each bus line	-	400	pF
V_{nL}	Noise margin at the LOW level for each connected device (including hysteresis)	$0.1V_{DD}$	-	V
V_{nH}	Noise margin at the HIGH level for each connected device (including hysteresis)	$0.2V_{DD}$	-	V

BUS INTERFACE

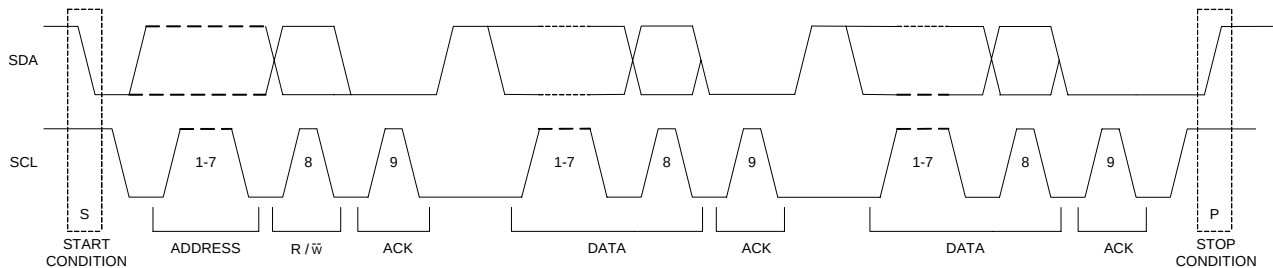
Data are transmitted to and from the MCU to the MS6266 via the SDA and SCL. The SDA and SCL make up the BUS interface. It should be noted that pull-up resistors must be connected to the positive supply voltage.



Interface protocol

The format consists of the following

- A START condition
- A chip address byte including the MS6266 address. (7bits)
- The 8th bit of the byte must be "0".(write=0, read=1)
- MS6266 must always acknowledge the end of each transmitted byte.
- A data sequence (N-bytes + Acknowledge)
- A STOP condition



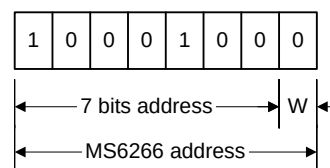
Address code

The MS6266 has four address codes, they were selected by AC1(pin17)and AC2(pin4).

AC1	AC2	Address code
0	0	80H
0	1	84H
1	0	88H
1	1	8CH

0: connected to GND, 1: connected to V_{DD}

AC1=1, AC2=0



Data bytes description

Function bits								
MSB							LSB	Function
1	1	1	0	A3	A2	A1	A0	6 channels, -1dB/step
1	1	0	1	B3	B2	B1	B0	6 channels, -10dB/step or +2dB/step
0	0	0	1	A3	A2	A1	A0	Channel 3, -1dB/step
0	0	0	0	B3	B2	B1	B0	Channel 3, -10dB/step or +2dB/step
0	0	1	1	A3	A2	A1	A0	Channel 4, -1dB/step
0	0	1	0	B3	B2	B1	B0	Channel 4, -10dB/step or +2dB/step
0	1	0	1	A3	A2	A1	A0	Channel 2, -1dB/step
0	1	0	0	B3	B2	B1	B0	Channel 2, -10dB/step or +2dB/step
0	1	1	1	A3	A2	A1	A0	Channel 5, -1dB/step
0	1	1	0	B3	B2	B1	B0	Channel 5, -10dB/step or +2dB/step
1	0	0	1	A3	A2	A1	A0	Channel 1, -1dB/step
1	0	0	0	B3	B2	B1	B0	Channel 1, -10dB/step or +2dB/step
1	0	1	1	A3	A2	A1	A0	Channel 6, -1dB/step
1	0	1	0	B3	B2	B1	B0	Channel 6, -10dB/step or +2dB/step
1	1	1	1	0	0	0	1	Power off preparation (pop noise free)
				1	0	0	1	6 channels, mute On
				1	0	0	0	6 channels, mute Off

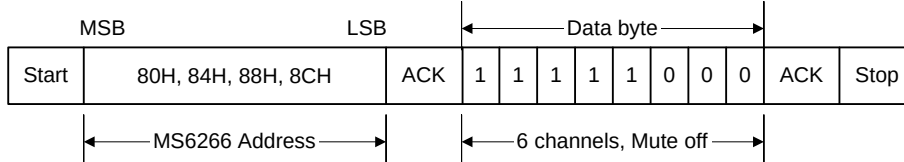
Gain / Attenuation bits					
A3	A2	A1	A0	Gain / Attenuation value (dB)	
B3	B2	B1	B0	A	B
0	0	0	0	0	0
0	0	0	1	-1	-10
0	0	1	0	-2	-20
0	0	1	1	-3	-30
0	1	0	0	-4	-40
0	1	0	1	-5	-50
0	1	1	0	-6	-60
0	1	1	1	-7	-70
1	0	0	0	-8	+2
1	0	0	1	-9	+4
1	0	1	0	-	+6
1	0	1	1	-	+8
1	1	0	0	-	+10
1	1	0	1	-	+12
1	1	1	0	-	+14
1	1	1	1	-	+16

1. Where $Ax = -1\text{dB/step}$, $Bx = -10\text{dB/step or } +2\text{dB/step}$, -10dB and $+2\text{dB}$ should not be loaded at the same time.
2. The initial condition is set to be maximum attenuation -79dB and mute on mode when the power on.
3. The output will drop down to ground gradually when enable power off preparation.
4. Odd gain $2N-1 = N * (+2\text{dB/step}) + (-1\text{dB})$, where $N = 1 \sim 8$. Please reference to examples.

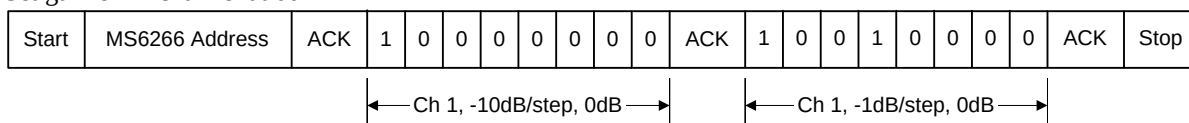
Examples

Mute off

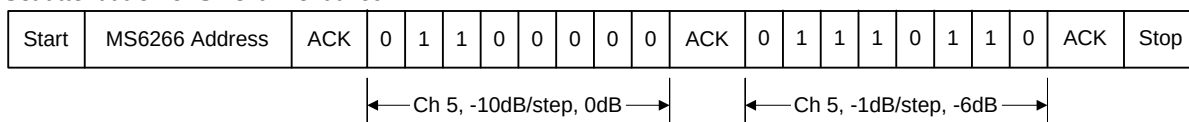
The initial condition is -79dB and mute on when power on. The first command must disable the mute function.



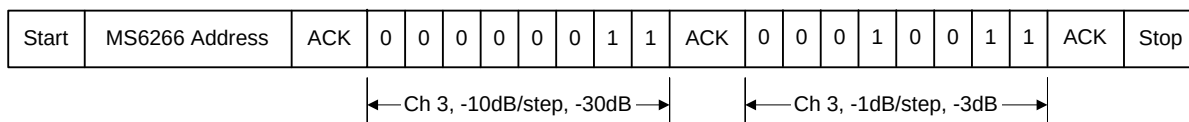
Set gain of 1st channel at 0dB



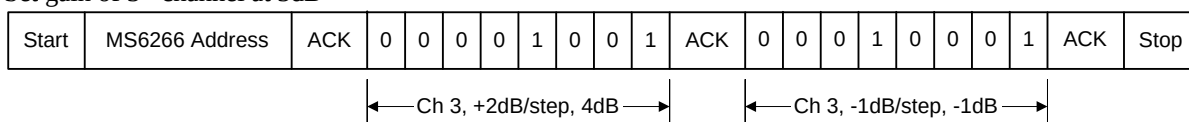
Set attenuation of 5th channel at -6dB



Set attenuation of 3rd channel at -33dB

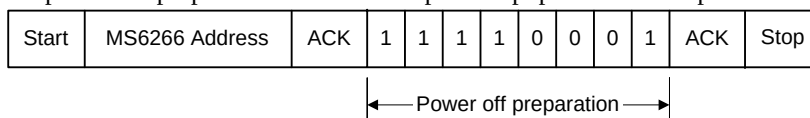


Set gain of 3rd channel at 3dB



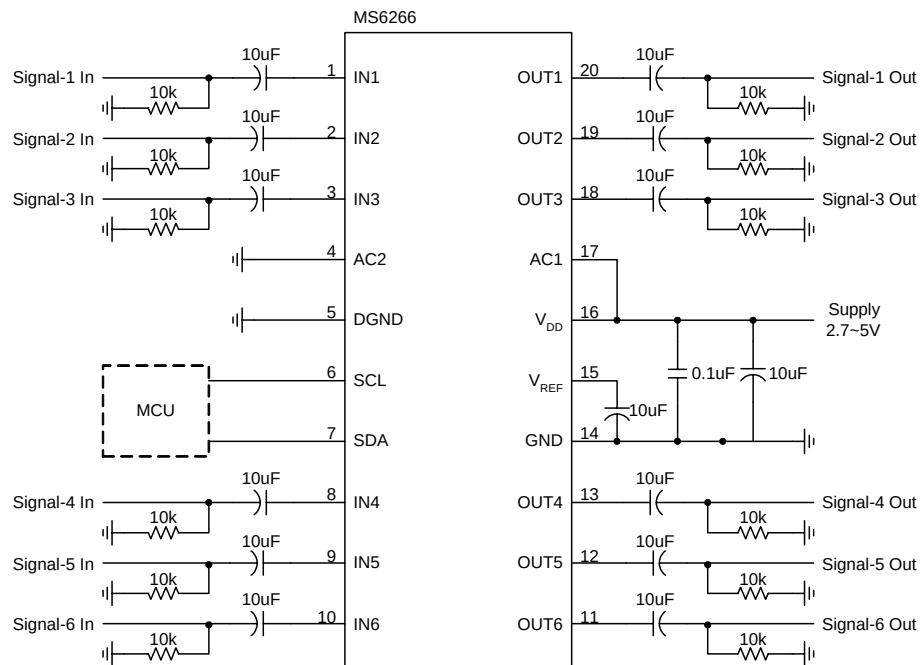
Odd gain 3dB = 2*2-1 = 2*(+2dB)+(-1dB)

Set power off preparation command to prevent pop noise before power is off.



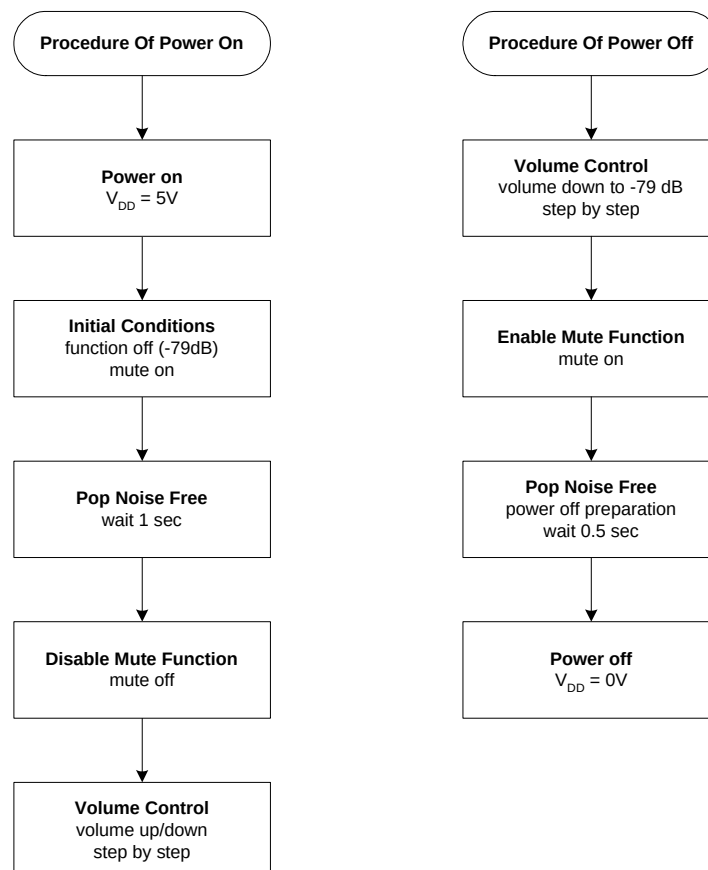
APPLICATION INFORMATION

Basic application example



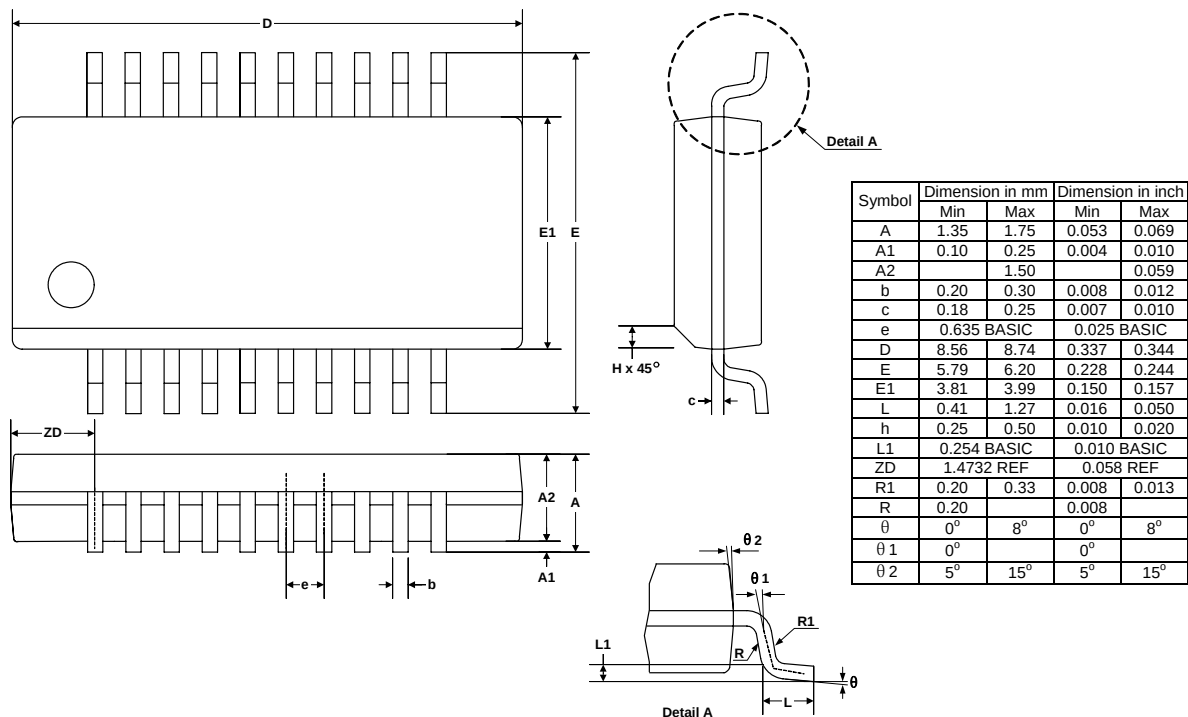
AC1=Hi, AC2=Lo, Address=88H

Basic application flow chart



EXTERNAL DIMENSIONS

SSOP20



SOP20 (300mil)

