MS81V06160 Preliminary

(401,408-word × 16-bit) FIFO memory

GENERAL DESCRIPTION

The MS81V06160 is a 6Mb FIFO (First-In First-Out) memory designed for 401,408-words × 16-bit high-speed asynchronous read/write operation.

The MS81V06160 is best suited for a field memory for digital TVs or LCD panels which require high-speed, large memory , and is not designed for high end use in professional graphics systems, which require long term picture storage and data storage.

The MS81V06160 is provided with independent control clocks to support asynchronous read and write operations. Different clock rates are also supported, which allow alternate data rates between write and read data streams.

The first data read operation can be performed after 1600 ns + 4 cycles from read reset and the first data write operation is enabled after 1600 ns + 4 cycles from write reset. Thereafter, the high-speed read/write operation is possible every cycle time.

Additionally, a write mask function by IE pin and a read-data skipping function by OE pin implement image data processing easily.

The MS81V06160 provides high speed FIFO (First-in First-out) operation without external refreshing: MS81V06160 refreshes its DRAM storage cells automatically, so that it appears fully static to the users.

Moreover, fully static type memory cells and decoders for serial access enable the refresh free serial access operation, so that serial read and/or write control clock can be halted high or low for any duration as long as the power is on. Internal conflicts of memory access and refreshing operations are prevented by special arbitration logic.

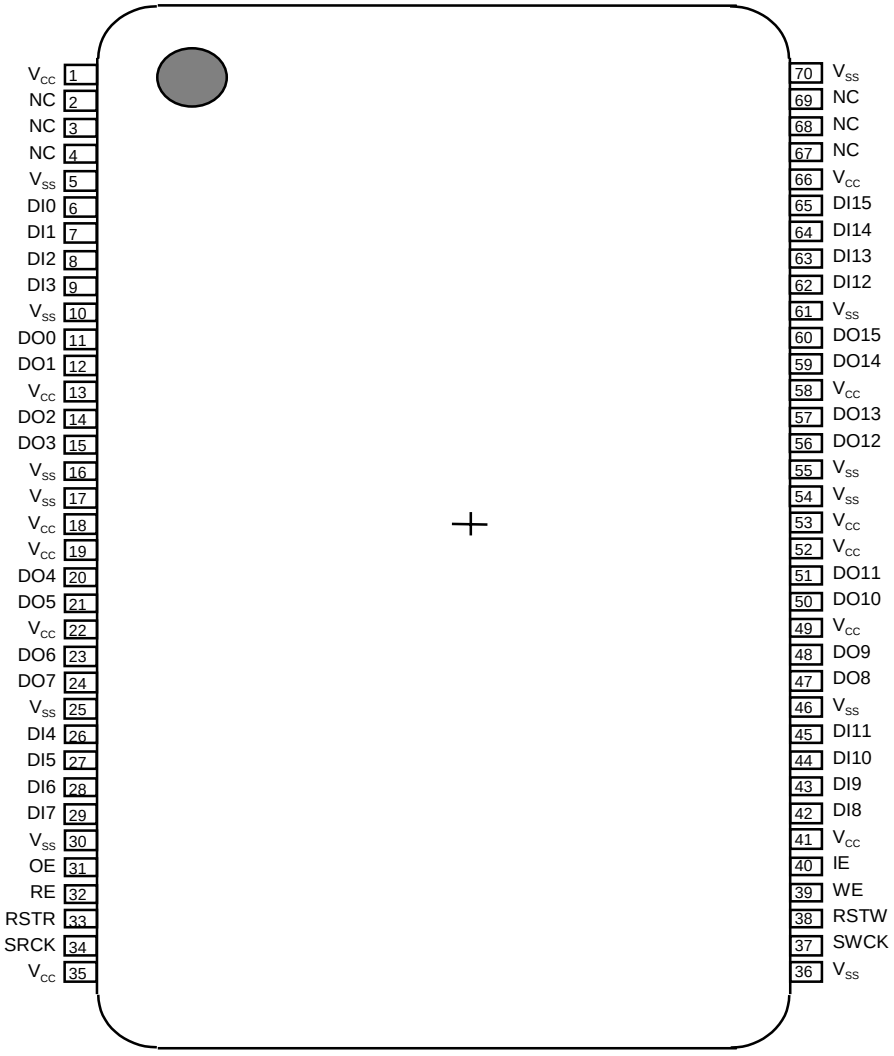
The MS81V06160's function is simple, and similar to a digital delay device whose delay-bit- length is easily set by reset timing. The delay length and the number of read delay clocks between write and read, is determined by externally controlled write and read reset timings. The MS81V06160 uses a thin and small 70-pin plastic TSOP.

FEATURES

- 401,408 words × 16 bits
- Fast FIFO (First-In First-Out) operation: 12 ns cycle time
- Self refresh (No refresh control is required)
- High speed asynchronous serial access
  Read/Write Cycle Time 12 ns/15 ns
  Access Time 9 ns/12 ns
- Variable length delay bit (600 to 401,408)
- Write mask function (Output enable control)
- Cascading capability
- Single power supply: 3.3 V ± 10%
- Package:
  70-pin plastic TSOP TYPE II (TSOP II 70-P-400-0.5-K) (Product name: MS81V06160-xxTA)
  xx indicates speed rank.

Parameter	Symbol	MS81V06160-TA	
		–12	–15
Access Time	tAC	9 ns	12 ns
Read/Write Cycle Time	tSWC tSRC	12 ns	15 ns
Operation current	Icc1	210 mA	170 mA
Standby current	Icc2	6 mA	6 mA

PIN CONFIGURATION (TOP VIEW)

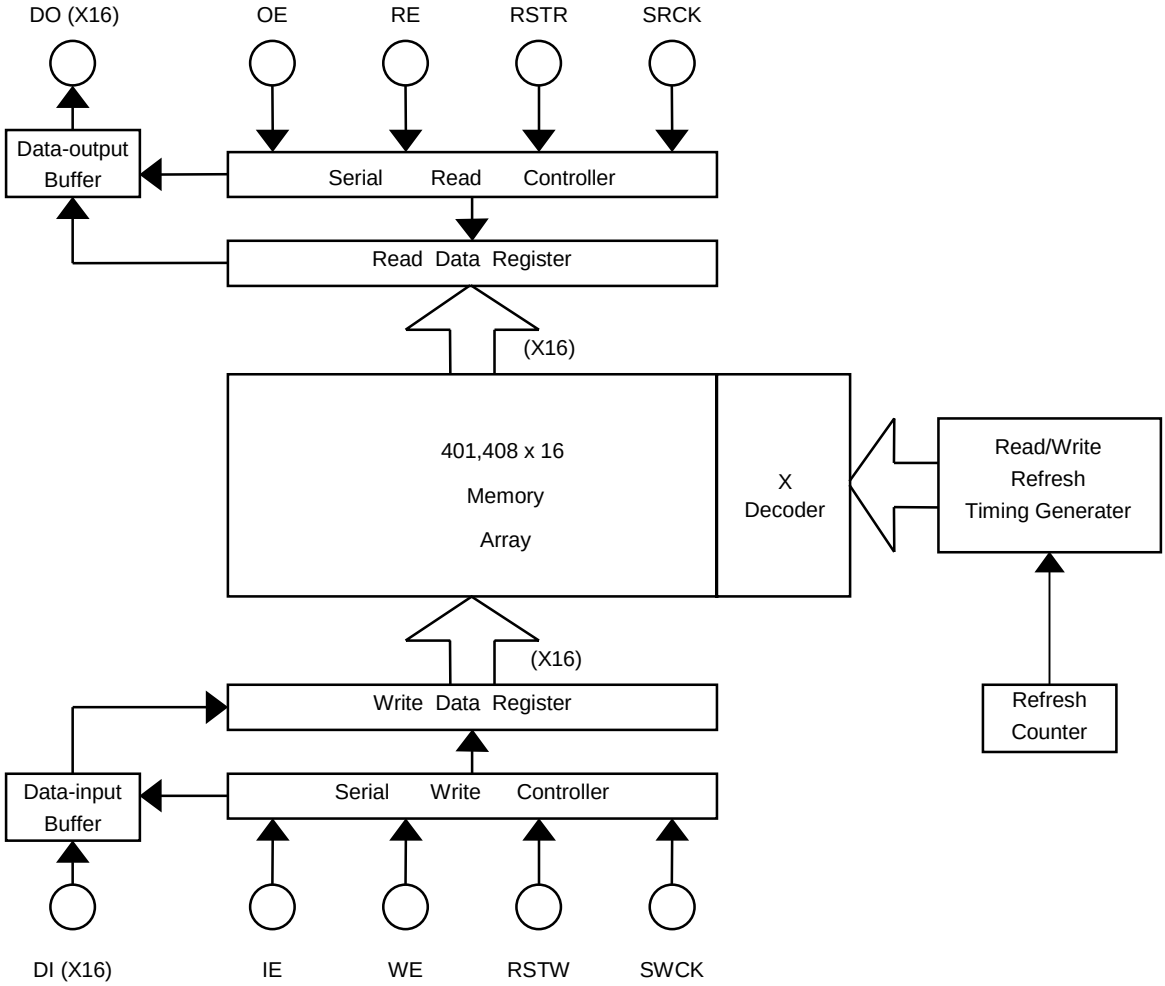


70-pin Plastic TSOP

SWCK	Serial Write Clock
SRCK	Serial Read Clock
WE	Write Enable
RE	Read Enable
IE	Input Enable
OE	Output Enable
RSTW	Reset Write
RSTR	Reset Read
DI0-15	Data Input
DO0-15	Data Output
V_{SS}	Ground (0 V)
V_{CC}	Power Supply (3.3 V)
NC	No Connection

Note: The same power supply voltage must be provided to every V_{CC} pin, and the same GND voltage level must be provided to every V_{SS} pin.

BLOCK DIAGRAM



PIN DESCRIPTION

Data Inputs: (DI0-15)
These pins are used for serial data inputs.

Write Reset: RSTW
The first positive transition of SWCK after RSTW becomes high resets the write address pointers to zero. RSTW setup and hold times are referenced to the rising edge of SWCK.

Write Enable: WE
WE is used for data write enable/disable control. WE high level enables the input, and WE low level disables the input and holds the internal write address pointer. There are no WE disable time (low) and WE enable time (high) restrictions, because the MS8106160 is in fully static operation as long as the power is on. Note that WE setup and hold times are referenced to the rising edge of SWCK. The latency for the write operation control by WE is 2.
After write reset, WE must remain low for more than 1600 ns (tFWD). After write reset, the write operation at address 0 is started after a time tWL form the cycle in which WE is brought high.
After write reset, WE should be remained high for 2 cycles after driving WE high first.

Input Enable: IE
IE is used to enable/disable writing into memory. IE high level enables writing. The internal write address pointer is always incremented by cycling SWCK regardless of the IE level. Note that IE setup and hold times are referenced to the rising edge of SWCK. The latency for the write operation control by IE is 2.

Data Out: (DO0-15)
These pins are used for serial data outputs.

Read Reset: RSTR
The first positive transition of SRCK after RSTR becomes high resets the read address pointers to zero.
RSTR setup and hold times are referenced to the rising edge of SRCK.

Read Enable: RE
The function of RE is to gate of the SRCK clock for incrementing the read pointer. When RE is high before the rising edge of SRCK, the read pointer is incremented. When RE is low, the read pointer is not incremented. RE setup times (tRENS and tRDSS) and RE hold times (tRENH and tRDSH) are referenced to the rising edge of the SRCK clock.
The latency for the read operation control by RE is 2. After read reset, RE must remain low for more than 1600 ns (tFRD). After read reset, the read data at address 0 is output after a time tRL from the cycle in which WE is brought high.
After read reset, RE should be remained high for 2 cycles after driving RE high first.

Output Enable: OE
OE is used to enable/disable the outputs. OE high level enables the outputs. The internal read address pointer is always incremented by cycling SRCK regardless of the OE level. Note that OE setup and hold times are referenced to the rising edge of SRCK. The latency for the read operation control by OE is 2.

Serial Write Clock: SWCK
The SWCK latches the input data on chip when WE is high, and also increments the internal write address pointer. Data-in setup time tDS, and hold time tDH are referenced to the rising edge of SWCK.

Serial Read Clock: SRCK
Data is shifted out of the data registers. It is triggered by the rising edge of SRCK when RE is high during a read operation. The SRCK input increments the internal read address pointer when RE is high.
The three-state output buffer provides direct TTL compatibility (no pullup resistor required). Data out is the same polarity as data in. The output becomes valid after the access time interval tAC that begins with the rising edge of SRCK. *There are no output valid time restriction on MS8106160.

ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Power Supply Voltage	V_{CC}	Ta = 25°C	• 0.5 to +4.6	V
Input Output Voltage	V_T	Ta = 25°C, V_{SS}	• 0.5 to +4.6	V
Output Current	I_{OS}	Ta = 25°C	50	mA
Power Dissipation	P_D	Ta = 25°C	1	W
Operating Temperature	T_{opr}	—	0 to 70	°C
Storage Temperature	T_{stg}	—	• 55 to +150	°C

Recommended Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit
Power Supply voltage	V_{CC}	3.0	3.3	3.6	V
Input High Voltage	V_{IH}	2.0	V_{CC}	V_{CC} + 0.2	V
Input Low Voltage	V_{IL}	• 0.3	0	0.8	V

DC Characteristics

Parameter	Symbol	Condition		Min.	Max.	Unit
Input Leakage Current	I_{LI}	$0 < V_I < V_{CC}$, Other Pins Tested at V = 0 V		–10	+10	µA
Output Leakage Current	I_{LO}	$0 < V_O < V_{CC}$		–10	+10	µA
Output “H” Level Voltage	V_{OH}	I_{OH} = –2 mA		2.4	—	V
Output “L” Level Voltage	V_{OL}	I_{OH} = 2 mA		—	0.4	V
Operating Current	I_{CC1}	Minimum Cycle Time Output Open	–12	—	210	mA
			–15	—	170	
Standby Current	I_{CC2}	Input Pin = V_{IH}/V_{IL}	–12	—	6	mA
			–15	—	6	

Capacitance

(V_{CC} = 3.3 V ± 0.3 V, Ta = 25°C, f = 1 MHz)

Parameter	Symbol	Max.	Unit
Input Capacitance	C_I	5	pF
Output Capacitance	C_O	7	pF

AC Characteristics

(V_{CC} = 3.3 V ± 10%, Ta = 0 to 70°C)

Parameter	Symbol	MS81V06160-12		MS81V06160-15		Unit
		Min.	Max.	Min.	Max.	
Access Time from SRCK	t_{AC}	—	9	—	12	ns
D_{OUT} Hold Time from SRCK	t_{DDCK}	3	—	3	—	ns
D_{OUT} Enable Time from SRCK	t_{DECK}	3	9	3	12	ns
SWCK “H” Pulse Width	t_{WSWH}	4	—	6	—	ns
SWCK “L” Pulse Width	t_{WSWL}	4	—	6	—	ns
Input Data Setup Time	t_{DS}	3	—	3	—	ns
Input Data Hold Time	t_{DH}	1	—	1.5	—	ns
WE Enable Setup Time	t_{WENS}	3	—	3	—	ns
WE Enable Hold Time	t_{WENH}	1	—	1.5	—	ns
WE Disable Setup Time	t_{WDSS}	3	—	3	—	ns
WE Disable Hold Time	t_{WDSH}	1	—	1.5	—	ns
IE Enable Setup Time	t_{IENS}	3	—	3	—	ns
IE Enable Hold Time	t_{IENH}	1	—	1.5	—	ns
IE Disable Setup Time	t_{IDSS}	3	—	3	—	ns
IE Disable Hold Time	t_{IDSH}	1	—	1.5	—	ns
WE “H” Pulse Width	t_{WWEH}	4	—	6	—	ns
WE “L” Pulse Width	t_{WWEL}	4	—	6	—	ns
IE “H” Pulse Width	t_{WIEH}	4	—	6	—	ns
IE “L” Pulse Width	t_{WIEL}	4	—	6	—	ns
RSTW Setup Time	t_{RSTWS}	3	—	3	—	ns
RSTW Hold Time	t_{RSTWH}	1	—	1.5	—	ns
SRCK “H” Pulse Width	t_{WSRH}	4	—	6	—	ns
SRCK “L” Pulse Width	t_{WSRL}	4	—	6	—	ns
RE Enable Setup Time	t_{RENS}	3	—	3	—	ns
RE Enable Hold Time	t_{RENH}	1	—	1.5	—	ns
RE Disable Setup Time	t_{RDSS}	3	—	3	—	ns
RE Disable Hold Time	t_{RDSH}	1	—	1.5	—	ns
OE Enable Setup Time	t_{OENS}	3	—	3	—	ns
OE Enable Hold Time	t_{OENH}	1	—	1.5	—	ns
OE Disable Setup Time	t_{ODSS}	3	—	3	—	ns
OE Disable Hold Time	t_{ODSH}	1	—	1.5	—	ns
RE “H” Pulse Width	t_{WREH}	4	—	6	—	ns
RE “L” Pulse Width	t_{WREL}	4	—	6	—	ns
OE “H” Pulse Width	t_{WOEH}	4	—	6	—	ns
OE “L” Pulse Width	t_{WOEL}	4	—	6	—	ns
RSTR Setup Time	t_{RSTRS}	3	—	3	—	ns
RSTR Hold Time	t_{RSTRH}	1	—	1.5	—	ns
SWCK Cycle Time	t_{SWC}	12	—	15	—	ns
SRCK Cycle Time	t_{SRC}	12	—	15	—	ns
Transition Time (Rise and Fall)	t_T	1	5	1	5	ns
WE “L” Period before W Reset	t_{LWE}	3	—	3	—	clk
RE “L” Period before R Reset	t_{LRE}	3	—	3	—	clk
RE Delay after Reset	t_{FRD}	1,600	—	1,600	—	ns
WE Delay after Reset	t_{FWD}	1,600	—	1,600	—	ns

Parameter	Symbol	MS81V06160-12, MS81V06160-15	Unit
Write Latency	t_{WL}	4	clk
Read Latency	t_{RL}	4	clk
WE Write Control Latency	t_{WEL}	2	clk
IE Write Control Latency	t_{IEL}	2	clk
RE Read Control Latency	t_{REL}	2	clk
OE Read Control Latency	t_{OEL}	2	clk

AC Characteristic Measuring Conditions

Output Compare Level	1.4 V
Output Load	1 TTL + 30 pF
Input Signal Level	3.0 V/0.0 V
Input Signal Rise/Fall Time	1 ns
Input Signal Measuring Reference Level	1.4 V

Note: Input voltage levels for the AC characteristic measurement are V_{IH} = 3.0 V and V_{IL} = 0 V. When transition time t_T becomes 1 ns or more, the input signal reference levels for the parameter measurement are V_{IH} (min.) and V_{IL} (max.).

OPERATION MODE

Write Operation Cycle

The write operation is controlled by four control signals, SWCK, RSTW, WE, and IE. The write operation is accomplished by cycling SWCK, and holding WE high after the write address pointer reset operation or RSTW. RSTW must be performed for internal circuit initialization before write operation. WE must be low before and after the reset cycle (t_{LWE} + t_{FWD}).

Each write operation, which begins after RSTW must contain at least 231 active write cycles, i.e., SWCK cycles while WE and IE are high.

Settings of WE and IE to the operation mode of Write address pointer and Data input.

WE	IE	Internal Write address pointer	Data input (Latency 2)
H	H	Incremented	Input
H	L		Not input
L	X	Halted	

X indicates "don't care"

Read Operation Cycle

The read operation is controlled by four control signals, SRCK, RSTR, RE, and OE. The read operation is accomplished by cycling SRCK, and holding both RE and OE high after the read address pointer reset operation or RSTR.

Each read operation, which begins after RSTR, must contain at least 231 active read cycles, i.e., SRCK cycles while RE and OE are high. RE must be low before and after the reset cycle (t_{LRE} + t_{FWD}).

Settings of RE and OE to the operation mode of read address pointer and Data output.

RE	OE	Internal Read address pointer	Data output (Latency 2)
H	H	Incremented	Output
H	L		High impedance
L	H	Halted	Output
L	L		High impedance

Power-up and Initialization

On power-up, the device is designed to begin proper operation after at least 200 µs after Vcc has stabilized to a value within the range of recommended operating conditions. After this 200 µs stabilization interval, the following initialization sequence must be performed. Because the read and write address pointers are undefined after power-up, a minimum of 330 dummy write operations (SWCK cycles) and read operations (SRCK cycles) must be performed, followed by an RSTW operation and an RSTR operation, to properly initialize the write and the read address pointer.

Old/New Data Access

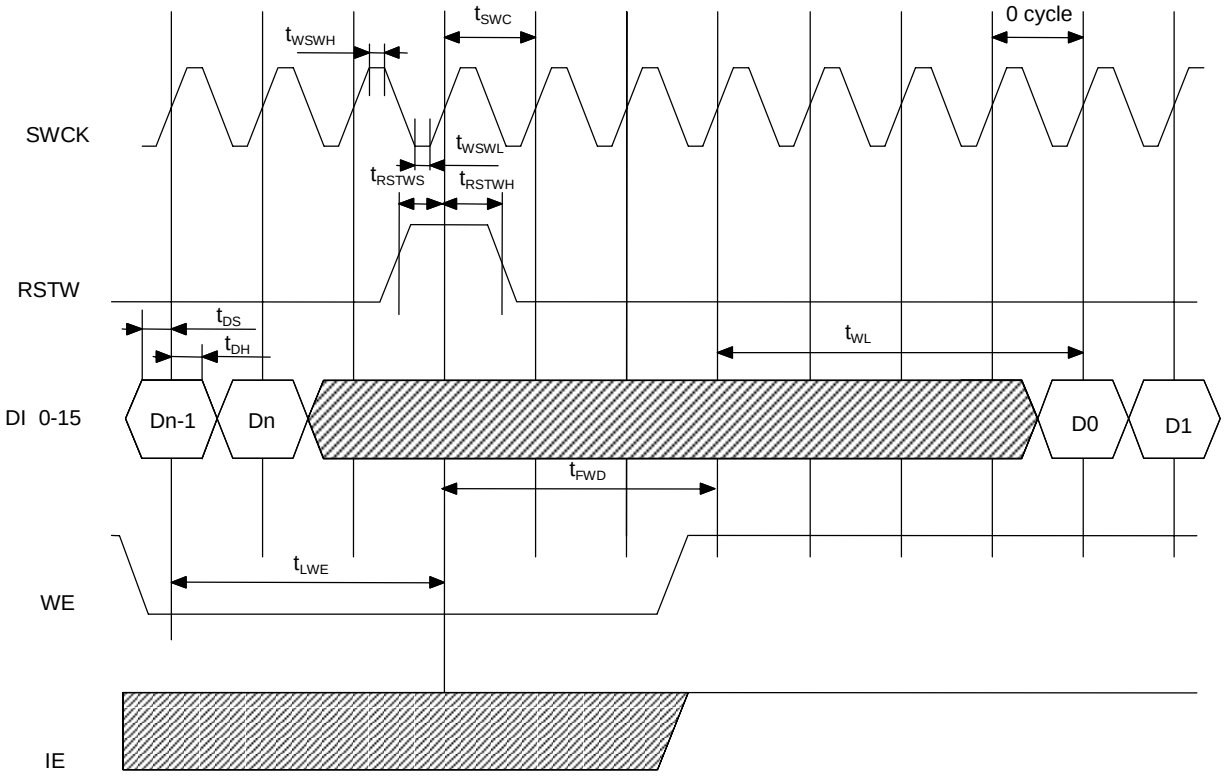
There must be a minimum delay of 600 SWCK cycles between writing into memory and reading out from memory. If reading from the first field starts with an RSTR operation, before the start of writing the second field (before the next RSTW operation), then the data just written will be read out.

The start of reading out the first field of data may be delayed past the beginning of writing in the second field of data for as many as 70 SWCK cycles. If the RSTR operation for the first field read-out occurs less than 70 SWCK cycles after the RSTW operation for the second field write-in, then the internal buffering of the device assures that the first field will still be read out. The first field of data that is read out while the second field of data is written is called “old data”. In order to read out “new data”, i.e., the second field written in, read reset must be input after write address 200 the delay between an RSTW operation and an RSTR operation must be at least 600 SRCK cycles. If the delay between RSTW and RSTR operations is more than 71 but less than 600 cycles, then the data read out will be undetermined. It may be “old data” or “new” data, or a combination of old and new data. Such a timing should be avoided.

When the read address delay is between more than 71 and less than 599 or more than 401,408, read data will be undetermined. However, normal write is achieved in this address codition.

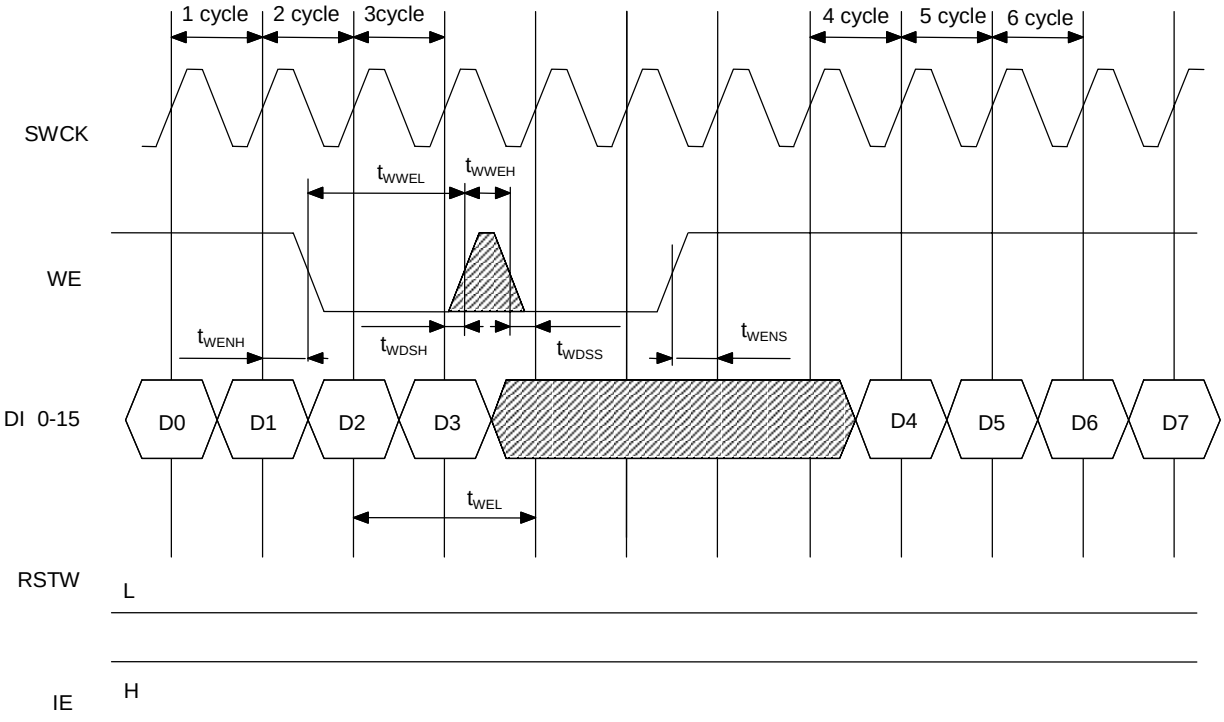
TIMING DIAGRAM

Write Cycle Timing (Write Reset)

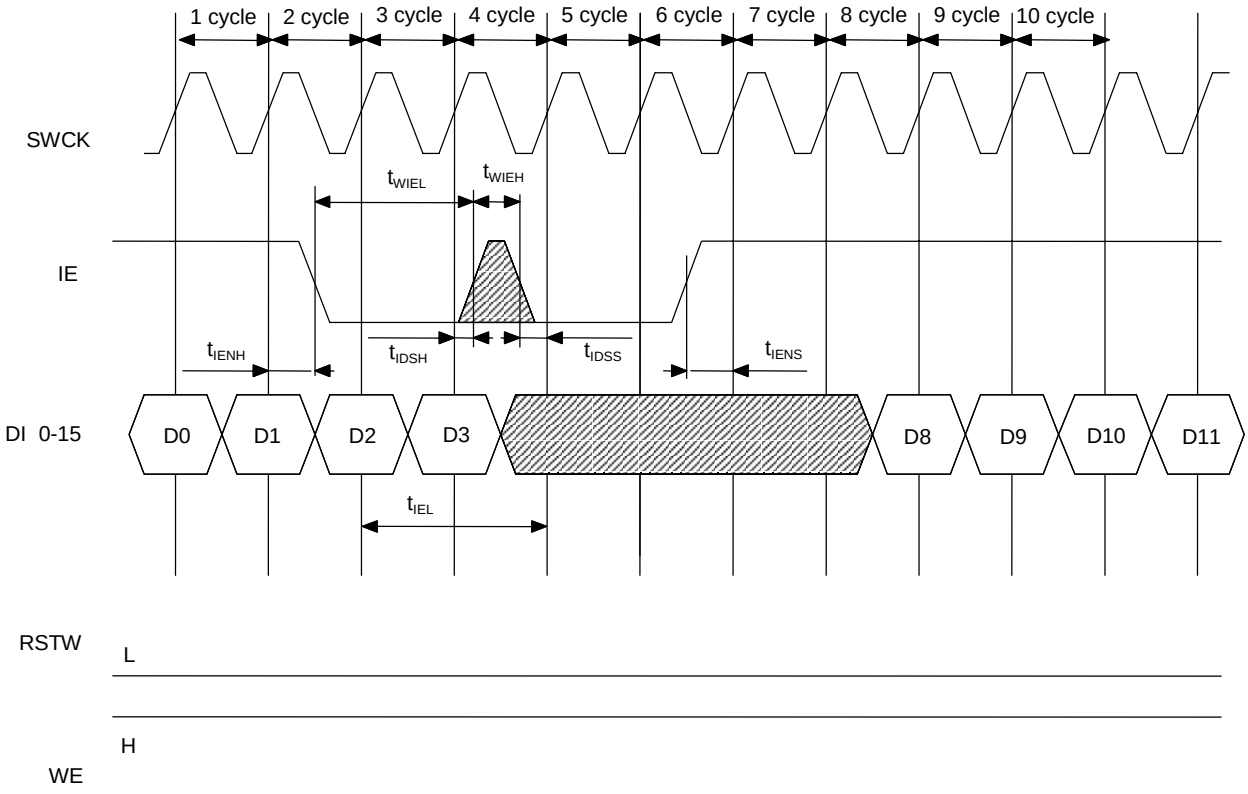


*After write reset, WE should be remained high for 2 cycles after driving WE high first.

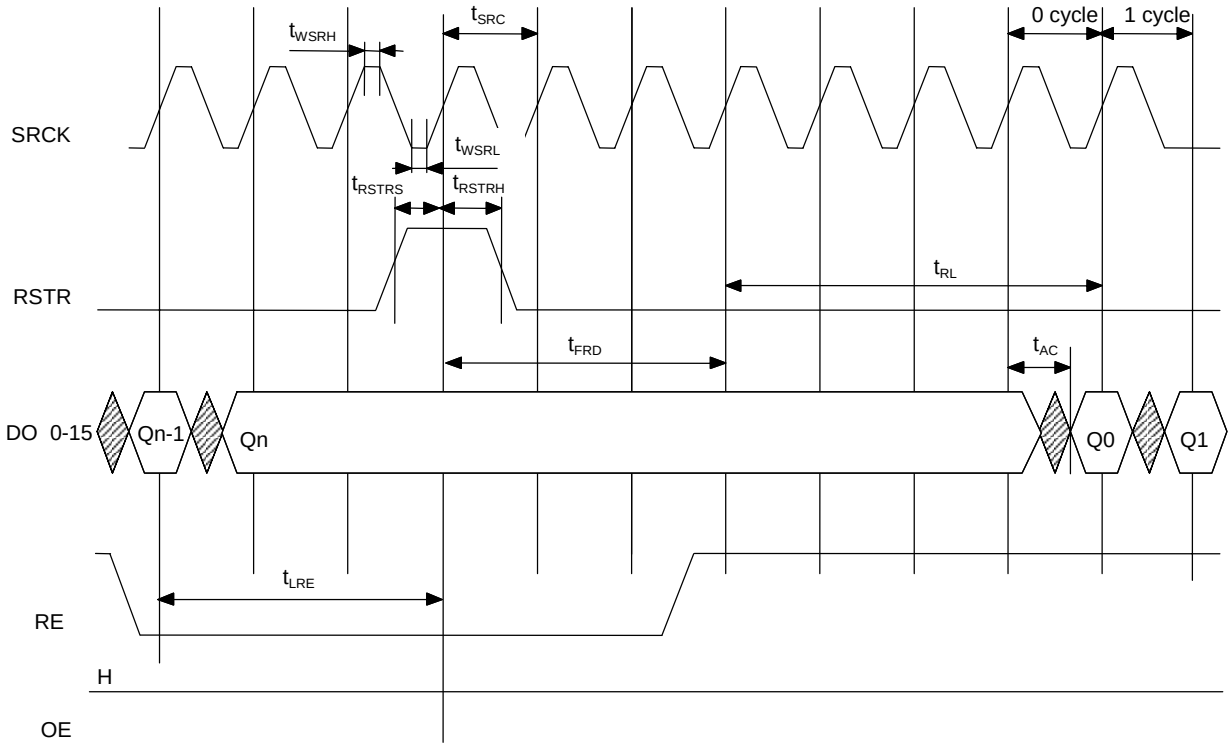
Write Cycle Timing (Write Enable)



Write Cycle Timing (Input Enable)

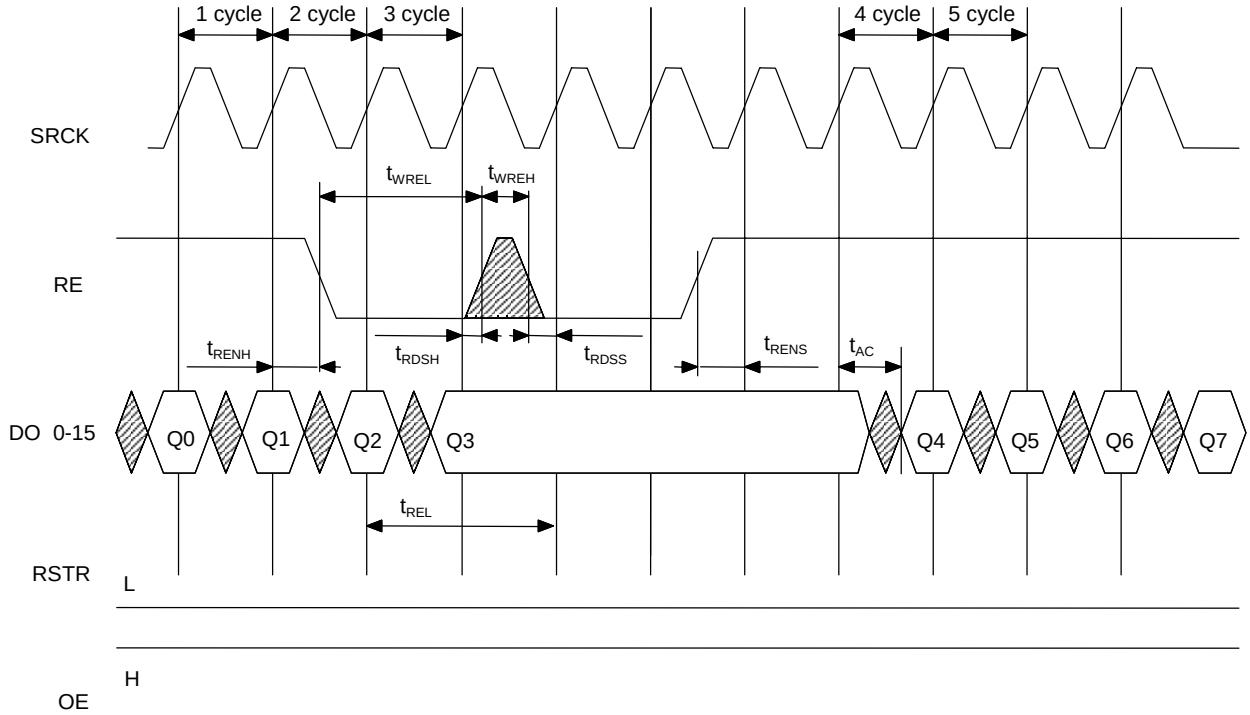


Read Cycle Timing (Read Reset)

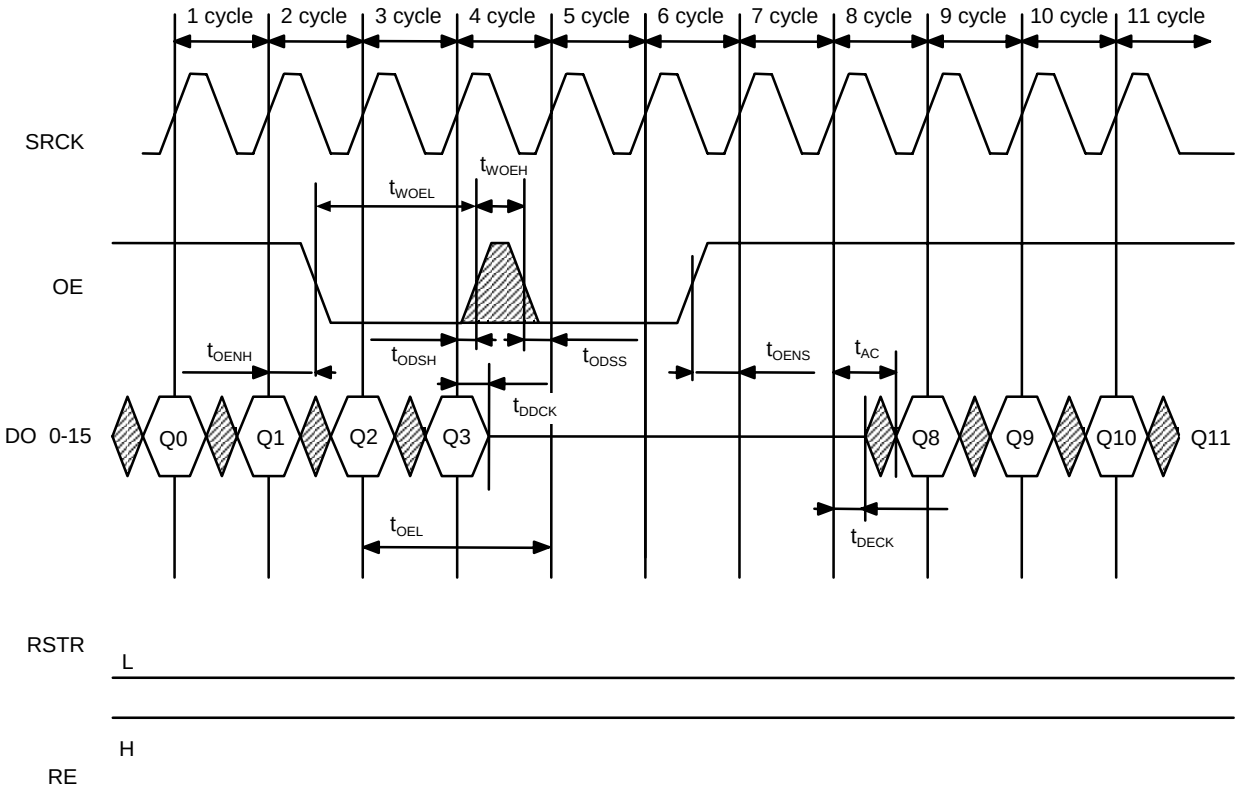


*After write reset, RE should be remained high for 2 cycles after driving RE high first.

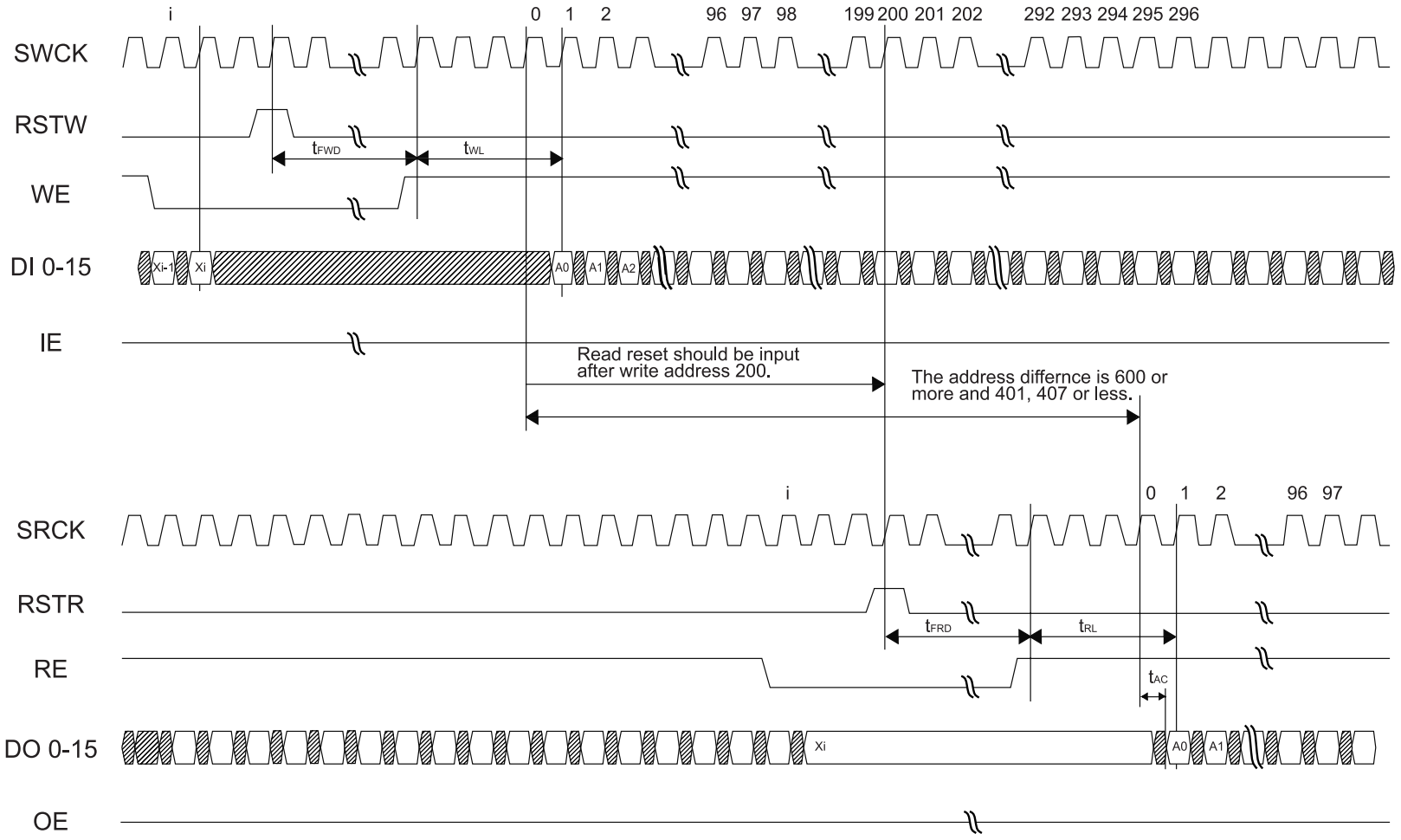
Read Cycle Timing (Read Enable)



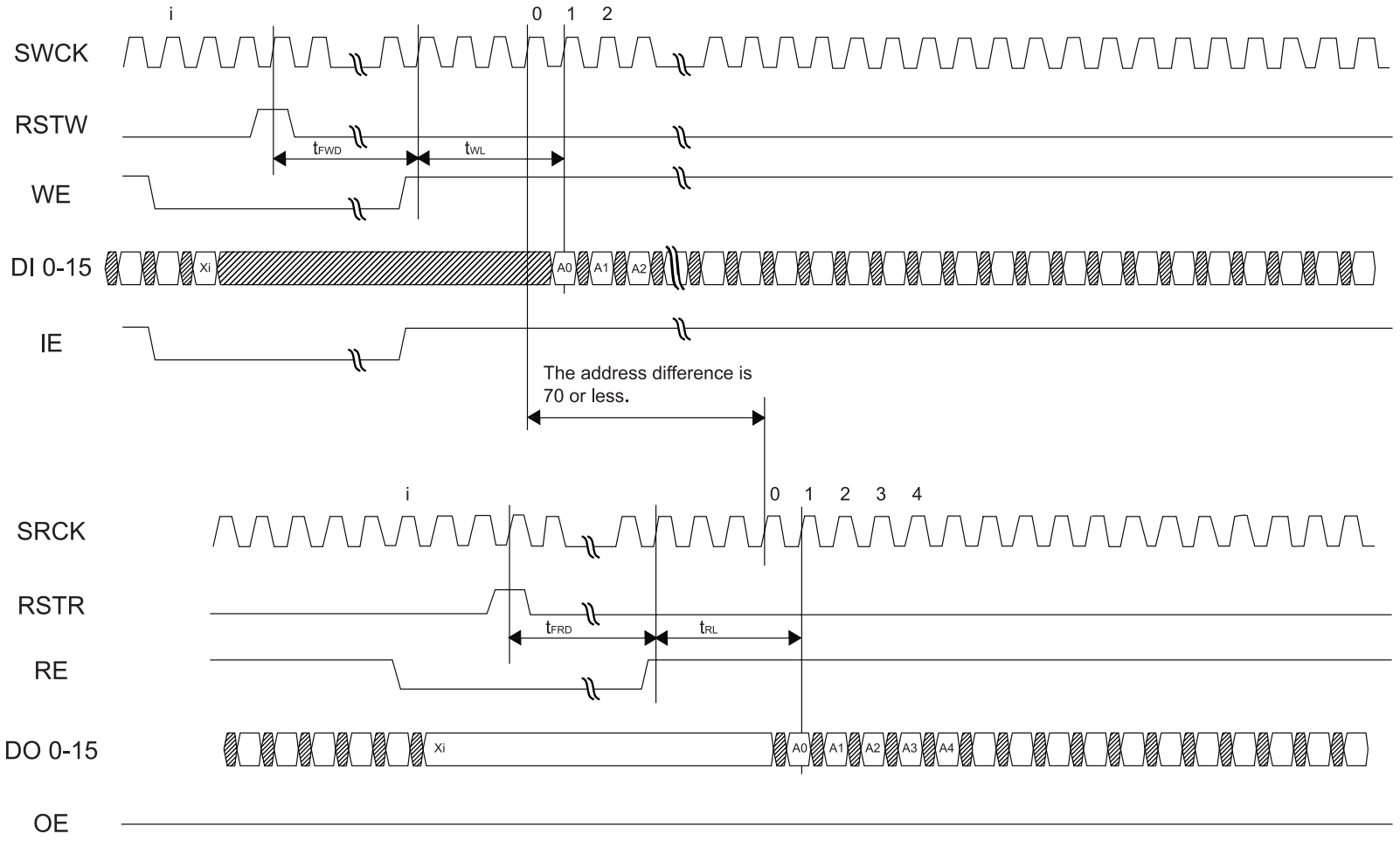
Read Cycle Timing (Output Enable)



Read/Write Cycle Timing (New Data Read)



Read/Write Cycle Timing (Old Data Read)



Read/Write Cycle Timing