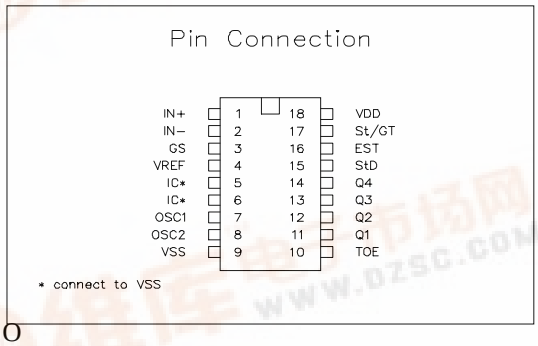
MOSA ELECTRONICS

MS8870
DTMF Receiver

Features

- Complete DTMF receiver
- Low power consumption
- Adjustable guard time
- Central Office Quality
- CMOS, Single 5V operation



Ordering Information
MS8870 : 18 PIN DIP PACKAGE

Description

The MS8870 is a complete DTMF receiver integrating both the bandsplit filter and digital decoder functions, fabricated in double poly technology and is pin and function compatible with MITEL8870. The filter section uses switched capacitor techniques for high and low group filters; the decoder uses digital counting techniques to detect and decode all 16 DTMF tone-pairs into a 4-bit code. External component count is minimized by on chip provision of a differential input amplifier, clock oscillator and latched 3-state bus interface.

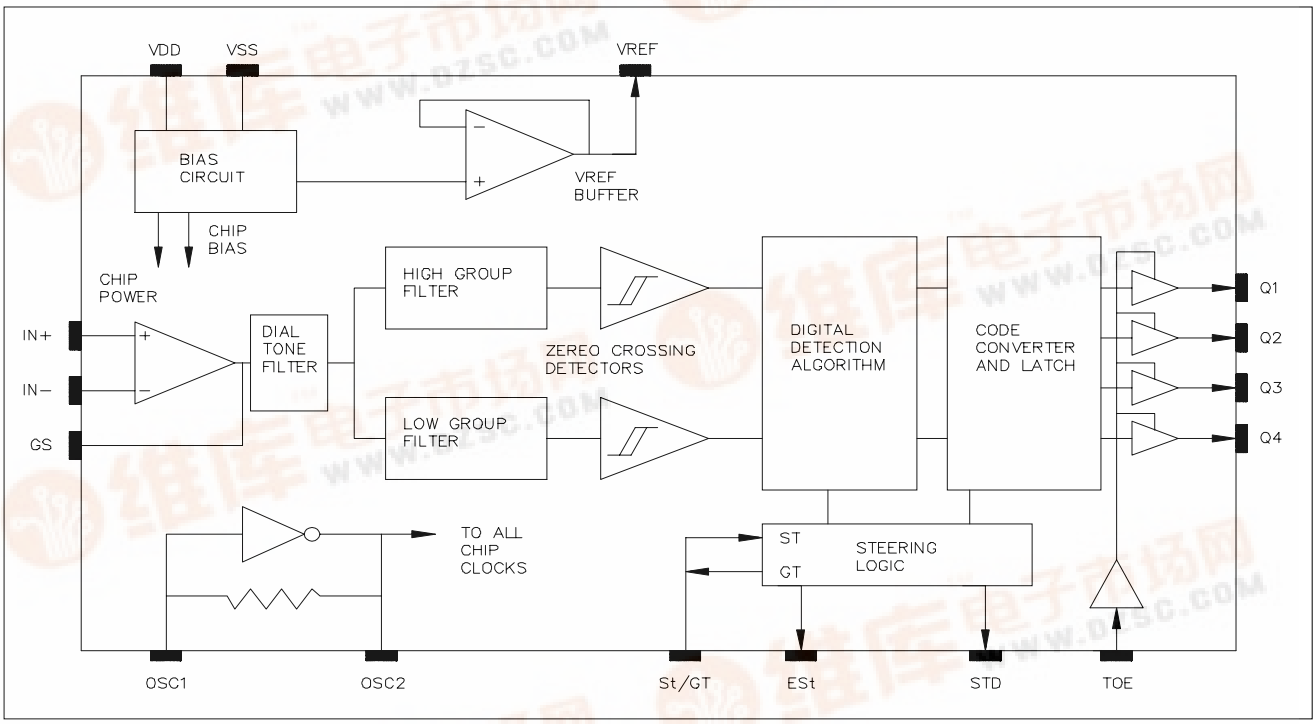


Figure 1. Functional Block Diagram

Pin Description

Pin #	Name	Description
1	IN +	Non-inverting op-amp input.
2	IN -	Inverting op-amp input.
3	GS	Gain select. Gives access to output of front end differential amplifier for connection of feedback resistor.
4	V_{REF}	Reference voltage output, nominally V_{DD} /2 is used to bias inputs at mid-rail (see Fig. 2).
5	IC	Internal connection. Must be tied to Vss.
6	IC	Internal connection. Must be tied to Vss.
7	OSC1	Clock input.
8	OSC2	Clock output. A 3.5795 MHz crystal connected between OSC1 and OSC2 completes the internal oscillator circuit.
9	Vss	Negative power supply input.
10	TOE	3-state output enable (input). Logic high enables the outputs Q1-Q4 Internal pull up.
11-14	Q1-Q4	3-state data output. When enable by TOE, provide the code corresponding to the last valid tone-pair received (see Fig. 5).
15	StD	Delayed steering output. Presents a logic high when a received tone-pair has been registered and the output latch updated; return to logic low when the voltage on St/GT falls below V_{TSt}.
16	ESt	Early steering output. Presents a logic high once the digital algorithm has detected a valid tone pair (signal condition). Any momentary loss of signal condition will cause ESt to return to a logic low.
17	St/GT	Steering input/guard time output (bi-directional). A voltage greater than V_{TSt} detected at St causes the device to register the detected tone pair and update the output latch. A Voltage less than V_{TSt} frees the device to accept a new tone pair. The GT output acts to reset the external steering time-constant; its state is a function of ESt and the voltage on St.
18	V_{DD}	Positive power supply input.

Absolute Maximum Ratings

	Parameter	Min	Max	Units
1	Power supply voltage V_{DD}-Vss		6	V
2	Voltage on any pin	Vss - 0.3	V_{DD} + 0.3	V
3	Current at any pin		10	mA
4	Operating temperature	-40	+85	℃
5	Storage temperature	-65	+150	℃
6	Package power dissipation		1000	mW

DC Electrical Characteristics

		Characteristics	Sym	Min	Typ	Max	Units	Test Conditions
1	SUPPLY	Operating supply voltage		4.75	5.0	5.25	V	
2		Operating supply current	I_{DD}		3.0	9.0	mA	
3		Power consumption	P_O		15	45	mW	f = 3.58 MHz; V_{DD}= 5V
4	INPUTS	High level input	V_{IH}	3.5			V	
5		Low level input voltage	V_{IL}			1.5	V	
6		Input leakage current	I_{IH}/I_{IL}		0.1		μA	V_{IN} = Vss or V_{DD}
7		Pull up (source) current	I_{SO}		7.5		μA	TOE (pin 10) = 0 V
8		Input impedance (IN+, IN-)	R_{IN}		10		MΩ	@ 1 KHz
9		Steering threshold voltage	V_{TSt}	2.2		2.5	V	
10	OUTPUTS	Low level output voltage	V_{OL}			0.03	V	No load
11		High level output voltage	V_{OH}	4.97			V	No load
12		Output low (sink) current	I_{OL}	1	2.5		mA	V_{OUT} = 0.4V
13		Output high (source) current	I_{OH}	0.4	0.8		mA	V_{OUT} = 4.6V
14		V_{Ref} output voltage	V_{Ref}	2.4		2.8	V	No load
15		V_{Ref} output resistance	R_{OR}		10		KΩ	

Operating Characteristics
Gain Setting Amplifier

Characteristics	Sym	Min	Typ	Max	Units	Test Conditions
Input leakage current	I_{IN}		100		nA	$V_{SS} \leq V_{IN} \leq V_{DD}$
Input resistance	R_{IN}		10		MΩ	
Input offset voltage	Vos		25		mV	
Power supply rejection	PSRR		60		dB	1 KHz
Common mode rejection	CMRR		60		dB	$-3.0V \leq V_{IN} \leq 3.0V$
DC open loop voltage gain	A_{VOL}		65		dB	
Open loop unity gain bandwidth	fc		1.5		MHz	
Output voltage swing	Vo		4.5		Vpp	$R_L \geq 100K\Omega$ to Vss
Maximum capacitive load (GS)	C_L		100		pF	
Maximum resistive load (GS)	R_L		50		KΩ	
Common mode range	V_{CM}		3.0		Vpp	No Load

Notes : 1. All voltages referenced to Vss unless otherwise noted.
2. V_{CC} = 5.0V, Vss = 0V, T_A = 25 ℃

AC Electrical Characteristics *

	Characteristics	Sym	Min	Typ	Max	Units	Notes
S			-29			dBm	1,2,3,5,6,9
I	Valid input signal levels		27.5			mVRMS	1,2,3,5,6,9
G	(each tone of composite signal)				+1	dBm	1,2,3,5,6,9
N					883	mVRMS	1,2,3,5,6,9
A	Positive twist accept			10		dB	2,3,6,9
L	Negative twist accept			10		dB	2,3,6,9
	Freq. deviation accept		±1.5%±2Hz			Nom.	2,3,5,9
C	Freq. deviation reject		±3.5%			Nom.	2,3,5,9
O	Third tone tolerance			-16		dB	2,3,4,5,9,10
N	Noise tolerance			-12		dB	2,3,4,5,7,9,10
D.	Dial tone tolerance			+22		dB	2,3,4,5,8,9,11
T	Tone present detect time	t_{DP}	5	11	14	ms	Refer to Fig. 3
I	Tone absent detect time	t_{DA}	0.5	4	8.5	ms	Refer to Fig. 3
M	Tone duration accept	t_{REC}			40	ms	User adjustable
I	Tone duration reject	$/t_{REC}$	20			ms	User adjustable
N	Interdigit pause accept	t_{ID}			40	ms	User adjustable
G	Interdigit pause reject	t_{DO}	20			ms	User adjustable
O	Propagation delay (St to Q)	t_{PQ}		8	11	μs	TOE = VDD
U	Propagation delay (St to StD)	t_{PStD}		12		μs	TOE = VDD
T	Output data set up (Q to StD)	t_{QStD}		3.4		μs	TOE = VDD
P	Propagation delay (TOE to Q	t_{PTE}		50		ns	RL = 10KΩ
U	ENABLE)						CL = 50 pF
T	Propagation delay (TOE to Q	t_{PTD}		300		ns	RL = 10KΩ
S	DISABLE)						CL = 50 pF
C	Crystal / clock frequency	fc	3.5759	3.5795	3.5831	MHz	
L	Clock input rise time	t_{LHCL}			110	ns	Ext. clock
O	Clock input fall time	t_{HLCL}			110	ns	Ext. clock
C	Clock input duty cycle	DC_{DL}	40	50	60	%	Ext. clock
K	Capacitive load (OSC2)	C_{LO}			30	pF	

* All voltages referenced to Vss unless otherwise noted. Vcc = 5.0V, Vss = 0V, T_A = 25℃, Fc = 3.579545 MHz, using test circuit shown in Figure 2

NOTES

1. dBm = decibels above or below a reference power of 1 mW into a 600 ohm load.
2. Digit sequence consists of all 16 DTMF tones.
3. Tone duration = 40 ms, tone pause = 40 ms.
4. Signal condition consists of nominal DTMF frequencies.
5. Both tones in composite signal have an equal amplitude.
6. Tone pair is deviated by ± 1.5% ± 2 Hz.
7. Bandwidth limited (3 KHz) Gaussian noise.
8. The precise dial tone frequencies are (350 Hz and 440 Hz) ± 2%.
9. For an error rate of better than 1 in 10,000.
10. Referenced to lowest level frequency component in DTMF signal.
11. Referenced to the minimum valid accept level.

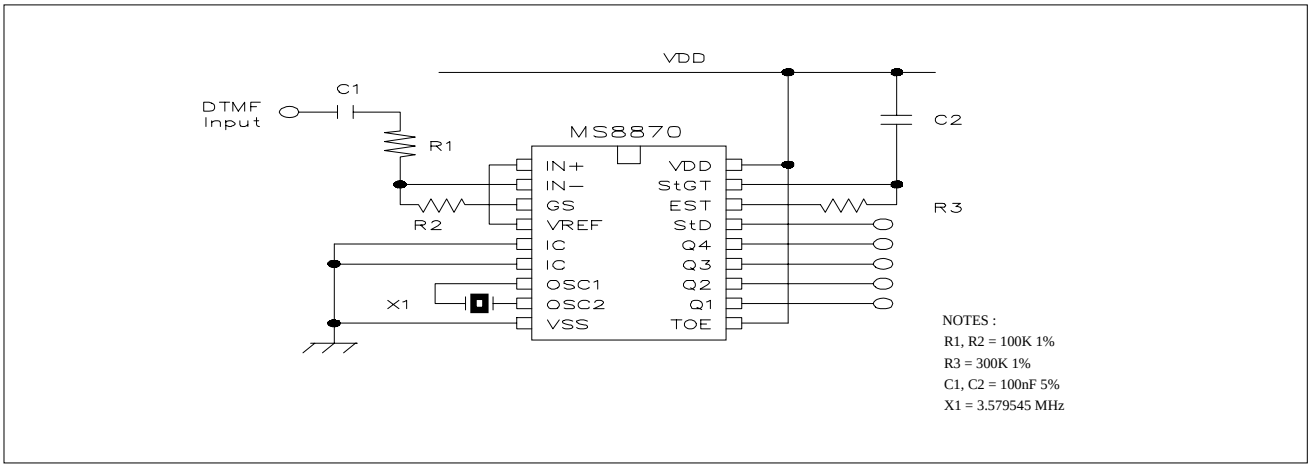


Figure 2. Single Ended Input Configuration

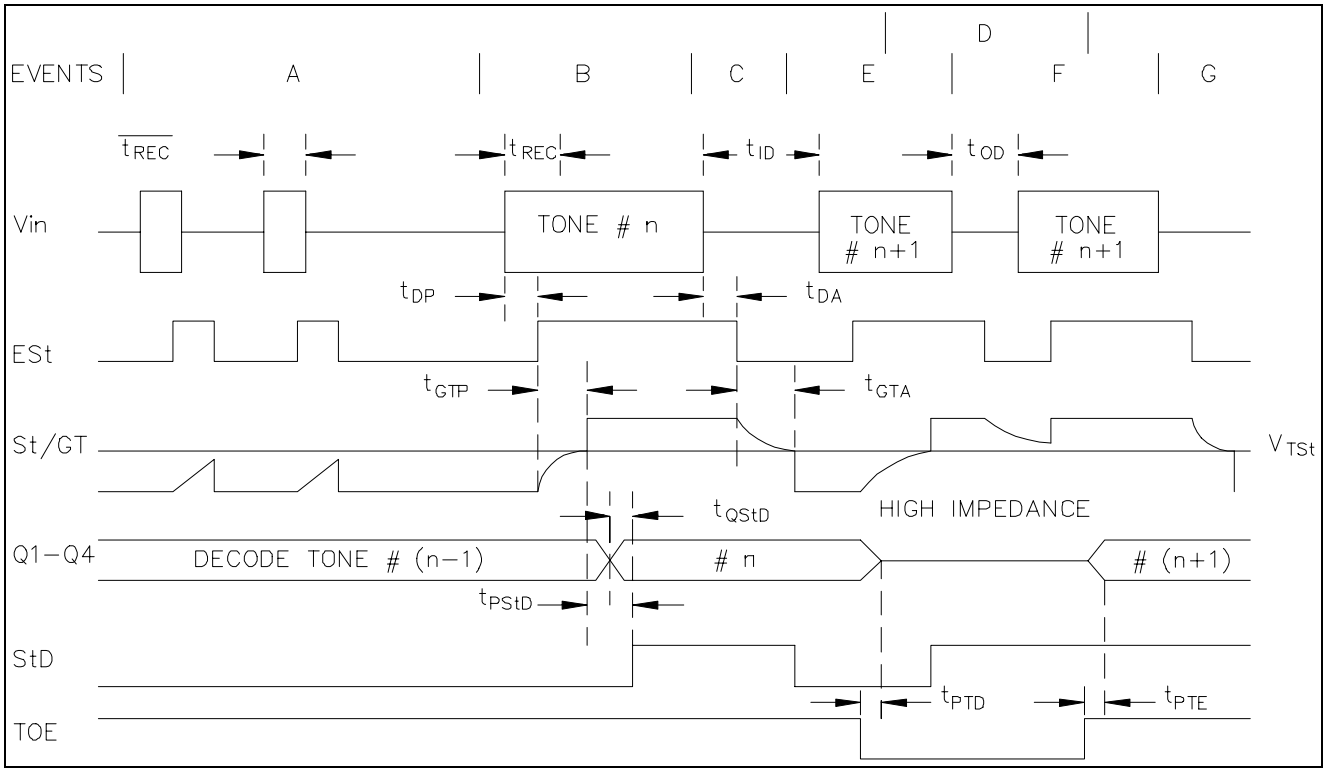


Figure 3. Timing Diagram

EXPLANATION OF EVENTS

A) Short tone bursts: detected. Tone duration is invalid.

B) Tone #n is detected. Tone duration is valid. Decoded to outputs.

C) End of Tone #n is detected and validated.

D) 3-State outputs disable (high impedance).

E) Tone #n + 1 is detected. Tone duration is valid. Decoded to outputs.

F) Tristate outputs are enabled. Acceptable drop out of Tone #n + 1 does not register at outputs.

G) End of Tone #n + 1 is detected and validated.

Functional Description

The MS8870 monolithic DTMF receiver offers small size, low power consumption and high performance. Its architecture consists of a bandsplit filter section, which separates the high and low group tones, followed by digital counting section which verifies the frequency and duration of the received tones before passing the corresponding code to the output bus.

Filter Section

Separation of the low-group and high-group tones is achieved by applying the DTMF signal to the inputs of two filters — a sixth order for the high group and an eighth order for the low group. The bandwidths of which correspond to the low and high group frequencies. The filter section also incorporates notches at 350 and 440 Hz for exceptional dial tone rejection (see Fig. 4). Each filter output is followed by a single order switched capacitor filter section which smoothes the signals prior to limiting. Limiting is performed by high-gain comparators which are provided with hysteresis to prevent detection of unwanted low-level signals. The outputs of the comparators provide full rail logic swings at the frequencies of the incoming DTMF signals.

Decoder Section

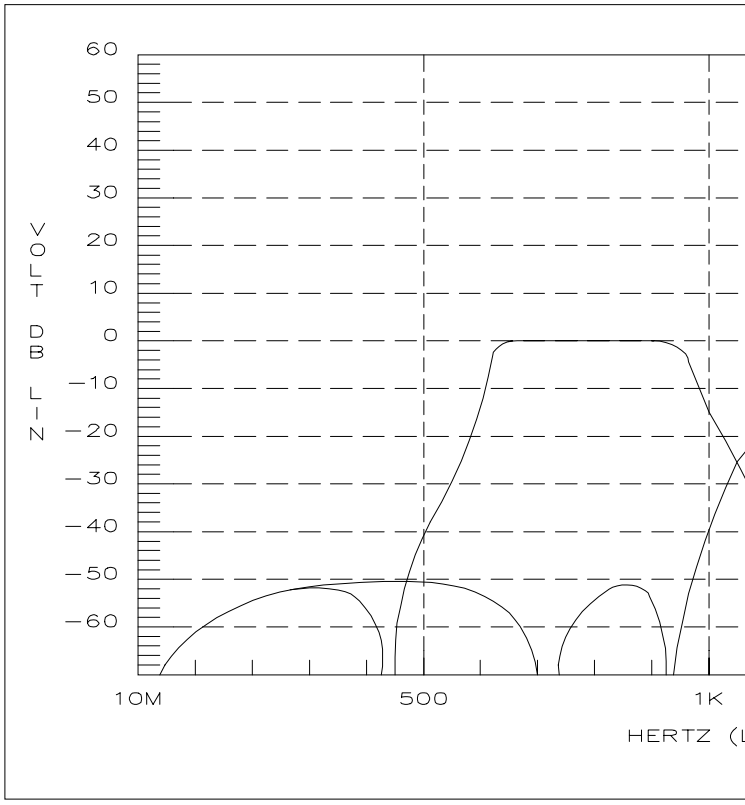


Figure 4. 6TH Order Bandpass

The decoder uses digital counting techniques to determine the frequencies of limited tones and to verify that they correspond to standard DTMF frequencies. A complex averaging algorithm protects against tone simulation by extraneous signals, such as voice, while providing tolerance to small frequency deviations and variations. This averaging algorithm has been developed to ensure an optimum combination of immunity to "talk-off" and tolerance to the presence of interfering signals ("third tones") and noise. When the detector recognizes the simultaneous presence of two valid tone (referred to as "signal condition" in some industry specifications), it raises the "early steering" flag (ESt). Any subsequent loss of signal-condition will cause ESt to fall.

FLOW	FHIGH	NO	TOE	Q4	Q3	Q2	Q1
697	1209	1	H	0	0	0	1
697	1336	2	H	0	0	1	0
697	1477	3	H	0	0	1	1
770	1209	4	H	0	1	0	0
770	1336	5	H	0	1	0	1
770	1477	6	H	0	1	1	0
852	1209	7	H	0	1	1	1
852	1336	8	H	1	0	0	0
852	1477	9	H	1	0	0	1
941	1336	0	H	1	0	1	0
941	1209	*	H	1	0	1	1
941	1477	#	H	1	1	0	0
697	1633	A	H	1	1	0	1
770	1633	B	H	1	1	1	0

852	1633	C	H	1	1	1	1
941	1633	D	H	0	0	0	0
		ANY	L	Z	Z	Z	Z

L = LOGIC LOW, H = LOGIC HIGH, Z = HIGH IMPEDANCE

Figure 5. Functional Decode Table

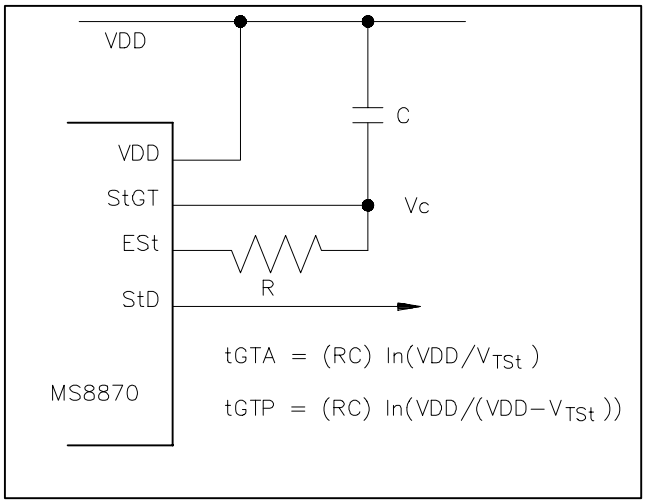


Figure 6. Basic Steering Circuit

Steering Circuit

Before registration of a decoded tone pair, the receiver checks for a valid signal duration (referred to as character recognition condition). This check is performed by an external RC time constant driven by ESt. A logic high on ESt causes Vc (see Fig. 6) to rise as the capacitor discharges.

Provided signal condition is maintained (ESt remains high) for the validation period (t_{GTP}), Vc reaches the threshold (V_{TSt}) of the steering logic to register the tone pair, latching its corresponding 4-bit code (see Fig. 5) into the output latch. At this point the GT output is activated and drives Vc to VDD. GT continues to drive high as long as ESt remains high. Finally, after a short delay to allow the output latch to settle, the delayed steering output flag (StD) goes high, signaling that a received tone pair has been registered. The contents of the output latch are made available on the 4-bit output bus by raising the three state control input (TOE) to a logic high. The steering circuit works in reverse to validate the interdigit pause between signals. Thus, as well as rejecting signals too short to be considered valid, the receiver will tolerate signal interruptions (drop out) too short to be considered a valid pause. This facility, together with the capability of selecting the steering time constants externally, allows the designer to tailor performance to meet a wide variety of system requirements.

Guard Time Adjustment

In many situations not requiring selection of tone duration and interdigital pause, the simple steering circuit shown in Fig. 6 is applicable. Component values are chosen according to the formula : $t_{REC} = t_{PD} + t_{GPT}$

$t_{ID} = t_{DA} + t_{GTA}$

The value of t_{DP} is a device parameter (see table) and t_{REC} is the minimum signal duration to be recognized by the receiver. A value for C of 0.1 μF is recommended for most applications, leaving R to be selected by the designer.

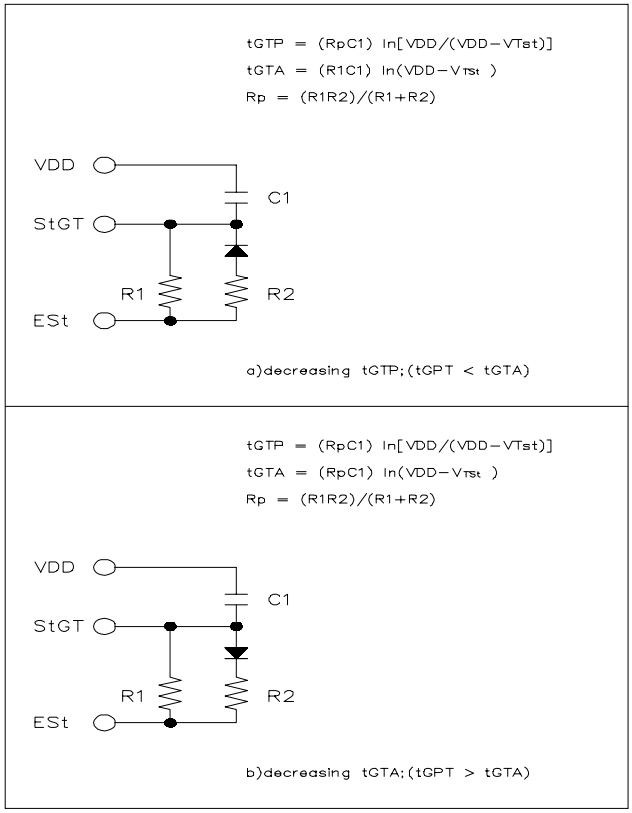
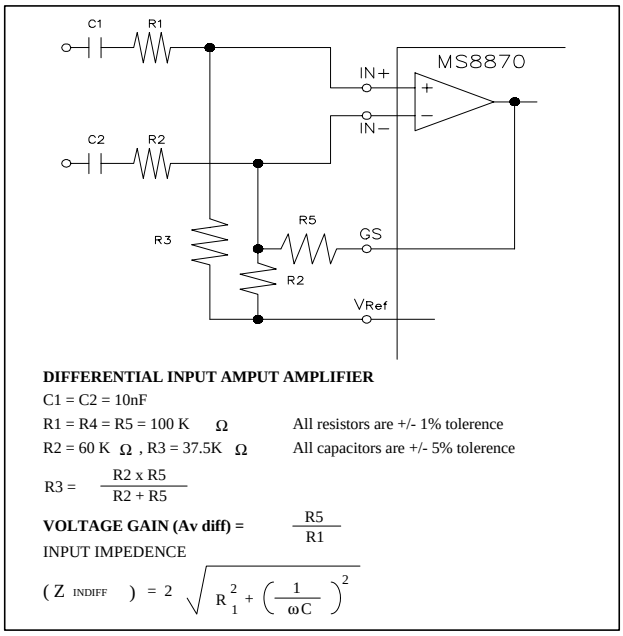


Figure 7. Guard Time Adjustment

Different steering arrangements may be used to select independently the guard times for tone present (t_{GTP}) and tone absent (t_{GTA}). This may be necessary to meet system specifications which place both accept and reject limits on both tone duration and interdigital pause. Guard time adjustment also allows the designer to tailor system parameters such as talk off and noise immunity. Increasing t_{REC} improves talk-off performance since it reduces the probability that tones simulated by speech will maintain signal condition long enough to be registered. Alternatively, a relatively short tREC with noisy environments where fast acquisition time and immunity to tone drop-outs are required. Design information for guard time adjustment is shown in Figure 7.

Differential Input Configuration



DIFFERENTIAL INPUT AMPUT AMPLIFIER

C1 = C2 = 10nF

R1 = R4 = R5 = 100 K Ω — All resistors are +/- 1% tolerence

R2 = 60 K Ω , R3 = 37.5K Ω — All capacitors are +/- 5% tolerence

$$R3 = \frac{R2 \times R5}{R2 + R5}$$

VOLTAGE GAIN (Av diff) = $\frac{R5}{R1}$

INPUT IMPEDENCE

$$(Z_{INDIFF}) = 2\sqrt{R_1^2 + \left(\frac{1}{\omega C}\right)^2}$$

Figure 8. Differential Input Configuration

The input arrangement of the MS8870 provides a differential-input operational amplifier as well as a bias source (V_{Ref}) which is used to bias the inputs at mid-rail. Provision is made for connection of a feedback resistor to the op-amp output (GS) for adjustment of gain. In a single-ended configuration, the input pins are connected as shown in Fig. 2 with the op-amp connected for unity gain and V_{Ref} biasing the input at ½ V_{DD}. Fig. 8 shows the differential configuration, which permits the adjustment of gain with the feedback resistor R_5.