

Cascadable Silicon Bipolar MMIC Amplifier

Technical Data

MSA-0300

Features

- **Cascadable 50 Ω Gain Block**
- **3 dB Bandwidth:**
DC to 2.8 GHz
- **12.0 dB Typical Gain at
1.0 GHz**
- **10.0 dBm Typical $P_{1\text{ dB}}$ at
1.0 GHz**

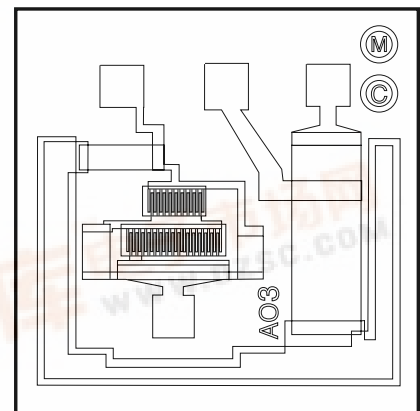
Description

The MSA-0300 is a high performance silicon bipolar Monolithic Microwave Integrated Circuit (MMIC) chip. This MMIC is designed for use as a general purpose 50 Ω gain block. Typical applications include narrow and broad band IF and RF amplifiers in commercial, industrial and military applications.

The MSA-series is fabricated using HP's 10 GHz f_T , 25 GHz f_{MAX} , silicon bipolar MMIC process which uses nitride self-alignment, ion implantation, and gold metallization to achieve excellent performance, uniformity and reliability. The use of an external bias resistor for temperature and current stability also allows bias flexibility.

The recommended assembly procedure is gold-eutectic die attach at 400°C and either wedge or ball bonding using 0.7 mil gold wire.^[1] See APPLICATIONS section, "Chip Use".

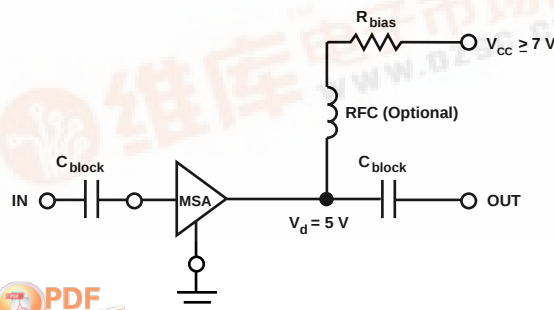
Chip Outline^[1]



Note:

1. This chip contains additional biasing options. The performance specified applies only to the bias option whose bond pads are indicated on the chip outline. Refer to the APPLICATIONS section "Silicon MMIC Chip Use" for additional information.

Typical Biasing Configuration



MSA-0300 Absolute Maximum Ratings

Parameter	Absolute Maximum ^[1]
Device Current	80 mA
Power Dissipation ^[2,3]	425 mW
RF Input Power	+13 dBm
Junction Temperature	200°C
Storage Temperature	–65 to 200°C

Thermal Resistance^[2,4]:

$$\theta_{jc} = 45^{\circ}\text{C/W}$$

Notes:

1. Permanent damage may occur if any of these limits are exceeded.
2. $T_{\text{Mounting Surface}} (T_{\text{MS}}) = 25^{\circ}\text{C}$.
3. Derate at 22.2 mW/°C for $T_{\text{C}} > 181^{\circ}\text{C}$.
4. The small spot size of this technique results in a higher, though more accurate determination of θ_{jc} than do alternate methods. See MEASUREMENTS section “Thermal Resistance” for more information.

Electrical Specifications^[1], $T_{\text{A}} = 25^{\circ}\text{C}$

Symbol	Parameters and Test Conditions ^[2] : $I_{\text{d}} = 35 \text{ mA}$, $Z_{\text{o}} = 50 \Omega$	Units	Min.	Typ.	Max.
G _P	Power Gain ($ S_{21} ^2$) f = 0.1 GHz	dB		12.5	
ΔG_{P}	Gain Flatness f = 0.1 to 1.8 GHz	dB		± 0.6	
f _{3 dB}	3 dB Bandwidth	GHz		2.8	
VSWR	Input VSWR f = 0.1 to 3.0 GHz			1.8:1	
	Output VSWR f = 0.1 to 3.0 GHz			1.8:1	
NF	50 Ω Noise Figure f = 1.0 GHz	dB		6.0	
P _{1 dB}	Output Power at 1 dB Gain Compression f = 1.0 GHz	dBm		10.0	
IP ₃	Third Order Intercept Point f = 1.0 GHz	dBm		23.0	
t _D	Group Delay f = 1.0 GHz	psec		125	
V _d	Device Voltage	V	4.5	5.0	5.5
dV/dT	Device Voltage Temperature Coefficient	mV/°C		–8.0	

Notes:

1. The recommended operating current range for this device is 20 to 50 mA. Typical performance as a function of current is on the following page.
2. RF performance of the chip is determined by packaging and testing 10 devices per wafer in a dual ground configuration.

Part Number Ordering Information

Part Number	Devices Per Tray
MSA-0300-GP4	100

MSA-0300 Typical Scattering Parameters^[1] ($Z_0 = 50\ \Omega$, $T_A = 25^\circ\text{C}$, $I_d = 35\ \text{mA}$)

Freq. GHz	S ₁₁		S ₂₁			S ₁₂			S ₂₂		k
	Mag	Ang	dB	Mag	Ang	dB	Mag	Ang	Mag	Ang	
0.1	.13	-179	12.6	4.28	177	-18.6	.118	2	.09	-13	1.21
0.2	.13	-179	12.6	4.27	172	-18.3	.121	3	.10	-27	1.19
0.4	.12	-179	12.5	4.24	165	-18.3	.121	5	.12	-48	1.19
0.6	.11	-177	12.5	4.22	158	-18.2	.123	8	.14	-65	1.18
0.8	.11	-172	12.4	4.19	152	-17.8	.129	11	.17	-76	1.15
1.0	.10	-166	12.4	4.15	144	-17.7	.130	1	.20	-85	1.14
1.5	.11	-145	12.0	4.00	126	-17.1	.139	1	.24	-104	1.09
2.0	.16	-140	11.5	3.76	109	-16.2	.154	2	.27	-122	1.03
2.5	.23	-141	10.8	3.47	97	-15.6	.166	2	.28	-133	0.99
3.0	.29	-149	9.8	3.10	82	-15.2	.173	24	.28	-145	0.99
3.5	.35	-157	8.7	2.72	67	-14.5	.188	21	.27	-148	0.97
4.0	.38	-164	7.6	2.40	55	-14.3	.193	22	.25	-146	1.00
5.0	.41	179	5.5	1.88	35	-13.7	.206	17	.21	-134	1.14
6.0	.43	153	3.6	1.51	18	-13.3	.217	14	.21	-137	1.27

Note:

- S-parameters are de-embedded from 70 mil package measured data using the package model found in the DEVICE MODELS section.

Typical Performance, $T_A = 25^\circ\text{C}$

(unless otherwise noted)

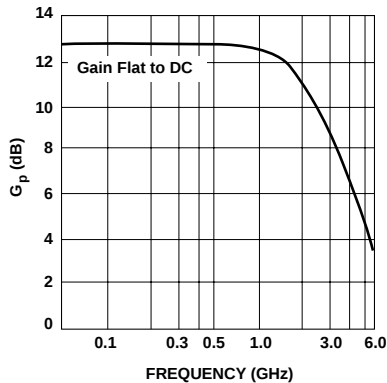


Figure 1. Typical Power Gain vs. Frequency, $T_A = 25^\circ\text{C}$, $I_d = 35\ \text{mA}$.

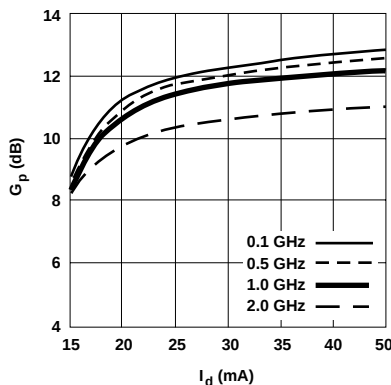


Figure 2. Power Gain vs. Current.

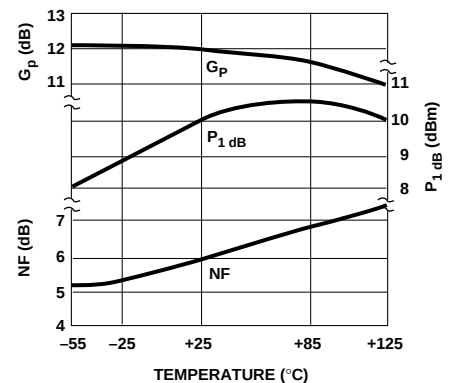


Figure 3. Output Power at 1 dB Gain Compression, NF and Power Gain vs. Mounting Surface Temperature, $f = 1.0\ \text{GHz}$, $I_d = 35\ \text{mA}$.

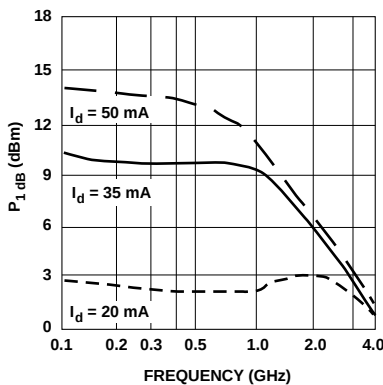


Figure 4. Output Power at 1 dB Gain Compression vs. Frequency.

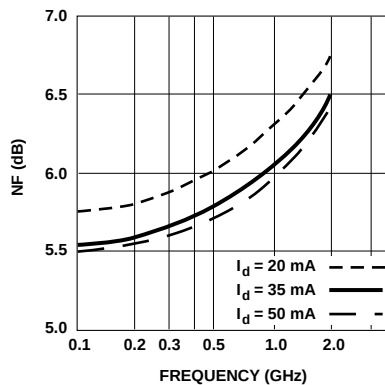


Figure 5. Noise Figure vs. Frequency.

Diagram illustrating the top view of the AO3 package, showing dimensions and pin locations:

- Dimensions:**
 - Width: 365 μm (14.4 mil)
 - Height: 365 μm (14.4 mil)
- Pin Locations:**
 - INPUT:** Pin 1 (left side)
 - GROUND:** Pin 2 (bottom left)
 - OPTIONAL OUTPUT^[1]:** Pin 3 (bottom right)
 - NOT APPLICABLE:** Pins 4 and 5 (top center)
 - M:** Pin 6 (top right)
 - C:** Pin 7 (bottom right)

Unless otherwise specified, tolerances are $\pm 13\text{ }\mu\text{m}/\pm 0.5\text{ mils}$. Chip thickness is $5.5 \pm 0.5\text{ mils}$. Bond Pads are $41\text{ }\mu\text{m}/1.6\text{ mil}$ typical on each side. Note 1: Output contact is made by die attaching the backside of the die.