E2C0018-27-Y3

This version: Nov. 1997
Previous version: Jul. 1996

OKI Semiconductor

MSC1205

32-Bit Duplex Controller/Driver with Digital Dimming Function

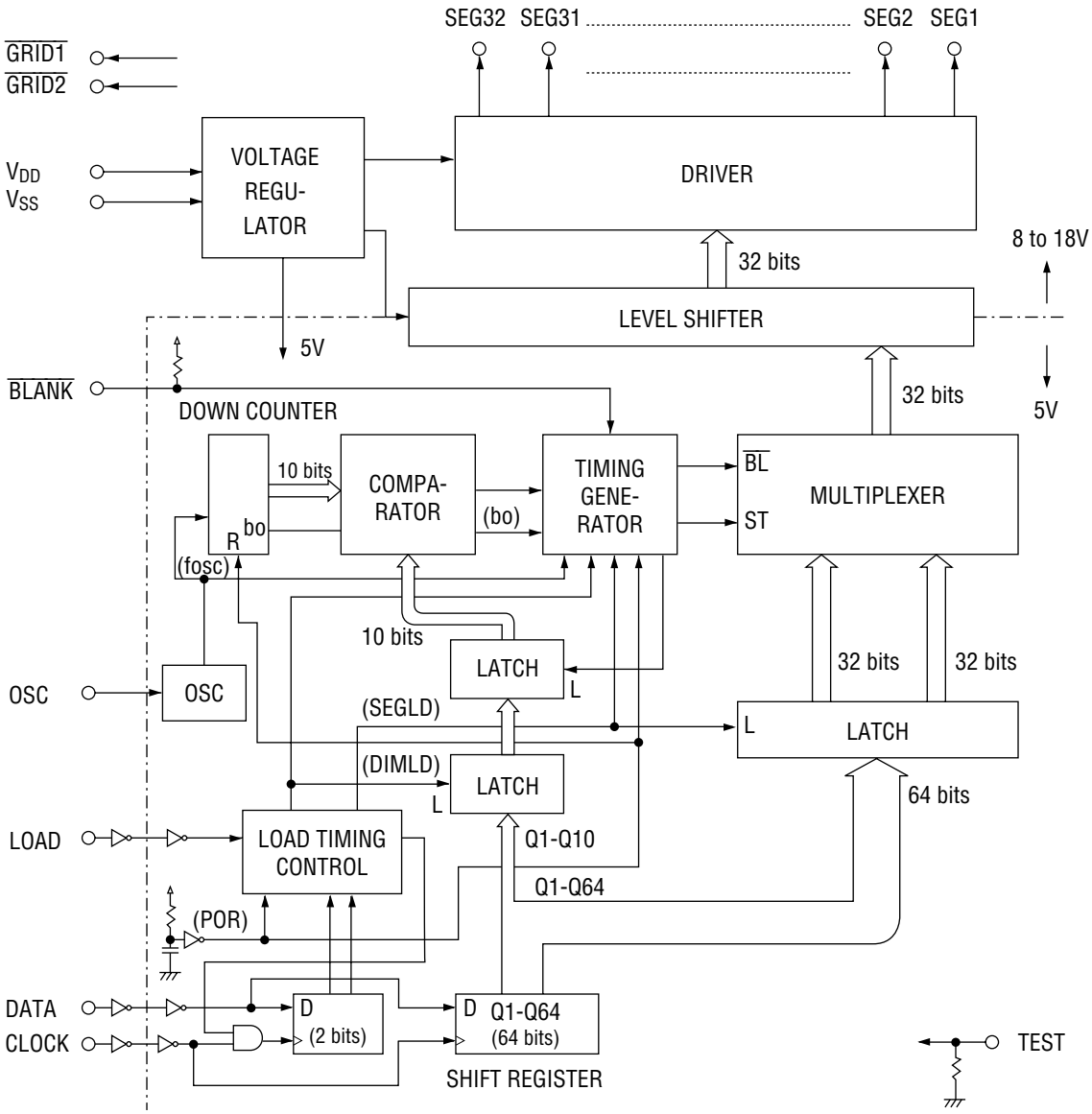
GENERAL DESCRIPTION

The MSC1205 is a Bi-CMOS display driver for a 1/2-duty vacuum fluorescent display tube. It consists of a 64-bit shift register, latch circuits, a digital diming circuit, and drivers.
The MSC1205 provides an interface with a microcomputer only by three signal lines: LOAD, DATA, and CLOCK.

FEATURES

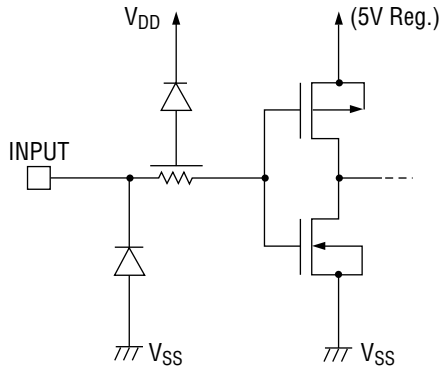
- Power Supply Voltage: 8 to 18V (built-in 5V regulator for logic)
- Built-in 1-terminal RC oscillation circuit (with external capacitor)
- Built-in digital dimming circuit
  10-bit resolution
  Programmable in the duty range of 0/2048 (0%) to 1015.5/2048 (49.6%).
- Can directly drive 32 × 2 display anodes.
- Built-in power-on reset circuit
- Package options:
  42-pin plastic DIP (DIP42-P-600-2.54) (Product name: MSC1205-RS)
  44-pin plastic QFP (QFP44-P-910-0.80-2K) (Product name: MSC1205GS-2K)

BLOCK DIAGRAM

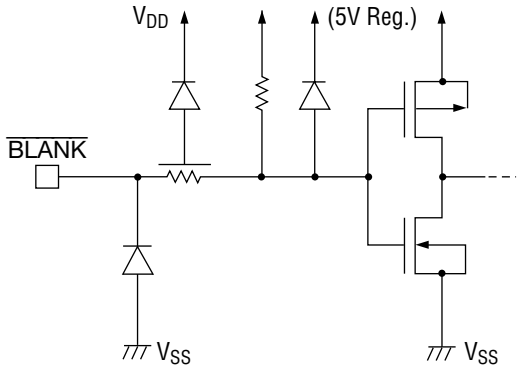


INPUT AND OUTPUT CONFIGURATION

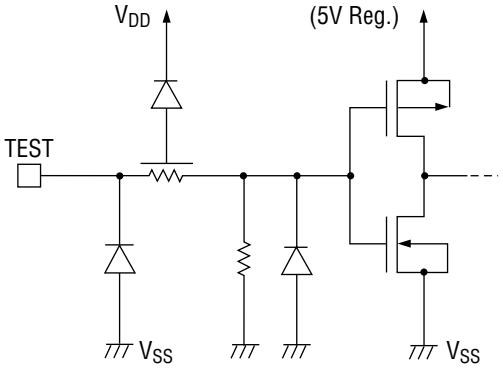
• Schematic Diagrams of Logic Portion Input Circuit 1



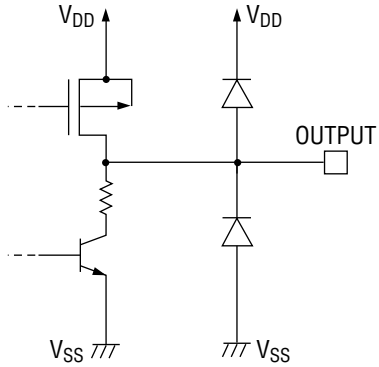
• Schematic Diagrams of Logic Portion Input Circuit 2



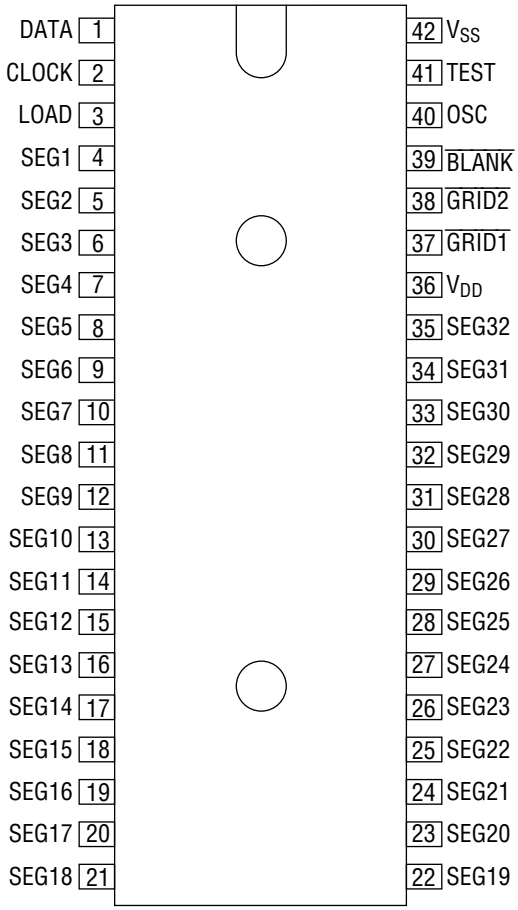
• Schematic Diagrams of Logic Portion Input Circuit 3



• Schematic Diagrams of Driver Output Circuit

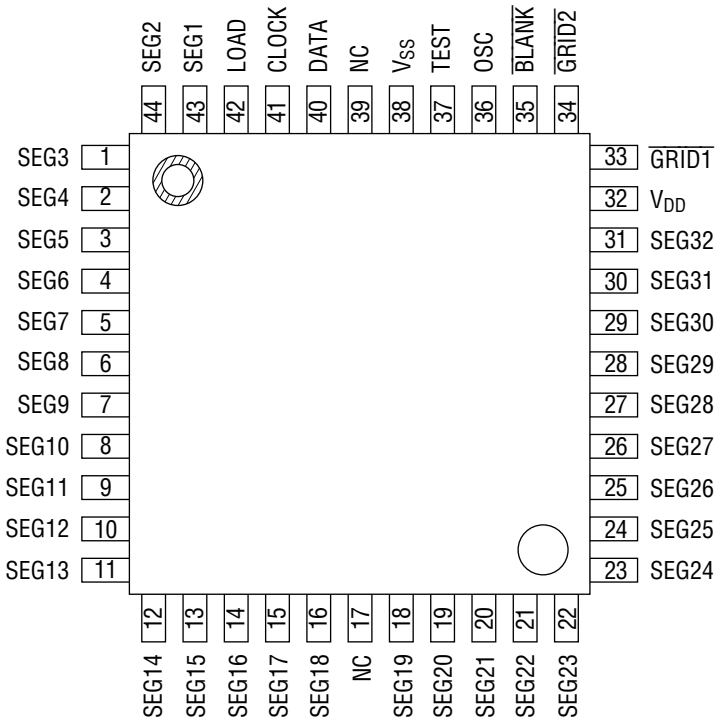


PIN CONFIGURATION (TOP VIEW)



42-Pin Plastic DIP

PIN CONFIGURATION (TOP VIEW)



NC : No-connection pin

44-Pin Plastic QFP

PIN DESCRIPTION

Symbol	Type	Description
DATA	I	Serial data input pin. This pin receives display data, dimming data, enable bit and mode bit.
CLOCK	I	Shift clock input pin with Schmitt circuit. Serial data is clocked in this pin at the rising edge of the shift clock pulse.
LOAD	I	Load pulse input pin. The load signal is input when dimming data and segment data transfer is finished.
SEG1 -SEG32	O	Segment driver output pins. These pins provide large current driving (I_{OH} = –5.5mA at V_{DD} = 12V) and small current driving (I_{OH} = –1.8mA at V_{DD} = 12V).
V_{DD}	—	Power supply voltage. This pin is connected to a power supply of 8 to 18V.
$\overline{GRID1}$	O	Grid driver output pin. When this pin is set to "L", the display is turned on. This pin is connected to external PNP transistor. The segment data of the first bit (S1) to the 32nd bit (S32) is valid in the segment data of 64 bits.
$\overline{GRID2}$	O	Grid driver output pin. When this pin is set to "L", the display is turned on. This pin is connected to external PNP transistor. The segment data of the 33rd bit (S33) to the 64th bit (S64) is valid in the segment data of 64 bits.
$\overline{BLANK}$	I	Display blank input pin with a pull-up resistor. When this pin is set to "L", the display is turned off (SEGn = "L")
OSC	I	Oscillation input pin. This pin is connected to an external capacitor of 82pF. A standard oscillation frequency is 512kHz.
TEST	I	Test input pin with a pull-down resistor. Normally this pin should be left open or should be connected to ground.
V_{SS}	—	Ground pin. This pin is connected to ground (V_{SS} = 0)

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Rating	Unit
Supply Voltage	V_{DD}	Ta = 25°C	–0.3 to +20	V
Input Voltage	V_{IN}	Ta = 25°C	–0.3 to +6.0	V
Storage Temperature Range	T_{STG}	—	–65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Condition	Range	Unit
Power Supply Voltage	V_{DD}	—	8 to 18	V
Operating Temperature Range	T_{op}	—	–40 to +85	°C

ELECTRICAL CHARACTERISTICS

DC Characteristics

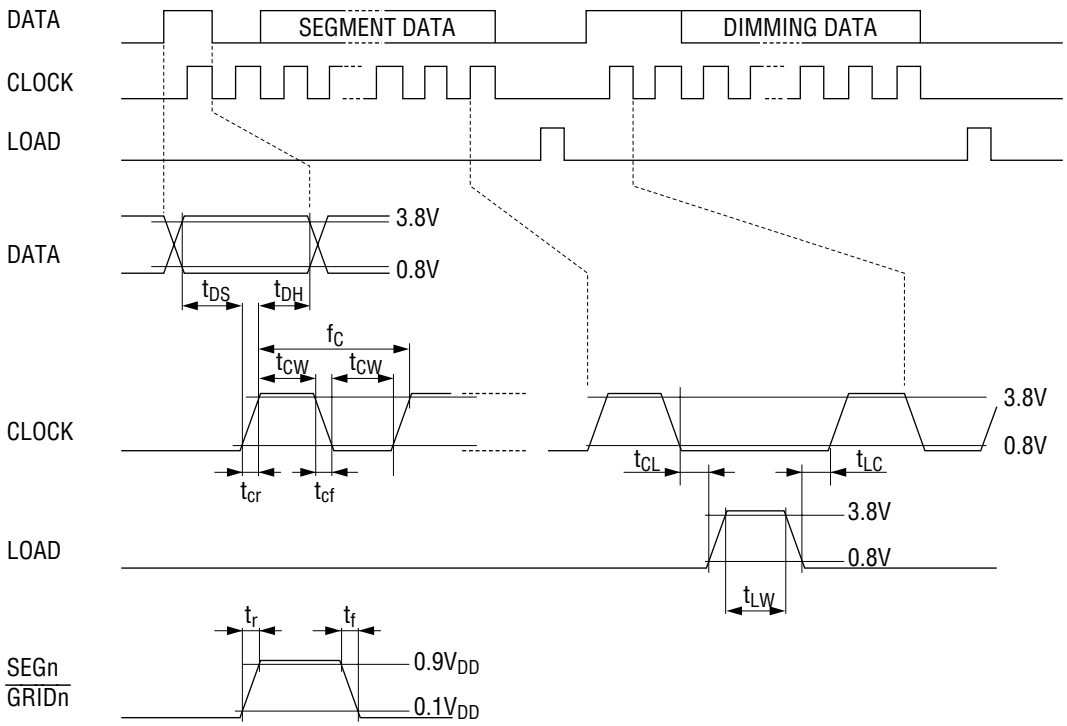
(Ta = –40 to +85°C, V_{DD} = 8 to 18V)

Parameter	Symbol	Condition	Min.	Max.	Unit	Applicable pin
High Level Input Voltage	V_{IH}	—	3.8	5.5	V	—
Low Level Input Voltage	V_{IL}	—	–0.3	0.8	V	—
High Level Input Current	I_{IH1}	V_I = 5V	–1	1	µA	DATA, LOAD CLOCK
	I_{IH3}	V_I = 5V	—	500	µA	TEST
Low Level Input Current	I_{IL1}	V_I = 0V	–1	1	µA	DATA, LOAD CLOCK
	I_{IL2}	V_I = 0V	–500	–100	µA	$\overline{\text{BLANK}}$
	I_{IL3}	V_I = 0V	–1	1	µA	TEST
High Level Output Voltage (1) (Small Current Driver)	V_{OH1}	V_{DD} = 9.5V, I_{OH1} = –1.3mA	V_{DD}-0.5	—	V	SEG (2n) n = 1-16
	V_{OH2}	V_{DD} = 12V, I_{OH2} = –1.8mA	V_{DD}-0.5	—	V	
	V_{OH3}	V_{DD} = 15V, I_{OH3} = –2.3mA	V_{DD}-0.5	—	V	
High Level Output Voltage (2) (Large Current Driver)	V_{OH4}	V_{DD} = 9.5V, I_{OH4} = –4.1mA	V_{DD}-0.5	—	V	SEG (2n-1) n = 1-16
	V_{OH5}	V_{DD} = 12V, I_{OH5} = –5.5mA	V_{DD}-0.5	—	V	
	V_{OH6}	V_{DD} = 15V, I_{OH6} = –7.0mA	V_{DD}-0.5	—	V	
Low Level Output Voltage	V_{OL1}	V_{DD} = 9.5V, I_{OL1} = 1mA	—	4	V	SEG1-SEG32 $\overline{\text{GRID1}}$, $\overline{\text{GRID2}}$
	V_{OL2}	V_{DD} = 9.5V, I_{OL2} = 500µA	—	2	V	
	V_{OL3}	V_{DD} = 9.5V, I_{OL3} = 2µA	—	0.3	V	
High Level Output Voltage (3)	V_{OH7}	V_{DD} = 9.5V, I_{OH7} = –0.8mA	V_{DD}-0.5	—	V	$\overline{\text{GRID1}}$, $\overline{\text{GRID2}}$
Current Consumption	I_{DD}	f_{OSC} = 512kHz, no load	—	20	mA	—

AC Characteristics

(Ta = –40 to +85°C, V_{DD} = 8 to 18V)

Parameter		Symbol	Condition	Min.	Typ.	Max.	Unit
Clock Frequency		f_C(1/tclock)	—	—	—	1	MHz
Clock Pulse Width		t_{CW}	—	500	—	—	ns
Clock Rise/Fall Time		t_{cr}, t_{cf}	—	—	—	500	ns
DATA Setup Time		t_{DS}	—	200	—	—	ns
DATA Hold Time		t_{DH}	—	200	—	—	ns
Clock → Load Time		t_{CL}	—	100	—	—	ns
Load → Clock Time		t_{LC}	—	50	—	—	ns
Load Pulse Width		t_{LW}	—	1.3	—	—	µs
SEGn Rise/Fall Time	Large Current	t_r, t_f	C_L = 20pF	0	4/120	400	ns
	Small Current	t_r, t_f	C_L = 20pF	0	15/120	400	ns
Grid Frequency		f_{GRID}	C_L = 82pF±5%	150	250	350	Hz
Oscillation Frequency		f_{OSC}		307.2	512	716.8	kHz



FUNCTIONAL DESCRIPTION

DATA Input

This device uses 10-bit dimming and 64-bit segment data.
In order to transfer this data, the enable bit (M0) and mode bit (M1) should be set to an initial state.
The data format is shown below.

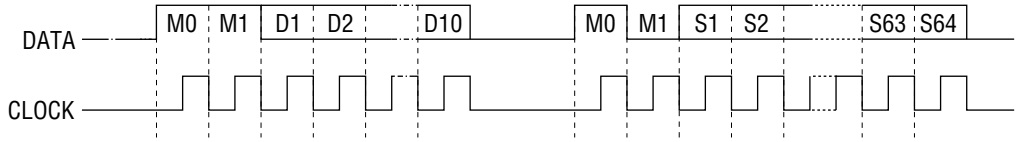


Figure 1. Data Transfer Timing

M0 : This bit is an enable bit.
M0 = "0" : Subsequent data is disabled; preceding data is held.
M0 = "1" : The beginning of data transfer. The following data is clocked in sequentially.
M1 : This bit is used to select the mode.
M1 = "0" : Subsequent data is handled as the segment data.
M1 = "1" : Subsequent data is handled as the dimming data.
D1 : LSB of dimming data.
S1 : data for grid1 of SEG1.
S2 : data for grid1 of SEG2.
⋮
S32 : data for grid1 of SEG32.
S33 : data for grid2 of SEG1.
⋮
S64 : data for grid2 of SEG32.

Notes: 1. Be sure to set the enable bit to "1" before data is transferred. Data following M0 is handled to be enable. If data is input with the enable bit not set to "1", the first "1" data coming next is handled as the enable bit.
2. If the number of the data bits applied is greater (for example, 67 bits are applied for the segment data of 64 bits), the data bits are pushed out in the same order that they are applied, and thus S1, S2, and S3 are ignored.
3. If the number of the data bits applied is smaller (for example, 62 bits are applied for the segment data of 64 bits), S63 and S64 prior to data transfer are shifted to S1 and S2 respectively.

CLOCK Input

DATA is shifted at the rising edge of the clock.

LOAD Input

The contents of the shift register are shifted in while the LOAD input is "H" and latched at "H" to "L" transition.
The LOAD signal is reproduced in the VF driver for the latch pulse for dimming data and segment data.
After 10-bit dimming data and 64-bit segment data are transferred, input the LOAD signal prior to the next clock.

Blank Function

A low-level voltage at the $\overline{\text{BLANK}}$ pin turns the display off (segment output = "L"). When segment data transfer is finished, the display is turned on.
The relationship between this data transfer and the display is shown in Figure 2.

Initial Setting

When powered on (i.e., when the segment data has never been transferred) the display is turned off (the segment output is "L").
When segment data transfer is finished, display is turned on. The relationship between this data transfer and the display is shown in Figure 2.

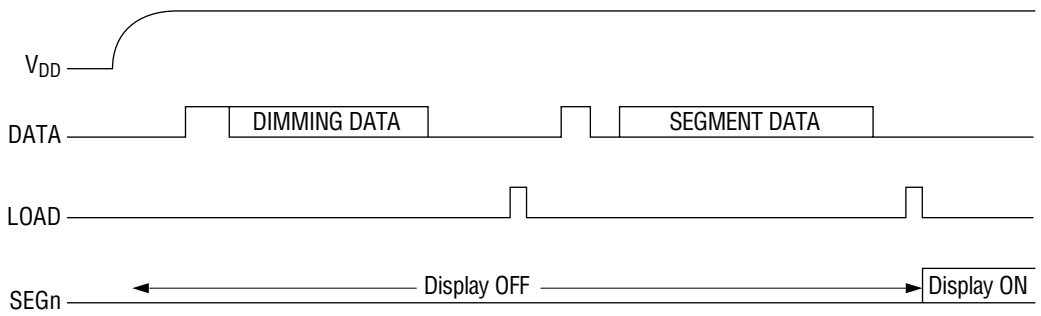


Figure 2. Relationship Between Data Transfer and Display

If the segment data is transferred before the dimming data is transferred after powered on, the display is turned on at the completion of segment data transfer, with undefined dimming values. The relationship between data transfer and display is shown in Figure. 3.

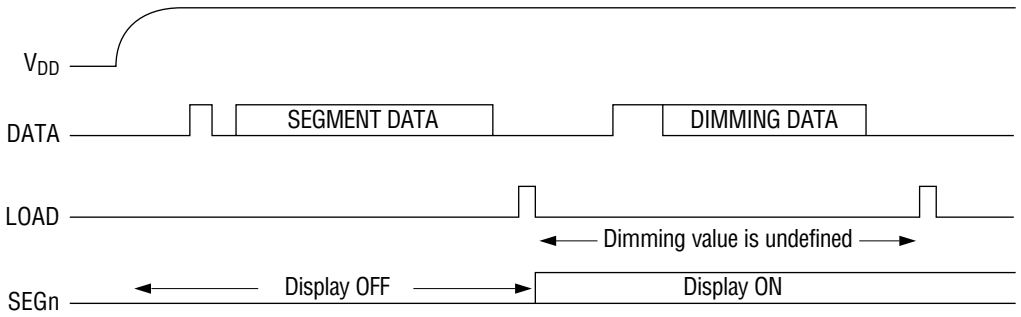


Figure 3. Relationship Between Advance Transfer of Segment Data and Display

Oscillator

Connect an external capacitor (C), as shown in Figure 4. The oscillating frequency f_{OSC} depends on the external capacitor used. The following equation is true between f_{OSC} and grid frequency (f_{GRID}):

$$f_{GRID} = f_{OSC}/2048$$

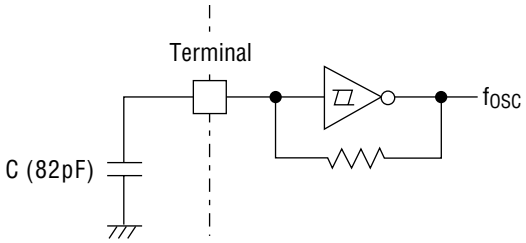


Figure 4. Oscillation Equivalent Circuit

Dimming Function

The duty cycle of grid output can be changed in 1/2048 step with respect to 10-bit dimming data. Table 1 shows the relationship between dimming data and duty ratio.

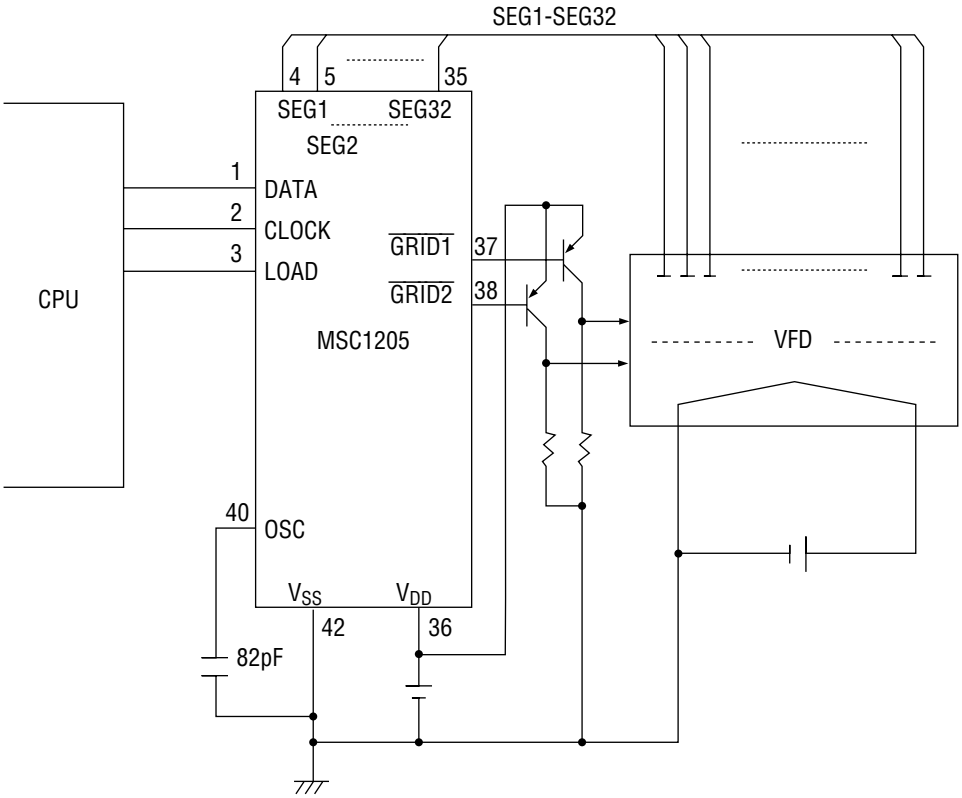
Table 1. Dimming Data and Duty Ratio

(MSB) dimming data (LSB)			Duty ratio	
00	0000	0000	0/2048	
00	0000	0001	1/2048	
˜	˜	˜	˜	
11	1111	0111	1015/2048	
11	1111	1000	1015.5/2048	Max
˜	˜	˜	˜	↓
11	1111	1110	1015.5/2048	Max

Note: Setting for address $3FF_H$ is invalid.

Duty ratios are programmable within the range of 0/2048 (0%) to 1015.5/2048 (49.6%).

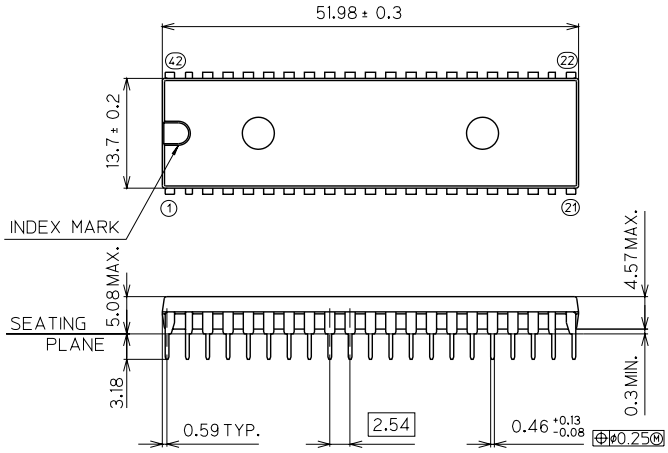
APPLICATION CIRCUIT



PACKAGE DIMENSIONS

(Unit : mm)

DIP42-P-600-2.54



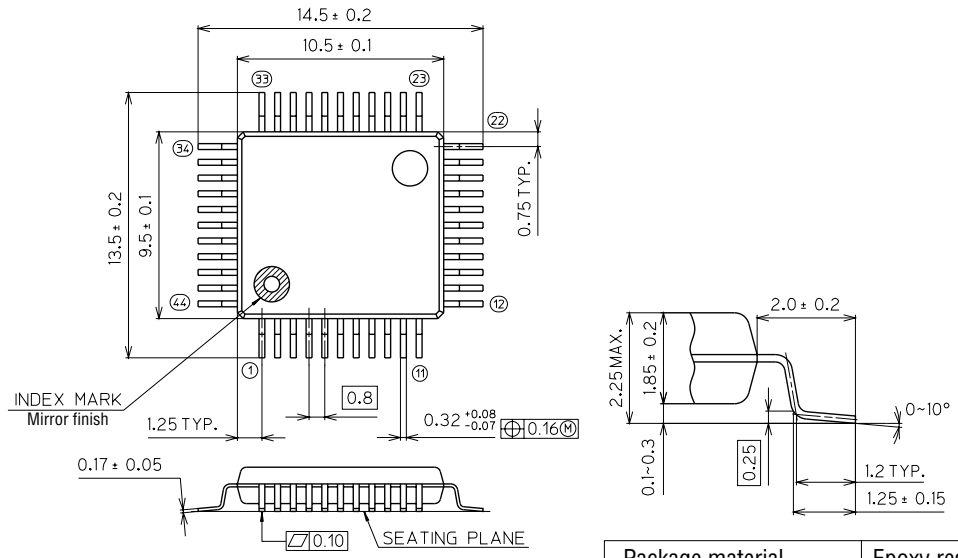
Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating
Solder plate thickness	5 μm or more
Package weight (g)	6.20 TYP.

Notes for Mounting the Surface Mount Type Package

The SOP, QFP, TSOP, SOJ, QFJ (PLCC), SHP and BGA are surface mount type packages, which are very susceptible to heat in reflow mounting and humidity absorbed in storage.
Therefore, before you perform reflow mounting, contact Oki's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

(Unit : mm)

QFP44-P-910-0.80-2K



Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating
Solder plate thickness	5 μm or more
Package weight (g)	0.41 TYP.

Notes for Mounting the Surface Mount Type Package

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