

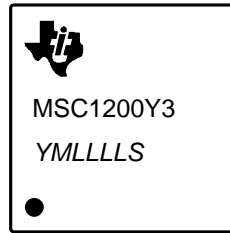
## Errata to MSC1200, Datasheet Literature Number SBAS317

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### Revision Identification

The device revision can be determined by the lot trace code marked on the top of the package or by the hardware version register internal to the device. The hardware version register is located at SFR EBh. Figure 1 shows an example of the package symbolization of the MSC1200.

**Figure 1. Package Symbolization Definition**



Where:

- Y is the year of assembly.
- M is the month of assembly.
- LLLL is the lot trace.
- S is the assembly site.

The MSC1200 device conforms functionally to the product data sheet (SBAS317), except for the anomalies described below.

*NOTE: The software files discussed in these errata are available for download from the MSC1200 web page at [www.ti.com](http://www.ti.com) as SBAC026.zip.*

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1. SPI operation.
2. I<sup>2</sup>C operation.
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6. IDAC operation with AVDD < 3.0V.
7. Only 128 bytes of RAM available.
8. Brownout voltage.

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## **Erratum #1**

### Brief Description of Issue

SPI Operation:

- 1) SPI Clock Phase Control for SPICON.CPHA = 0 is operational, but SPICON.CPHA = 1 is not operational. SPICON.CPHA must be cleared to '0' for SPI operation.
- 2) SPI Slave Select for SPICON.ESS = 0 is operational, but SPICON.ESS = 1 is not operational. SPICON.ESS must be cleared to '0' for SPI operation.
- 3) PDCON.PDSPI must be cleared to '0' for SPI operation.

### Detailed Description of Issue

SPI communication is only supported for clock phase '0' (SPICON.CPHA = 0) and no hardware slave select (SPICON.ESS = 0).

When the MSC1200 is used as a slave, the device drives the DOUT pin (P1.2) irrespective of the  $\overline{SS}$  input pin (P1.4) and SPICON.ESS settings.

### Impact to Customer

- 1) The SPICON.CPHA bit does not enable SPI clock phase '1' operation.
- 2) The SPICON.ESS bit does not enable hardware slave select for the DOUT pin (P1.2).

### SW or HW Workaround

$\overline{SS}$  can be implemented using software. The customer can use one of the external interrupts and a timer to achieve this operation. This may affect SPI data transfer rates.

*Download SBAC026.zip located on the MSC1200 web page at [www.ti.com](http://www.ti.com) for the C-code for software  $\overline{SS}$  implementation.*

### Affected Devices

MSC1200Y2 with lot trace codes of 51ZL45W and earlier, and hardware versions 06h and earlier.

MSC1200Y3 with lot trace codes of 51ZF8YW and earlier, and hardware versions 06h and earlier.

## **Erratum #2**

### Brief Description of Issue

I<sup>2</sup>C Operation:

- 1) I<sup>2</sup>C Clock Stretch Disable for I2CCON.DCS must be set to '1' for I<sup>2</sup>C operation; however, this will not disable I<sup>2</sup>C clock stretching.
- 2) PDCON.PDI2C is not operational (the state of PDCON.PDI2C is a *don't care*). However, the PDCON.PDSPI bit must be cleared to '0' and the I2CCON.DCS bit must be set to '1' to enable I<sup>2</sup>C operation.

### Detailed Description of Issue

To enable I<sup>2</sup>C operation, PDCON.PDSPI must be cleared to '0', PDCON.PDI2C is a *don't care*, and I2CCON.DCS must be set to '1'. During I<sup>2</sup>C slave operation, when the remote I<sup>2</sup>C master transfers data, the MSC1200 slave will stretch SCL.

### Impact to Customer

In a multiple slave system, the MSC1200 must release SCL stretching for each data transfer. This may decrease the throughput of the bus.

### SW or HW Workaround

Software can be used to release SCL stretching.

*Download SBAC026.zip located on the MSC1200 web page at [www.ti.com](http://www.ti.com) for the i2c\_slave.c C-code for SCL stretching implementation.*

### Affected Devices

MSC1200Y2 with lot trace codes of 51ZL45W and earlier, and hardware versions 06h and earlier.  
MSC1200Y3 with lot trace codes of 51ZF8YW and earlier, and hardware versions 06h and earlier.

### **Erratum #3**

#### Brief Description of Issue

The frequency output in Internal Oscillator Low Frequency mode [setting HCR2:CLKSEL = 111 (default)] at 5V is 13.4MHz  $\pm$ 300kHz.

#### Detailed Description of Issue

The frequency output in Internal Oscillator Low Frequency mode at 5V should be 12.8MHz (nominal).

#### Impact to Customer

Adjustments for internal timing differences must be made to take the frequency difference into account.

#### SW or HW Workaround

SFR settings for timing should be made to take the frequency difference into account.

#### Affected Devices

MSC1200Y2 with lot trace codes of 51ZL45W and earlier, and hardware versions 06h and earlier.  
MSC1200Y3 with lot trace codes of 51ZF8YW and earlier, and hardware versions 06h and earlier.

### **Erratum #4**

#### Brief Description of Issue

Stop mode digital and analog currents are excessive.

#### Detailed Description of Issue

All analog and digital circuits do not power down in Stop mode; therefore, the Stop mode digital and analog currents are excessive.

#### Impact to Customer

Stop mode digital and analog currents are excessive.

#### SW or HW Workaround

None.

#### Affected Devices

MSC1200Y2 with lot trace codes of 51ZL45W and earlier, and hardware versions 06h and earlier.  
MSC1200Y3 with lot trace codes of 51ZF8YW and earlier, and hardware versions 06h and earlier.

**Erratum #5**Brief Description of Issue

The PLL lock status bit (PLLH:PLLLOCK) is not operational.

Detailed Description of Issue

The PLL lock status bit (PLL:PLLLOCK) is always cleared to '0'.

Impact to Customer

There is no indication that the PLL has locked.

SW or HW Workaround

None.

Affected Devices

MSC1200Y2 with lot trace codes of 51ZL45W and earlier, and hardware versions 06h and earlier.  
MSC1200Y3 with lot trace codes of 51ZF8YW and earlier, and hardware versions 06h and earlier.

**Erratum #6**Brief Description of Issue

IDAC may not function when AVDD < 3.0V.

Detailed Description of Issue

IDAC may not function when AVDD < 3.0V.

Impact to Customer

IDAC may not function when AVDD < 3.0V.

SW or HW Workaround

Operate IDAC AVDD > 3.0V.

Affected Devices

MSC1200Y2 with lot trace codes of 51ZL45W and earlier, and hardware versions 06h and earlier.  
MSC1200Y3 with lot trace codes of 51ZF8YW and earlier, and hardware versions 06h and earlier.

**Erratum #7**Brief Description of Issue

Only 128 bytes of RAM are available, but the data sheet describes 256 bytes of available RAM.

Detailed Description of Issue

The MSC1200 was originally released with 128 bytes of RAM. The design was updated and newer versions of the device now have 256 bytes of available RAM.

Impact to Customer

Only 128 bytes can be used.

SW or HW Workaround

None.

Affected Devices

MSC1200Y2 with lot trace codes of 51ZL45W and earlier, and hardware versions 06h and earlier.  
MSC1200Y3 with lot trace codes of 51ZF8YW and earlier, and hardware versions 06h and earlier.

**Erratum #8**Brief Description of Issue

The description for HCR1 indicates several selectable voltage levels for Digital Brownout Reset. However, only one voltage (2.7V) is selected when Digital Brownout is enabled.

Detailed Description of Issue

The brownout voltage selection bits have no effect on the actual brownout voltage. This voltage is always 2.7V.

Impact to Customer

The brownout voltage is always 2.7V.

SW or HW Workaround

None.

Affected Devices

MSC1200Y2 with lot trace codes of 51ZL45W and earlier, and hardware versions 06h and earlier.  
MSC1200Y3 with lot trace codes of 51ZF8YW and earlier, and hardware versions 06h and earlier.

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