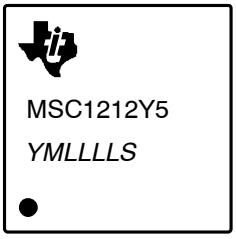
Errata to MSC1212, Datasheet Literature Number SBAS323

Revision Identification

The device revision can be determined by the lot trace code marked on the top of the package or by the hardware version register internal to the device. The hardware version register is located at SFR EBh. Figure 1 shows an example of the package symbolization of the MSC1212.

Figure 1. Package Symbolization Definition



Where:
Y is the year of assembly.
M is the month of assembly.
LLLL is the lot trace.
S is the assembly site.

MSC1212 device conforms functionally to the product data sheet (SBAS323), except for the anomalies described below.

Errata Index

1. IDACxDIS incorrect default value.
2. RST pin susceptible to latch up when pin voltage exceeds absolute maximum rating of 6.0V.
3. Internal SRAM corruption may occur in SPI™ FIFO mode.
4. Flash memory write operation fails when an additional MOVX command is issued before the operation is complete (only when system is executing from external program memory).
5. Setting and Clearing the RWDT bit in register WDTCON does not reset watchdog timer
6. The SPI MISO pin (P1.6) drives strong output even though the $\overline{SS}$ pin (P1.4) is high in slave mode.
7. The voltage and current output of the DAC is limited based on the analog supply voltage.
8. The maximum operating frequency of the device is limited based on the supply voltage and temperature.
9. Summation register (SUMR3:SUMR0) data corruption may occur.

Erratum #1

Brief Description of Issue

The IDAC0DIS bit in register DACCON0 and the IDAC1DIS bit in register DACCON1 have incorrect default values.

Detailed Description of Issue

After a reset, bits IDAC0DIS and IDAC1DIS are set to 0, thus enabling IDAC0 and IDAC1. This behavior is not desired since the current DACs should be disabled after a reset. The proper default value for these two bits should be 1.

Impact to Customer

Undesired current sourced out of the IDAC0/AIN0 and IDAC1/AIN1 pins after a reset. This could affect the voltage seen at the AIN0 and AIN1 inputs of the analog-to-digital converter.

SW or HW Workaround

After reset, in order to power off IDAC0 and IDAC1, user must configure VDAC0 and VDAC1 for normal mode, disable over-current protection, and set IDACxDIS bit to 1. That is, set DACCONx (1:0) to 00, DACCONx (6) to 0, and DACCONx (5) to 1.

Affected Devices

MSC1212Y2 with lot trace codes of 52Z66NW and earlier, and hardware version 00h.
MSC1212Y3 with lot trace codes of 52Z66RW and earlier, and hardware version 00h.
MSC1212Y4 with lot trace codes of 52Z66TW and earlier, and hardware version 00h.
MSC1212Y5 with lot trace codes of 52ZC37W and earlier, and hardware version 00h.

Erratum #2

Brief Description of Issue

RST pin susceptible to latch up when pin voltage exceeds the absolute maximum rating of 6.0V.

Detailed Description of Issue

RST (pin 13) passes latch-up testing (100mA) for DV_{DD} = 6.4V, which is beyond the maximum operating voltage of 6.0V. However, JESD78 requires latch-up testing to be performed at 1.5 x DV_{DD} max, which is 7.9V. When the test condition is clamped to 7.9V, the MSC1212 fails above 80mA.

Impact to Customer

The above test conditions are beyond the maximum ratings that are specified in the SBAS323 datasheet.

SW or HW Workaround

It is recommended that a series resistor of greater than 100Ω be placed between the RST pin and external reset circuitry.

Affected Devices

MSC1212Y2 with lot trace codes of 52Z66NW and earlier, and hardware version 00h.
MSC1212Y3 with lot trace codes of 52Z66RW and earlier, and hardware version 00h.
MSC1212Y4 with lot trace codes of 52Z66TW and earlier, and hardware version 00h.
MSC1212Y5 with lot trace codes of 52ZC37W and earlier, and hardware version 00h.

Erratum #3

Brief Description of Issue

SPI FIFO mode improper operation and internal SRAM corruption.

Detailed Description of Issue

SPI data transfers occur in a circular fashion (that is, the byte residing in the master buffer transfers to the slave buffer and vice versa). Therefore, a data write and read are both occurring in each device during an SPI transfer. When using the SPI in FIFO mode, the address and/or data during the data transfer may be corrupted by the DMA controller. If the data is corrupted during the transfer, then incorrect data may be written into internal SRAM. If the address is corrupted during the transfer, then the data will be written to an incorrect address in SRAM (the internal SRAM address range is 00h-FFh). In either case, data in the internal SRAM will be corrupted.

Impact to Customer

Use of the SPI in FIFO mode is not recommended; instead, the SPI should only be used in double-buffer mode.

SW or HW Workaround

None.

Affected Devices

MSC1212Y2 with lot trace codes of 52Z66NW and earlier, and hardware version 00h.
MSC1212Y3 with lot trace codes of 52Z66RW and earlier, and hardware version 00h.
MSC1212Y4 with lot trace codes of 52Z66TW and earlier, and hardware version 00h.
MSC1212Y5 with lot trace codes of 52ZC37W and earlier, and hardware version 00h.

Erratum #4

Brief Description of Issue

Using the MOVX command (from non-boot ROM program memory) after the MSC1212 has initiated an internal flash write may cause the flash memory to become corrupted.

Detailed Description of Issue

When a flash write is initiated by the MOVX @DPTR, ACC command, the value in the accumulator is placed onto the data input lines of the flash memory. If another MOVX @DPTR, ACC command is issued while the write operation is still in progress, the data input lines are updated with the new accumulator value. Thus, the area in flash memory that is being written to may be corrupted by the second memory write.
Note: The address of the second MOVX has no effect on the flash write destination.

Impact to Customer

The behavior is only observed when MSC1212 is executing code from non-boot ROM program memory. It has no effect on the customer if the system is executing from flash memory or boot ROM memory. The user has to ensure the flash write is completed before executing the next write command by polling the BUSY bit in register FMCON. Since the length of the flash write operation is 60μs, this latency must be accounted for in the user application.

SW or HW Workaround

While flash memory is being written, ensure that the BUSY bit in register FMCON is low before initiating the next MOVX @DPTR, ACC command.

Affected Devices

MSC1212Y2 with lot trace codes of 52Z66NW and earlier, and hardware version 00h.
MSC1212Y3 with lot trace codes of 52Z66RW and earlier, and hardware version 00h.
MSC1212Y4 with lot trace codes of 52Z66TW and earlier, and hardware version 00h.
MSC1212Y5 with lot trace codes of 52ZC37W and earlier, and hardware version 00h.

Erratum #5

Brief Description of Issue

Setting and clearing the RWDT bit in register WDTCON does not reset the watchdog timer.

Detailed Description of Issue

A write 1/write 0 sequence to the RWDT bit in register WDTCON (while the watchdog timer is enabled) does not cause the timer to restart. Instead, the timer continues to count until it expires.

Impact to Customer

If the EWDR bit in register HCR0 is enabled and the watchdog timer interrupt is enabled, the watchdog timer will cause an unexpected system reset when it expires, even though a write 1/write 0 sequence is performed on RWDT bit.

If the EWDR bit in register HCR0 is disabled and the watchdog timer interrupt is enabled, the watchdog timer will cause an unexpected interrupt when it expires, even though a write 1/write 0 sequence is performed on RWDT bit.

SW or HW Workaround

Instead of performing a write 1/write 0 sequence on RWDT bit, perform a write 1/write 0 sequence on the DWDT bit (disable watchdog) followed by a write 1/write 0 sequence on the EWDT bit (enable watchdog). These two bits are located in WDTCON (bit 6 and 7, respectively). Performing the disable/enable sequence has the overall effect of resetting the timer.

Affected Devices

MSC1212Y2 with lot trace codes of 52Z66NW and earlier, and hardware version 00h.
MSC1212Y3 with lot trace codes of 52Z66RW and earlier, and hardware version 00h.
MSC1212Y4 with lot trace codes of 52Z66TW and earlier, and hardware version 00h.
MSC1212Y5 with lot trace codes of 52ZC37W and earlier, and hardware version 00h.

Erratum #6

Brief Description of Issue

The SPI MISO pin (P1.6) drives a strong output even when the $\overline{SS}$ pin (P1.4) is high in slave mode.

Detailed Description of Issue

When SPI is in slave mode, P1.6 (MISO: Slave output) drives a strong output (could be '1' or '0') even when the $\overline{SS}$ pin (P1.4) is high. To be compliant with SPI protocol, this pin should be in a high-impedance state when $\overline{SS}$ is high. The $\overline{SS}$ pin is used to stop the slave from transmitting/receiving data but is not used to force P1.6 into a high-impedance state.

Impact to Customer

Customer must code additional software to disable the slave output line when the SPI is configured as a slave in multiple-slave mode.

SW or HW Workaround

INT2 is implemented on P1.4, so the interrupt can be used for disabling the SPI when the $\overline{SS}$ pin goes high. When SPI is disabled, pin P1.6 (MISO) is pulled up to '1' via the internal pull-up resistor. To enable the SPI, the $\overline{SS}$ pin must be connected to another port that supports low-active interrupts (for example, $\overline{INT0}$). This interrupt can be used to enable the SPI when $\overline{SS}$ goes low.

Affected Devices

MSC1212Y2 with lot trace codes of 52Z66NW and earlier, and hardware version 00h.
MSC1212Y3 with lot trace codes of 52Z66RW and earlier, and hardware version 00h.
MSC1212Y4 with lot trace codes of 52Z66TW and earlier, and hardware version 00h.
MSC1212Y5 with lot trace codes of 52ZC37W and earlier, and hardware version 00h.

Erratum #7

Brief Description of Issue

The voltage and current output of the DAC is limited based on the analog supply voltage.

Detailed Description of Issue

Each DAC can be selected to use the internal REFOUT/REF IN+ voltage or the supply voltage (AV_{DD}) as the reference for the DAC. The tables below summarize DAC operations for the various conditions.

VDAC OUTPUT	AV_{DD} = 5V	AV_{DD} = 3V	AV_{DD} < 3.0V
DACREF = AV_{DD}	Full Range	Full Range	Not Recommended
DACREF = 2.5V	Full Range	Not Recommended	Not Recommended
DACREF =1.25V	Full Range	Full Range	Not Recommended

IDAC OUTPUT	AV_{DD} = 5V	AV_{DD} = 3V	AV_{DD} < 3.0V
DACREF = AV_{DD}	0000h-7FFFh	0000h-3FFFh	Not Recommended
DACREF = 2.5V	Full Range	Not Recommended	Not Recommended
DACREF =1.25V	Full Range	Full Range	Not Recommended

Impact to Customer

The full output range of the DAC may not be usable under all conditions, as shown in the tables above.

SW or HW Workaround

This erratum has been fixed in the most recent revision of the device. There is no workaround for this revision of the device.

Affected Devices

MSC1212Y2 with lot trace codes of 52Z66NW and earlier, and hardware version 00h.
MSC1212Y3 with lot trace codes of 52Z66RW and earlier, and hardware version 00h.
MSC1212Y4 with lot trace codes of 52Z66TW and earlier, and hardware version 00h.
MSC1212Y5 with lot trace codes of 52ZC37W and earlier, and hardware version 00h.

Erratum #8

Brief Description of Issue

The maximum operating frequency of the device is limited based on the supply voltage and temperature.

Detailed Description of Issue

The table below lists the operating frequency ranges of the device.

SYMBOL	PARAMETER	2.7V to 3.6V		4.75V to 5.25V		UNITS
		MIN	MAX	MIN	MAX	
System Clock						
f_{OSC}	External Crystal Frequency (f_{OSC})	1	16	1	30	MHz
$1/f_{OSC}$	External Clock Frequency (f_{OSC})	0	16	1	30	MHz
f_{OSC}	External Ceramic Resonator Frequency (f_{OSC})	1	12	1	12	MHz

Impact to Customer

The device will not be able to operate of frequencies outside of this range.

SW or HW Workaround

This erratum has been fixed in the most recent revision of the device. There is no workaround for this revision of the device.

Affected Devices

MSC1212Y2 with lot trace codes of 52Z66NW and earlier, and hardware version 00h.
MSC1212Y3 with lot trace codes of 52Z66RW and earlier, and hardware version 00h.
MSC1212Y4 with lot trace codes of 52Z66TW and earlier, and hardware version 00h.
MSC1212Y5 with lot trace codes of 52ZC37W and earlier, and hardware version 00h.

Erratum #9

Brief Description of Issue

Summation register (SUMR3:SUMR0) data corruption may occur.

Detailed Description of Issue

When the summation register is used, the resulting value in the summation register may be corrupted.

Impact to Customer

Results from the summation register may be corrupted.

SW or HW Workaround

This erratum has been fixed in the most recent revision of the device.

For the most recent revision of the device, software routines for summation and shift operations can be used for proper operation.

Affected Devices

MSC1212Y2 with lot trace codes of 52Z66NW and earlier, and hardware version 00h.
MSC1212Y3 with lot trace codes of 52Z66RW and earlier, and hardware version 00h.
MSC1212Y4 with lot trace codes of 52Z66TW and earlier, and hardware version 00h.
MSC1212Y5 with lot trace codes of 52ZC37W and earlier, and hardware version 00h.

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