

FEDD5117400F-01

OKI Semiconductor

MSM5117400F

This version: June. 2000

Previous version : —

4,194,304-Word × 4-Bit DYNAMIC RAM : FAST PAGE MODE TYPE

DESCRIPTION

The MSM5117400F is a 4,194,304-word × 4-bit dynamic RAM fabricated in Oki's silicon-gate CMOS technology. The MSM5117400F achieves high integration, high-speed operation, and low-power consumption because Oki manufactures the device in a quadruple-layer polysilicon/double-layer metal CMOS process. The MSM5117400F is available in a 26/24-pin plastic SOJ or 26/24-pin plastic TSOP.

FEATURES

- 4,194,304-word × 4-bit configuration
- Single 5V power supply, ±10% tolerance
- Input : TTL compatible, low input capacitance
- Output : TTL compatible, 3-state
- Refresh : 2048 cycles/32ms
- Fast page mode, read modify write capability
- CAS before $\overline{\text{RAS}}$ refresh, hidden refresh, $\overline{\text{RAS}}$ -only refresh capability
- Packages

26/24-pin 300mil plastic SOJ (SOJ26/24-P-300-1.27)

(Product : MSM5117400F-xxSJ)

26/24-pin 300mil plastic TSOP (TSOPII26/24-P-300-0.80-K)

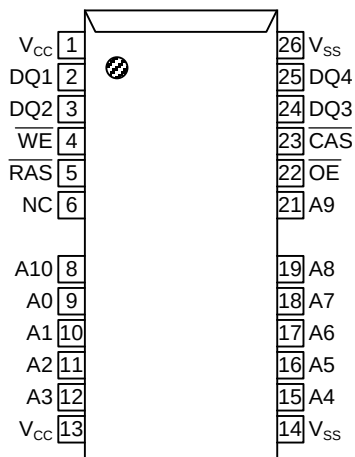
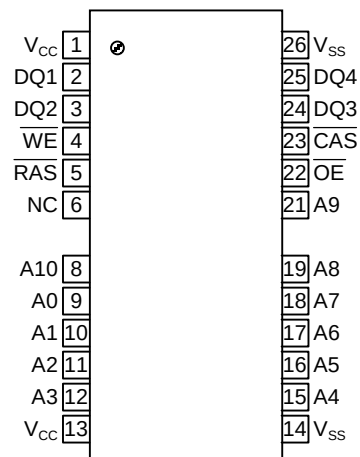
(Product : MSM5117400F-xxTS-K)

xx indicates speed rank.

PRODUCT FAMILY

Family	Access Time (Max.)				Cycle Time (Min.)	Power Dissipation	
	t_{RAC}	t_{AA}	t_{CAC}	t_{OEA}		Operating (Max.)	Standby (Max.)
MSM5117400F	50ns	25ns	13ns	13ns	90ns	550mW	5.5mW
	60ns	30ns	15ns	15ns	110ns	495mW	
	70ns	35ns	20ns	20ns	130ns	440mW	

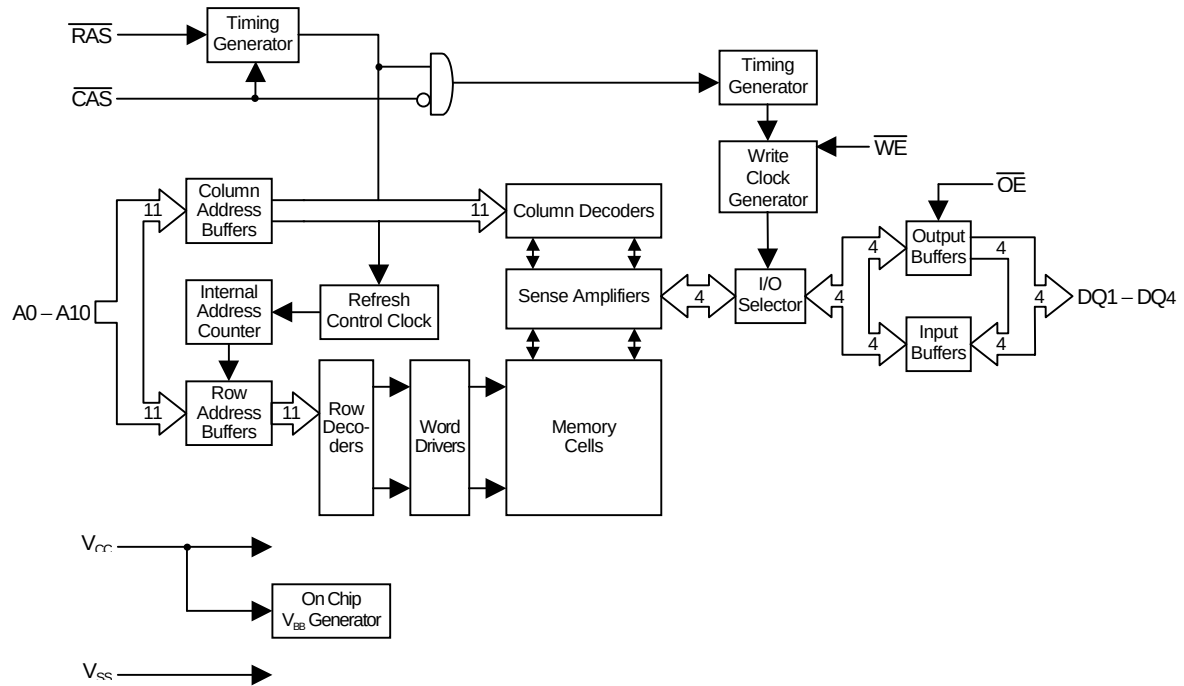
PIN CONFIGURATION (TOP VIEW)

26/24-Pin Plastic
SOJ26/24-Pin Plastic TSOP
(K Type)

Pin Name	Function
A0–A10	Address Input
$\overline{\text{RAS}}$	Row Address Strobe
$\overline{\text{CAS}}$	Column Address Strobe
DQ1–DQ4	Data Input/Data Output
$\overline{\text{OE}}$	Output Enable
$\overline{\text{WE}}$	Write Enable
V_{CC}	Power Supply (5V)
V_{SS}	Ground (0V)
NC	No Connection

Note : The same power supply voltage must be provided to every V_{CC} pin, and the same GND voltage level must be provided to every V_{SS} pin.

BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS**ABSOLUTE MAXIMUM RATINGS**

Parameter	Symbol	Value	Unit
Voltage V_{CC} Supply relative to V_{SS}	V_T	-0.5 to $V_{CC}+0.5$	V
Short Circuit Output Current	I_{OS}	50	mA
Power Dissipation	P_D^*	1	W
Operating Temperature	T_{opr}	0 to 70	°C
Storage Temperature	T_{stg}	-55 to 150	°C

*: $T_a = 25^{\circ}\text{C}$ **RECOMMENDED OPERATING CONDITIONS**

(Ta = 0 to 70°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Power Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.4	—	$V_{CC} + 0.5^{*1}$	V
Input Low Voltage	V_{IL}	-0.5^{*2}	—	0.8	V

Notes: *1. The input voltage is $V_{CC} + 1.0\text{V}$ when the pulse width is less than 20ns (the pulse width is with respect to the point at which V_{CC} is applied).

*2. The input voltage is $V_{SS} - 1.0\text{V}$ when the pulse width is less than 20ns (the pulse width respect to the point at which V_{SS} is applied).

PIN CAPACITANCE

(Vcc = 5V ± 10%, Ta = 25°C, f = 1 MHz)

Parameter	Symbol	Min.	Typ.	Min.	Unit
Input Capacitance (A0 – A10)	C_{IN1}	—	—	5	pF
Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$)	C_{IN2}	—	—	7	pF
Output Capacitance (DQ1 – DQ4)	$C_{I/O}$	—	—	7	pF

DC CHARACTERISTICS

(V_{CC} = 5V ± 10%, Ta = 0 to 70°C)

Parameter	Symbol	Condition	MSM5117400 F-50		MSM5117400 F-60		MSM5117400 F-70		Unit	Note
			Min.	Max.	Min.	Max.	Min.	Max.		
Output High Voltage	V _{OH}	I _{OH} = -5.0mA	2.4	V _{CC}	2.4	V _{CC}	2.4	V _{CC}	V	
Output Low Voltage	V _{OL}	I _{OL} = 4.2mA	0	0.4	0	0.4	0	0.4	V	
Input Leakage Current	I _{LI}	0V ≤ V _I ≤ 6.5V; All other pins not under test = 0V	-10	10	-10	10	-10	10	μA	
Output Leakage Current	I _{LO}	DQ disable 0V ≤ V _O ≤ V _{CC}	-10	10	-10	10	-10	10	μA	
Average Power Supply Current (Operating)	I _{CC1}	$\overline{\text{RAS}}$, $\overline{\text{CAS}}$ cycling, t _{RC} = Min.	—	100	—	90	—	80	mA	1,2
Power Supply Current (Standby)	I _{CC2}	$\overline{\text{RAS}}$, $\overline{\text{CAS}}$ = V _{IH}	—	2	—	2	—	2	mA	1
		$\overline{\text{RAS}}$, $\overline{\text{CAS}}$ ≥ V _{CC} - 0.2V	—	1	—	1	—	1		
Average Power Supply Current ($\overline{\text{RAS}}$ -only Refresh)	I _{CC3}	$\overline{\text{RAS}}$ cycling, $\overline{\text{CAS}}$ = V _{IH} , t _{RC} = Min.	—	100	—	90	—	80	mA	1,2
Power Supply Current (Standby)	I _{CC5}	$\overline{\text{RAS}}$ = V _{IH} , $\overline{\text{CAS}}$ = V _{IL} , DQ = enable	—	5	—	5	—	5	mA	1
Average Power Supply Current ($\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ Refresh)	I _{CC6}	$\overline{\text{RAS}}$ = cycling, $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$	—	100	—	90	—	80	mA	1,2
Average Power Supply Current (Fast Page Mode)	I _{CC7}	$\overline{\text{RAS}}$ = V _{IL} , $\overline{\text{CAS}}$ cycling, t _{PC} = Min.	—	80	—	70	—	60	mA	1,3

- Notes: 1. I_{CC} Max. is specified as I_{CC} for output open condition.
2. The address can be changed once or less while $\overline{\text{RAS}}$ = V_{IL}.
3. The address can be changed once or less while $\overline{\text{CAS}}$ = V_{IH}.

AC CHARACTERISTICS (1/2)

(V_{CC} = 5V ± 10%, Ta = 0 to 70°C) Note1,2,3,11,12

Parameter	Symbol	MSM5117400 F-50		MSM5117400 F-60		MSM5117400 F-70		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.		
Random Read or Write Cycle Time	t _{RC}	90	—	110	—	130	—	ns	
Read Modify Write Cycle Time	t _{RWC}	131	—	155	—	185	—	ns	
Fast Page Mode Cycle Time	t _{PC}	35	—	40	—	45	—	ns	
Fast Page Mode Read Modify Write Cycle Time	t _{PRWC}	76	—	85	—	100	—	ns	
Access Time from $\overline{\text{RAS}}$	t _{RAC}	—	50	—	60	—	70	ns	4, 5, 6
Access Time from $\overline{\text{CAS}}$	t _{CAC}	—	13	—	15	—	20	ns	4, 5
Access Time from Column Address	t _{AA}	—	25	—	30	—	35	ns	4, 6
Access Time from $\overline{\text{CAS}}$ Precharge	t _{CPA}	—	30	—	35	—	40	ns	4
Access Time from $\overline{\text{OE}}$	t _{OEa}	—	13	—	15	—	20	ns	4
Output Low Impedance Time from $\overline{\text{CAS}}$	t _{CLZ}	0	—	0	—	0	—	ns	4
$\overline{\text{CAS}}$ to Data Output Buffer Turn-off Delay Time	t _{OFF}	0	13	0	15	0	20	ns	7
$\overline{\text{OE}}$ to Data Output Buffer Turn-off Delay Time	t _{OEZ}	0	13	0	15	0	20	ns	7
Transition Time	t _T	3	50	3	50	3	50	ns	3
Refresh Period	t _{REF}	—	32	—	32	—	32	ms	
$\overline{\text{RAS}}$ Precharge Time	t _{RP}	30	—	40	—	50	—	ns	
$\overline{\text{RAS}}$ Pulse Width	t _{RAS}	50	10,000	60	10,000	70	10,000	ns	
$\overline{\text{RAS}}$ Pulse Width (Fast Page Mode)	t _{RASP}	50	100,000	60	100,000	70	100,000	ns	
$\overline{\text{RAS}}$ Hold Time	t _{RSH}	13	—	15	—	20	—	ns	
$\overline{\text{RAS}}$ Hold Time referenced to $\overline{\text{OE}}$	t _{ROH}	13	—	15	—	20	—	ns	
$\overline{\text{CAS}}$ Precharge Time (Fast Page Mode)	t _{CP}	7	—	10	—	10	—	ns	
$\overline{\text{CAS}}$ Pulse Width	t _{CAS}	13	10,000	15	10,000	20	10,000	ns	
$\overline{\text{CAS}}$ Hold Time	t _{CSH}	50	—	60	—	70	—	ns	
$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ Precharge Time	t _{CRP}	5	—	5	—	5	—	ns	
$\overline{\text{RAS}}$ Hold Time from $\overline{\text{CAS}}$ Precharge	t _{RHCP}	30	—	35	—	40	—	ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Delay Time	t _{RCD}	17	37	20	45	20	50	ns	5
$\overline{\text{RAS}}$ to Column Address Delay Time	t _{RAD}	12	25	15	30	15	35	ns	6
Row Address Set-up Time	t _{ASR}	0	—	0	—	0	—	ns	

AC CHARACTERISTICS (2/2)

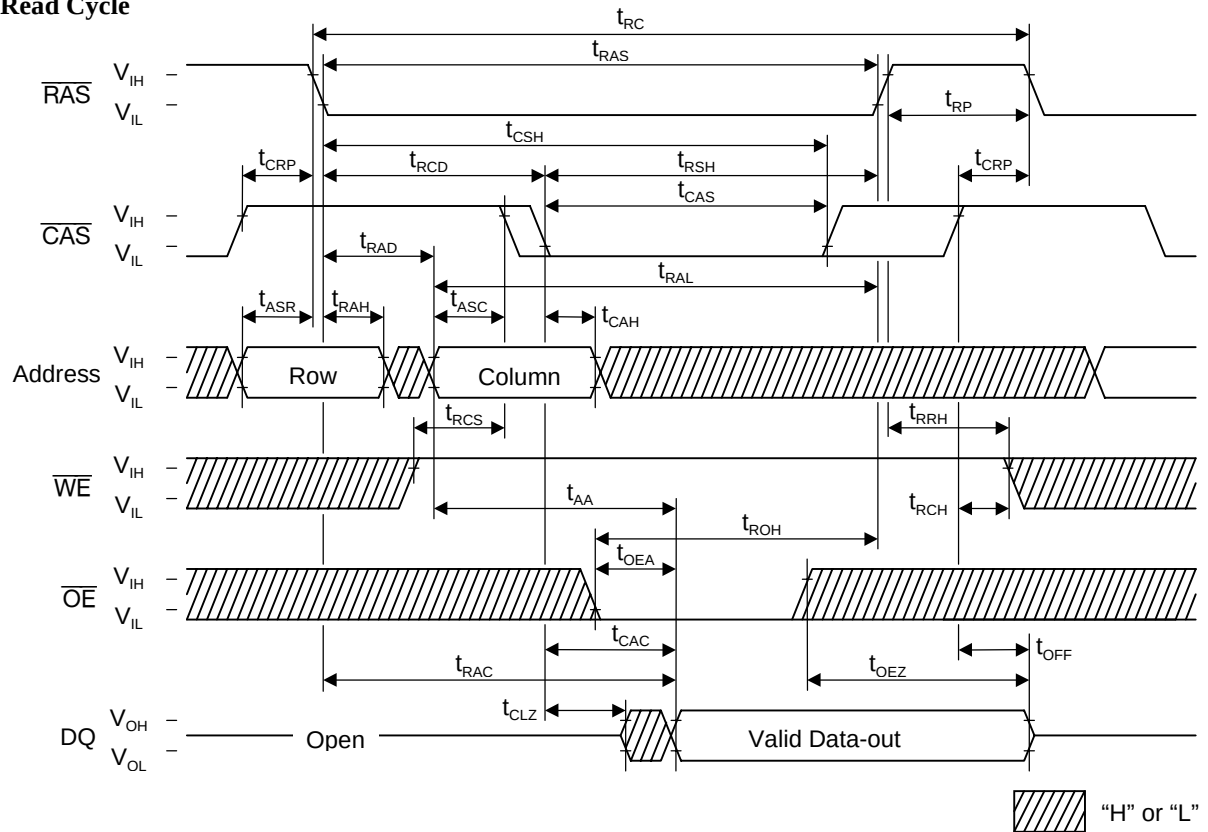
(V_{CC} = 5V ± 10%, Ta = 0 to 70°C) Note1,2,3,11,12

Parameter	Symbol	MSM5117400 F-50		MSM5117400 F-60		MSM5117400 F-70		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.		
Row Address Hold Time	t _{RAH}	7	—	10	—	10	—	ns	
Column Address Set-up Time	t _{ASC}	0	—	0	—	0	—	ns	
Column Address Hold Time	t _{CAH}	7	—	10	—	15	—	ns	
Column Address to $\overline{\text{RAS}}$ Lead Time	t _{RAL}	25	—	30	—	35	—	ns	
Read Command Set-up Time	t _{RCS}	0	—	0	—	0	—	ns	
Read Command Hold Time	t _{RCH}	0	—	0	—	0	—	ns	8
Read Command Hold Time referenced to $\overline{\text{RAS}}$	t _{RRH}	0	—	0	—	0	—	ns	8
Write Command Set-up Time	t _{WCS}	0	—	0	—	0	—	ns	9
Write Command Hold Time	t _{WCH}	7	—	10	—	15	—	ns	
Write Command Pulse Width	t _{WP}	7	—	10	—	10	—	ns	
$\overline{\text{OE}}$ Command Hold Time	t _{OEH}	13	—	15	—	20	—	ns	
Write Command to $\overline{\text{RAS}}$ Lead Time	t _{RWL}	13	—	15	—	20	—	ns	
Write Command to $\overline{\text{CAS}}$ Lead Time	t _{CWL}	13	—	15	—	20	—	ns	
Data-in Set-up Time	t _{DS}	0	—	0	—	0	—	ns	10
Data-in Hold Time	t _{DH}	7	—	10	—	15	—	ns	10
$\overline{\text{OE}}$ to Data-in Delay Time	t _{OED}	13	—	15	—	20	—	ns	
$\overline{\text{CAS}}$ to $\overline{\text{WE}}$ Delay Time	t _{CWD}	36	—	40	—	50	—	ns	9
Column Address to $\overline{\text{WE}}$ Delay Time	t _{AWD}	48	—	55	—	65	—	ns	9
$\overline{\text{RAS}}$ to $\overline{\text{WE}}$ Delay Time	t _{RWD}	73	—	85	—	100	—	ns	9
$\overline{\text{CAS}}$ Precharge $\overline{\text{WE}}$ Delay Time	t _{CPWD}	53	—	60	—	70	—	ns	9
$\overline{\text{CAS}}$ Active Delay Time from $\overline{\text{RAS}}$ Precharge	t _{RPC}	5	—	5	—	5	—	ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Set-up Time ($\overline{\text{CAS}}$ before $\overline{\text{RAS}}$)	t _{CSR}	10	—	5	—	5	—	ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Hold Time ($\overline{\text{CAS}}$ before $\overline{\text{RAS}}$)	t _{CHR}	10	—	10	—	10	—	ns	
$\overline{\text{WE}}$ to $\overline{\text{RAS}}$ Precharge Time ($\overline{\text{CAS}}$ before $\overline{\text{RAS}}$)	t _{WRP}	10	—	10	—	10	—	ns	
$\overline{\text{WE}}$ Hold Time from $\overline{\text{RAS}}$ ($\overline{\text{CAS}}$ before $\overline{\text{RAS}}$)	t _{WRH}	10	—	10	—	10	—	ns	
$\overline{\text{RAS}}$ to $\overline{\text{WE}}$ Set-up Time (Test Mode)	t _{WTS}	10	—	10	—	10	—	ns	
$\overline{\text{RAS}}$ to $\overline{\text{WE}}$ Hold Time (Test Mode)	t _{WTH}	10	—	10	—	10	—	ns	

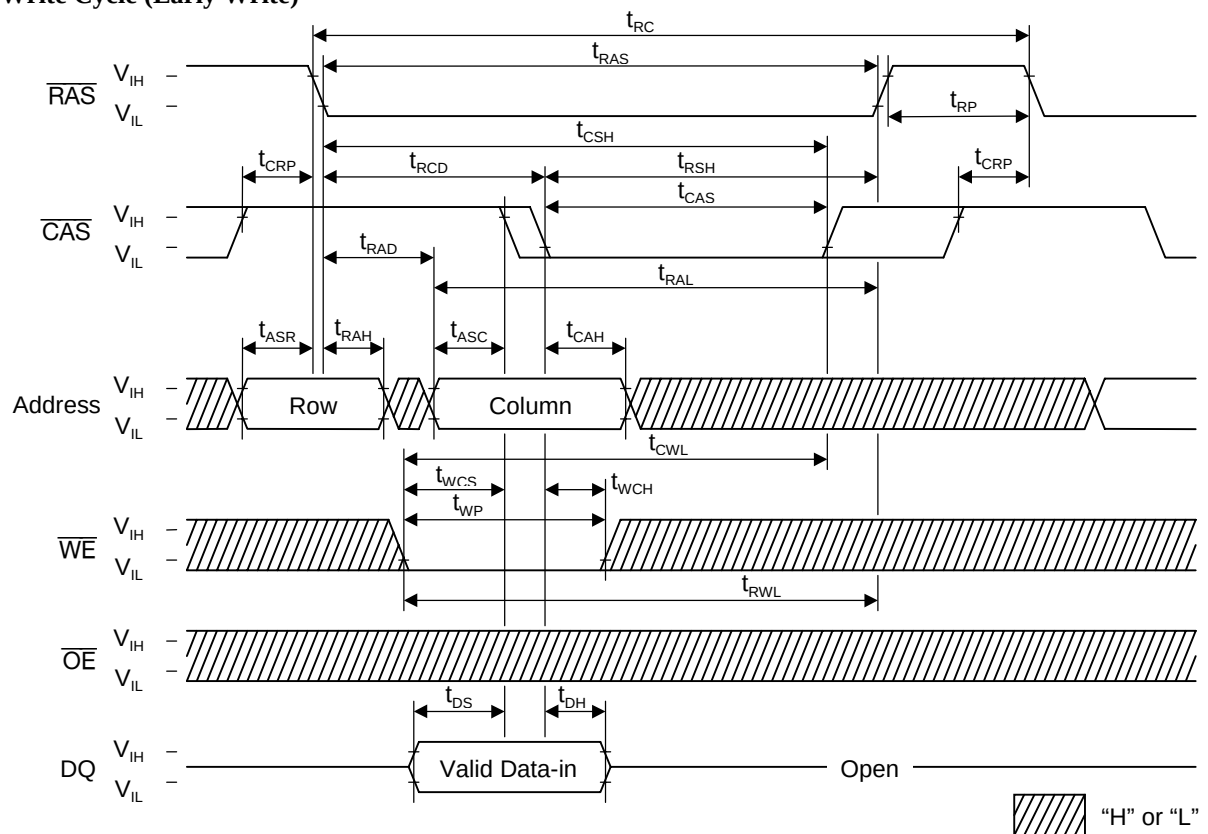
- Notes:
1. A start-up delay of 200 μ s is required after power-up, followed by a minimum of eight initialization cycles ($\overline{\text{RAS}}$ -only refresh or $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh) before proper device operation is achieved.
 2. The AC characteristics assume $t_T = 5\text{ns}$.
 3. V_{IH} (Min.) and V_{IL} (Max.) are reference levels for measuring input timing signals. Transition times (t_T) are measured between V_{IH} and V_{IL} .
 4. -50 is measured with a load circuit equivalent to 2TTL load and 50pF, and -60/-70 is measured with a load circuit equivalent to 2TTL load and 100pF.
 5. Operation within the t_{RCD} (Max.) limit ensures that t_{RAC} (Max.) can be met. t_{RCD} (Max.) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD} (Max.) limit, then the access time is controlled by t_{CAC} .
 6. Operation within the t_{RAD} (Max.) limit ensures that t_{RAC} (Max.) can be met. t_{RAD} (Max.) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD} (Max.) limit, then the access time is controlled by t_{AA} .
 7. t_{OFF} (Max.) and t_{OEZ} (Max.) define the time at which the output achieved the open circuit condition and are not referenced to output voltage levels.
 8. t_{RCH} or t_{RRH} must be satisfied for a read cycle.
 9. t_{WCS} , t_{CWD} , t_{RWD} , t_{AWD} and t_{CPWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$ (Min.), then the cycle is an early write cycle and the data out will remain open circuit (high impedance) throughout the entire cycle. If $t_{CWD} \geq t_{CWD}$ (Min.), $t_{RWD} \geq t_{RWD}$ (Min.), $t_{AWD} \geq t_{AWD}$ (Min.) and $t_{CPWD} \geq t_{CPWD}$ (Min.), then the cycle is a read modify write cycle and data out will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, then the condition of the data out (at access time) is indeterminate.
 10. These parameters are referenced to the $\overline{\text{CAS}}$, leading edges in an early write cycle, and to the $\overline{\text{WE}}$ leading edge in an $\overline{\text{OE}}$ control write cycle, or a read modify write cycle.
 11. The test mode is initiated by performing a $\overline{\text{WE}}$ and $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh cycle. This mode is latched and remains in effect until the exit cycle is generated. In a test CA0, CA1 and CA10 are not used and each DQ pin now access 8-bit locations. Since all 4 DQ pins are used, a total 32 data bits can be written in parallel into the memory array. In a read cycle, if 8 data bits are equal, the DQ pin will indicate a high level. If the 8 data bits are not equal, the DQ pin will indicate a low level. The test mode is cleared and the memory device returned to its normal operating state by performing a $\overline{\text{RAS}}$ -only refresh cycle or a $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh cycle.
 12. In a test mode read cycle, the value of access time parameter is delayed for 5ns for the specified value. These parameters should be specified in test mode cycle by adding the above value to the specified value in this data sheet.

TIMING CHART

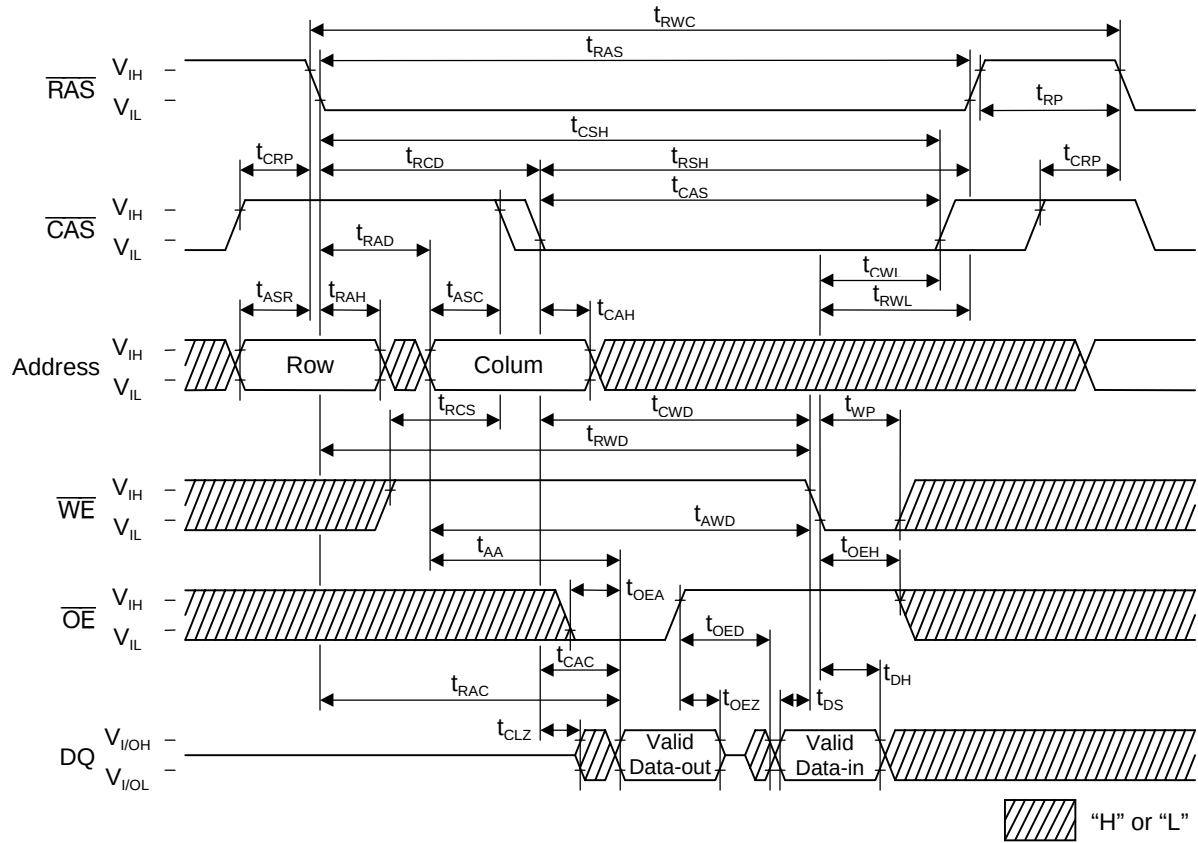
Read Cycle



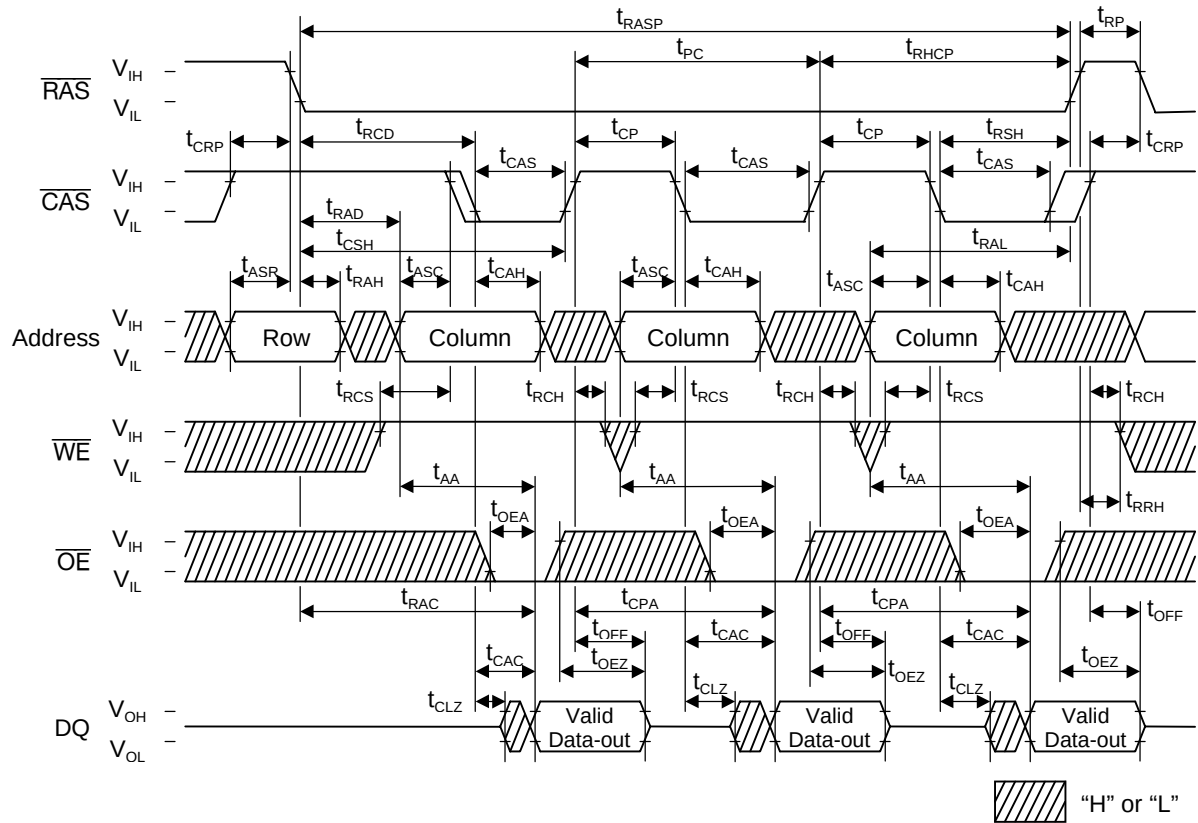
Write Cycle (Early Write)



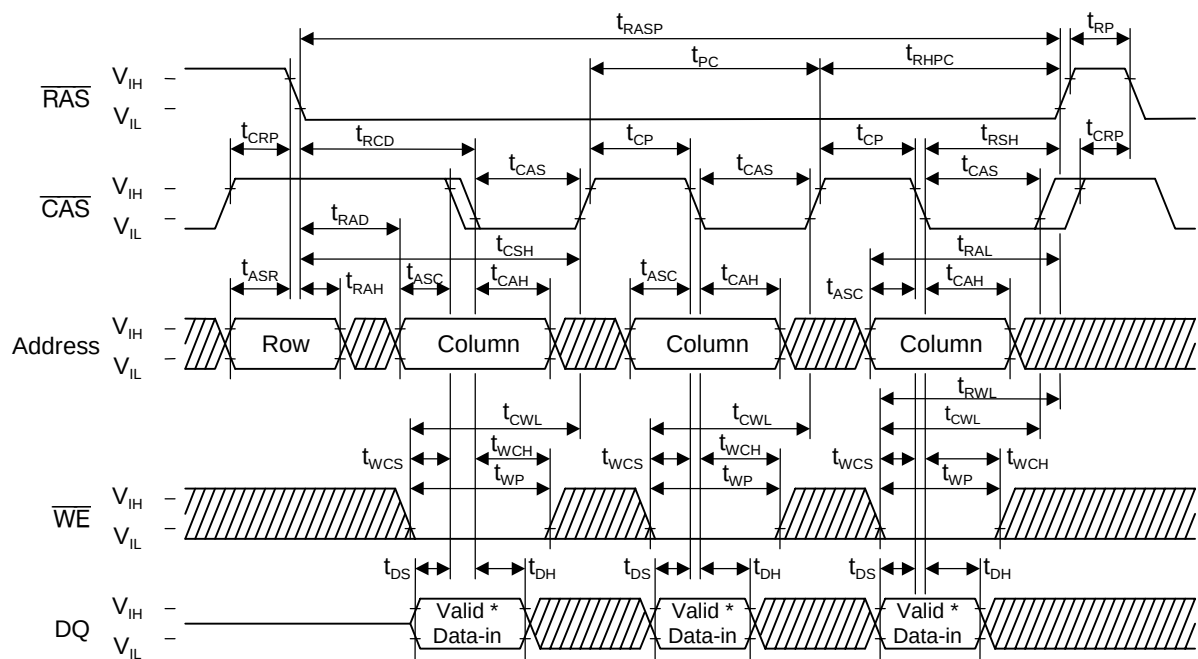
Read Modify Write Cycle



Fast Page Mode Write Cycle



Fast Page Mode Write Cycle (Early Write)



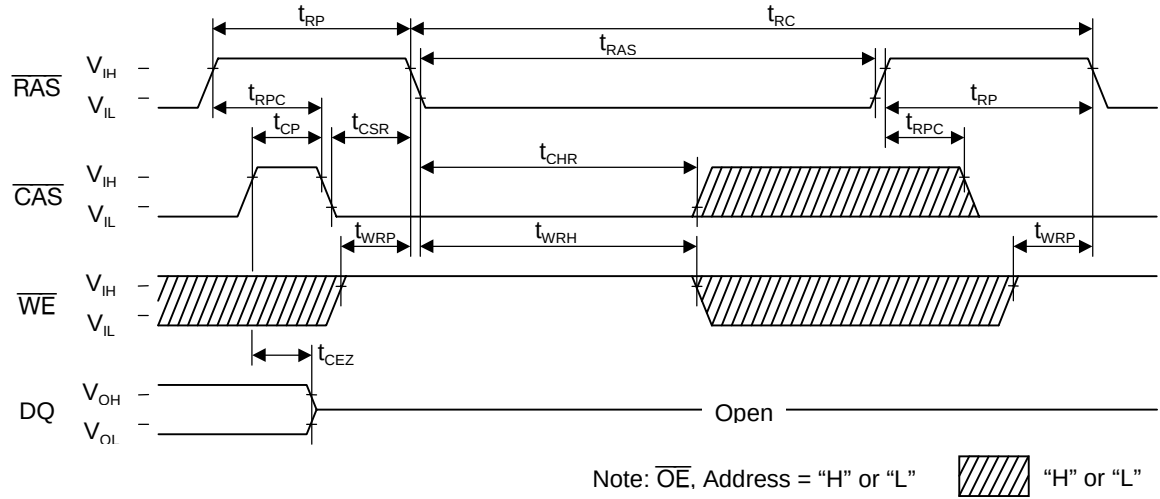
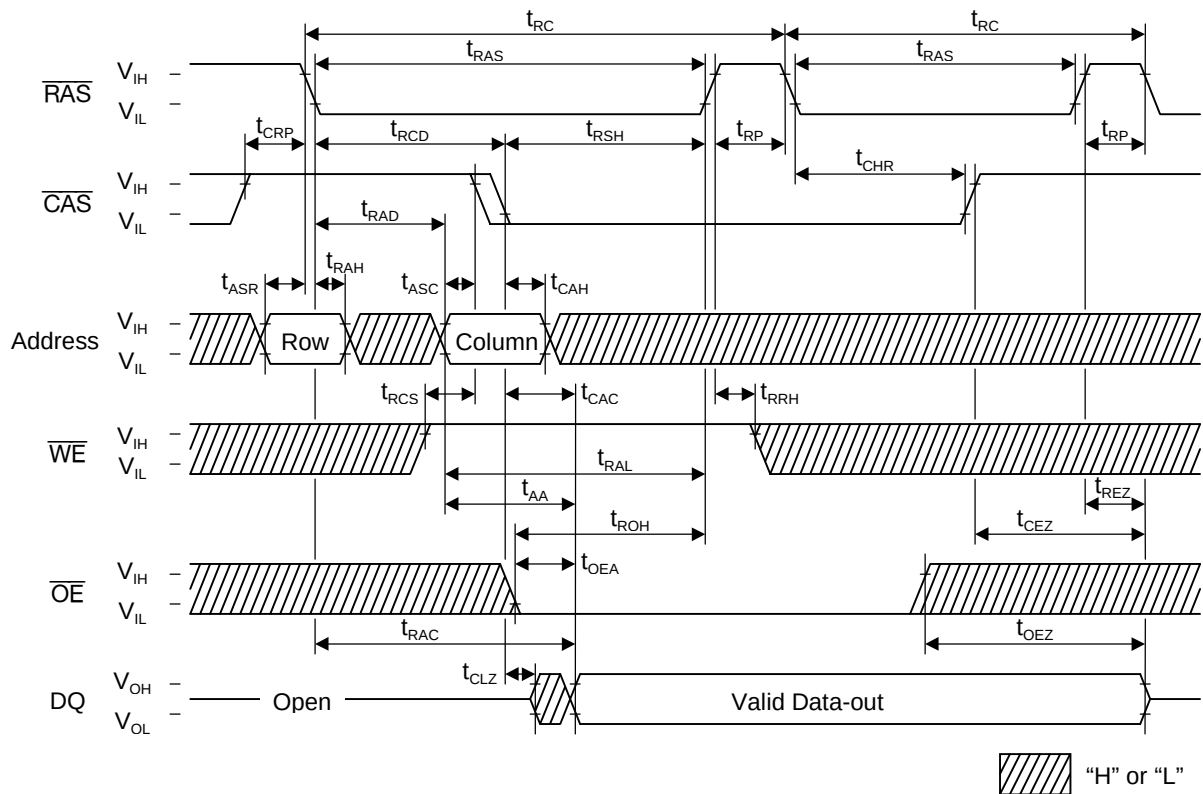
Note: $\overline{\text{OE}}$ = "H" or "L"  "H" or "L"

Note: In = Valid Data-in, Out = Valid Data-out  "H" or "L"

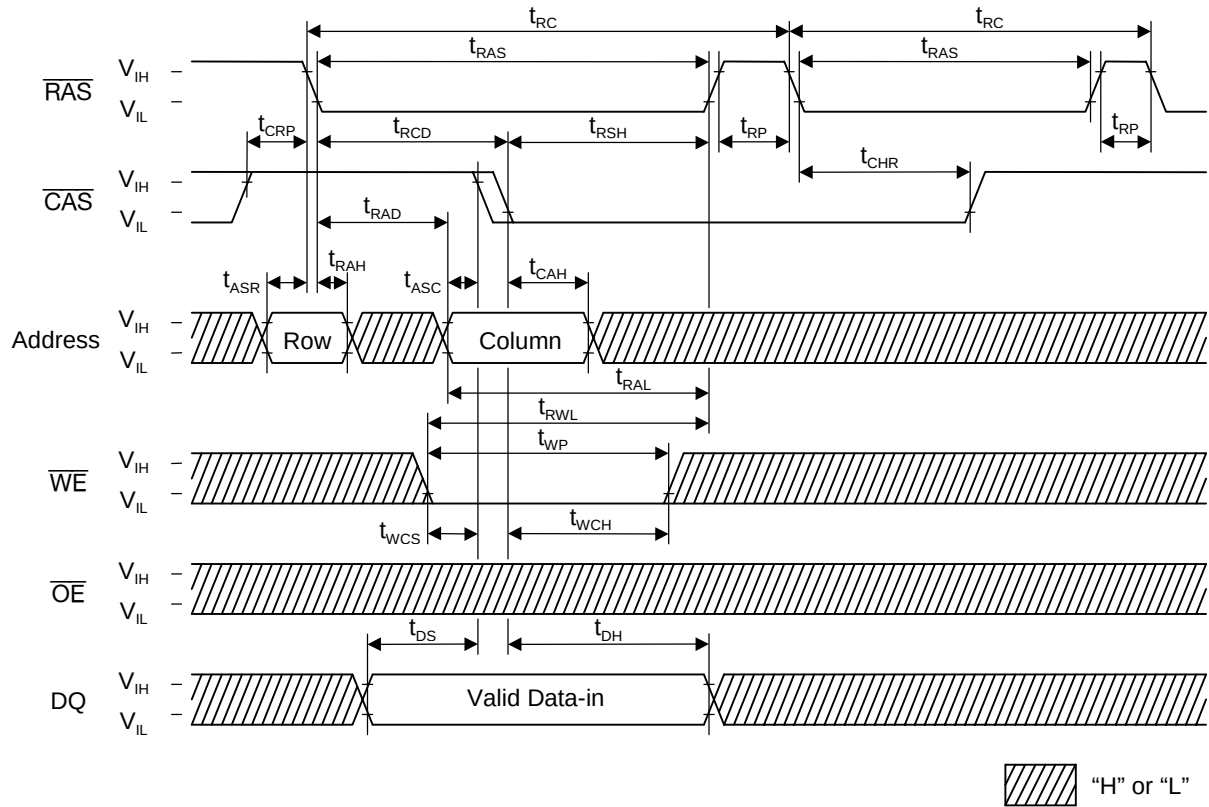
The diagram illustrates the timing relationships for a memory access. The signals shown are $\overline{\text{RAS}}$, $\overline{\text{CAS}}$, Address, and DQ. The voltage levels are indicated as V_{IH} (high) and V_{IL} (low) for the control signals, and V_{OH} (output high) and V_{OL} (output low) for the data signal. The timing parameters are defined as follows:

- t_{RAS} : RAS access time, from the falling edge of $\overline{\text{RAS}}$ to the data becoming valid.
- t_{RC} : RAS refresh time, from the falling edge of $\overline{\text{RAS}}$ to the data becoming invalid.
- t_{CRP} : RAS to CAS precharge time, from the rising edge of $\overline{\text{CAS}}$ to the falling edge of $\overline{\text{RAS}}$.
- t_{RP} : RAS precharge time, from the rising edge of $\overline{\text{RAS}}$ to the data becoming invalid.
- t_{RPC} : RAS to CAS precharge time, from the rising edge of $\overline{\text{CAS}}$ to the rising edge of $\overline{\text{RAS}}$.
- t_{ASR} : Address setup time, from the falling edge of Address to the falling edge of $\overline{\text{RAS}}$.
- t_{RAH} : Address hold time, from the rising edge of Address to the rising edge of $\overline{\text{RAS}}$.
- t_{OFF} : Output delay time, from the falling edge of $\overline{\text{RAS}}$ to the data becoming invalid.
- t_{OH} : Output hold time, from the falling edge of $\overline{\text{RAS}}$ to the data becoming invalid.

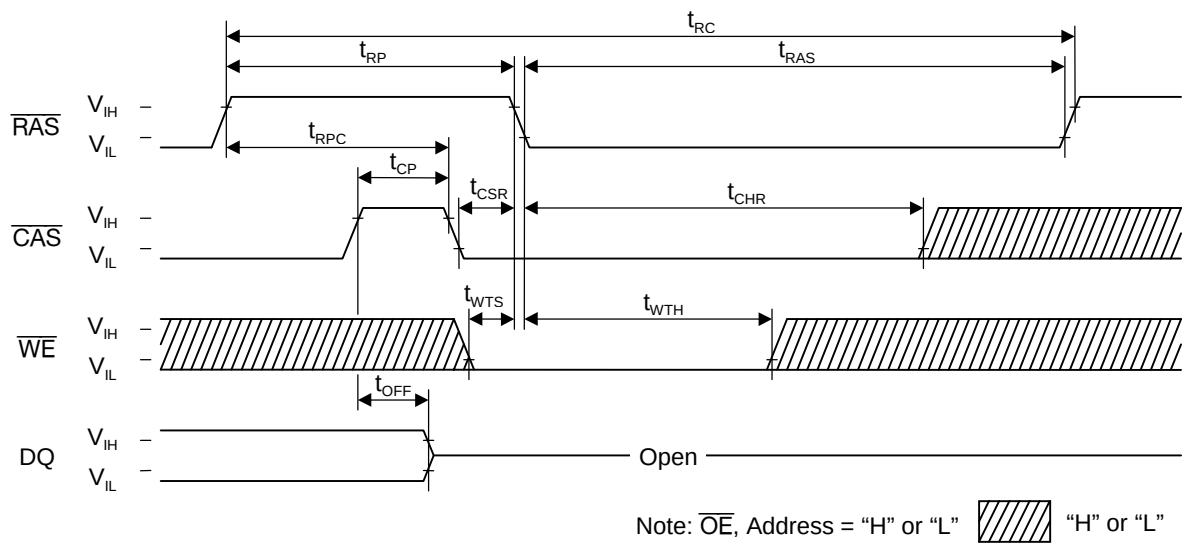
Note: $\overline{WE}$, $\overline{OE}$ = "H" or "L"  "H" or "L"

CAS before RAS Refresh Cycle**Hidden Refresh Read Cycle**

Hidden Refresh Write Cycle



Test Mode-in Cycle



NOTICE

1. The information contained herein can change without notice owing to product and/or technical improvements. Before using the product, please make sure that the information being referred to is up-to-date.
2. The outline of action and examples for application circuits described herein have been chosen as an explanation for the standard action and performance of the product. When planning to use the product, please ensure that the external conditions are reflected in the actual circuit, assembly, and program designs.
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