OKI semiconductor

MSM5279

DOT MATRIX LCD 80 DOT SEGMENT DRIVER

GENERAL DESCRIPTION

The OKI MSM5279GS is a dot matrix LCD's segment driver LSI which is fabricated by CMOS low power metal gate technology. This LSI consists of 80-bit bidirectional shift register, 80-bit latch, 80-bit level shifter and 80-bit 4-level driver.

It receives the display driving data, which consists of 4-bit parallel, from the LCD controller LSI, then output the LCD driving waveform to the LCD .

The MSM5279GS has the power down function which permits reduced power consumption.

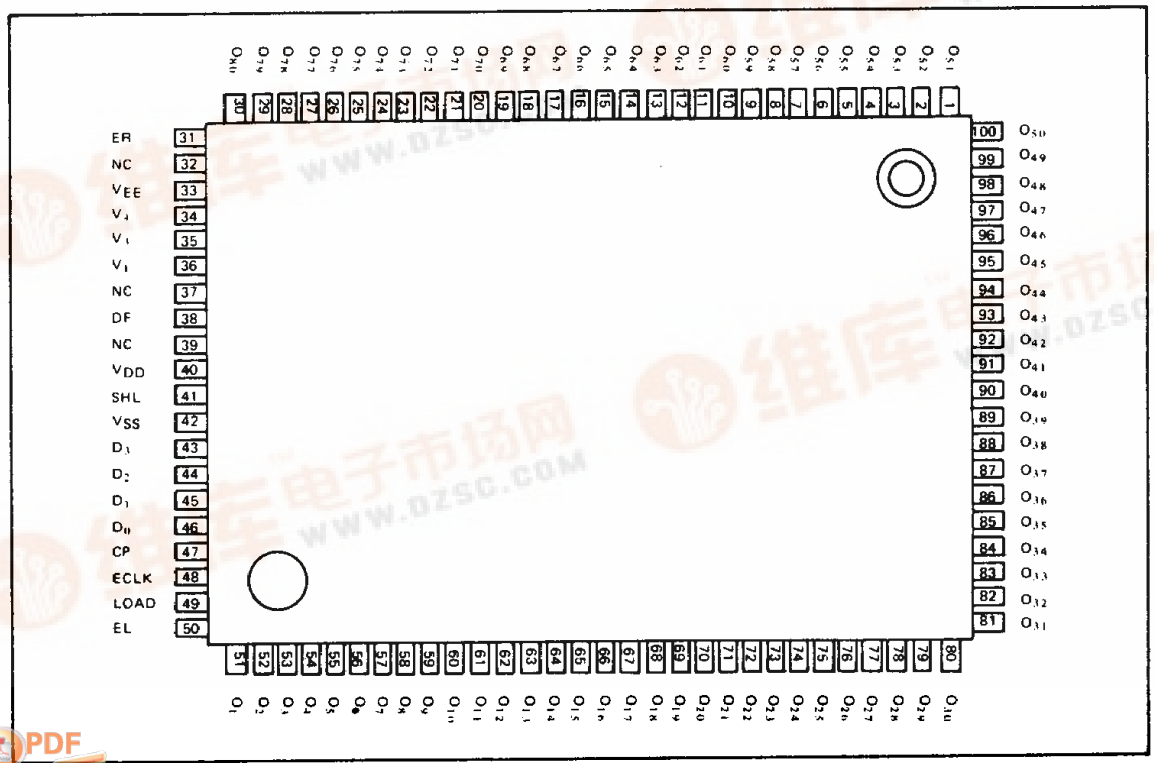
The MSM5279GS can drive a variety of LCD panel because the bias voltage, which determines the LCD driving voltage, can be optionally supplied from the external source.

FEATURES

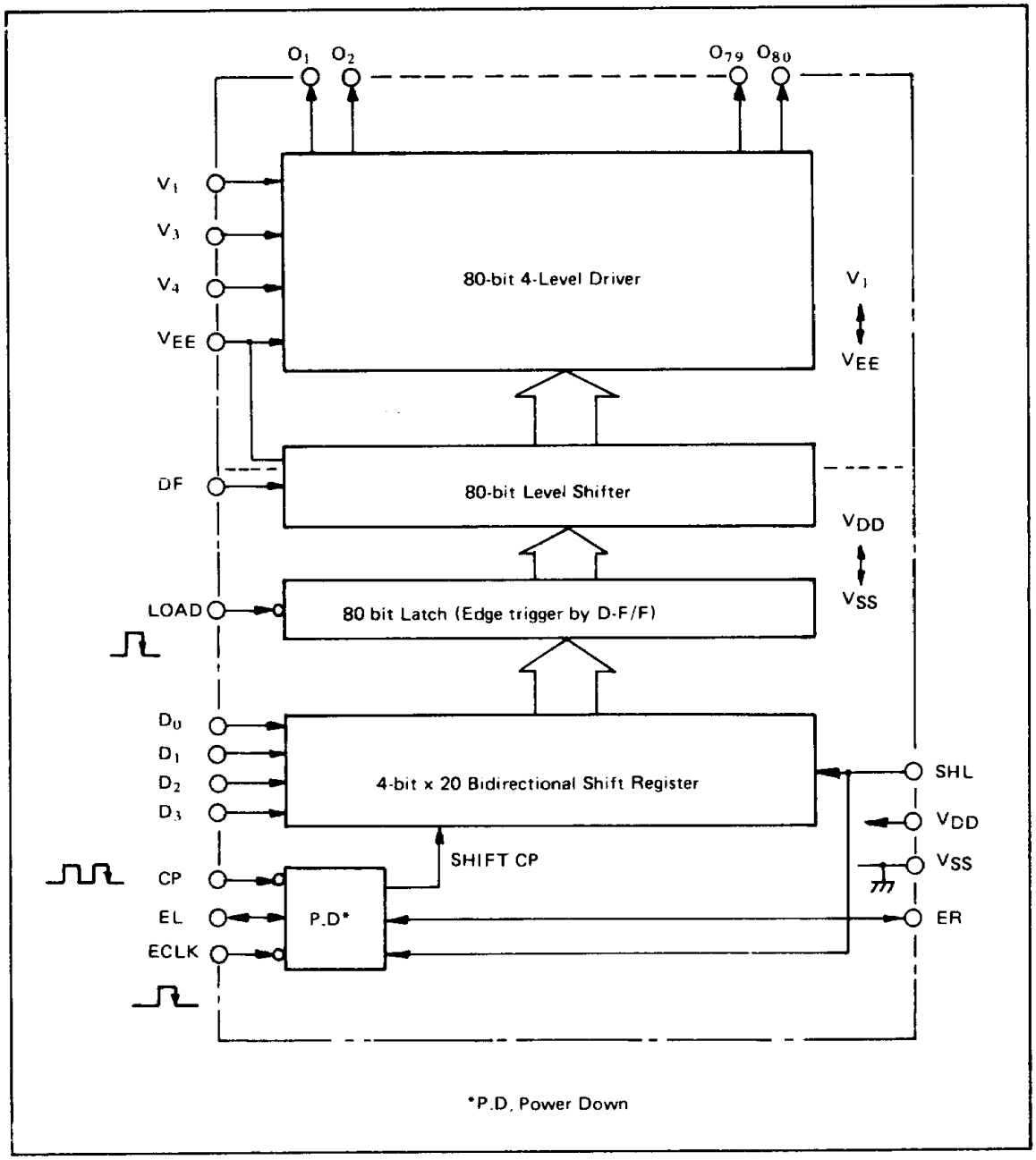
- Supply voltage: 4.5 ~ 5.5V
- LCD driving voltage: 8 ~ 20V
- Applicable LCD duty: 1/16 ~ 1/128
- Bias voltage can be supplied externally
- Power down function
- 4-bit parallel data processing
- Can be interfaced with the MSM6255GS, MSM6265GS, LCD controller LSI
- 100 pin plastic QFP (QFP100-P-1420-K)

PIN CONFIGURATION

(Top view) 100 pin plastic QFP



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Limits	Unit
Supply voltage (1)	V_{DD}	T_a = 25°C	−0.3 ~ 6	V
Supply voltage (2)	$V_{DD} - V_{EE}$*1	T_a = 25°C	0 ~ 22	V
Input voltage	V_I	T_a = 25°C	−0.3 ~ V_{DD} + 0.3	V
Storage temperature	T_{stg}	—	−55 ~ + 150	°C

*1 $V_1 > V_3 > V_4 > V_{EE}$, $V_1 \leqq V_{DD}$

OPERATING RANGE

Parameter	Symbol	Condition	Limits	Unit
Supply voltage (1)	V_{DD}	—	4.5 ~ 5.5	V
Supply voltage (2)	$V_{DD} - V_{EE}$*1	—	8 ~ 20	V
Operating temperature	Top	—	−20 ~ + 85	°C

*1 $V_1 > V_3 > V_4 > V_{EE}$, $V_1 \leqq V_{DD}$

DC CHARACTERISTICS

(V_{DD} = 5V ± 10%, Ta = −20 ~ +85°C)

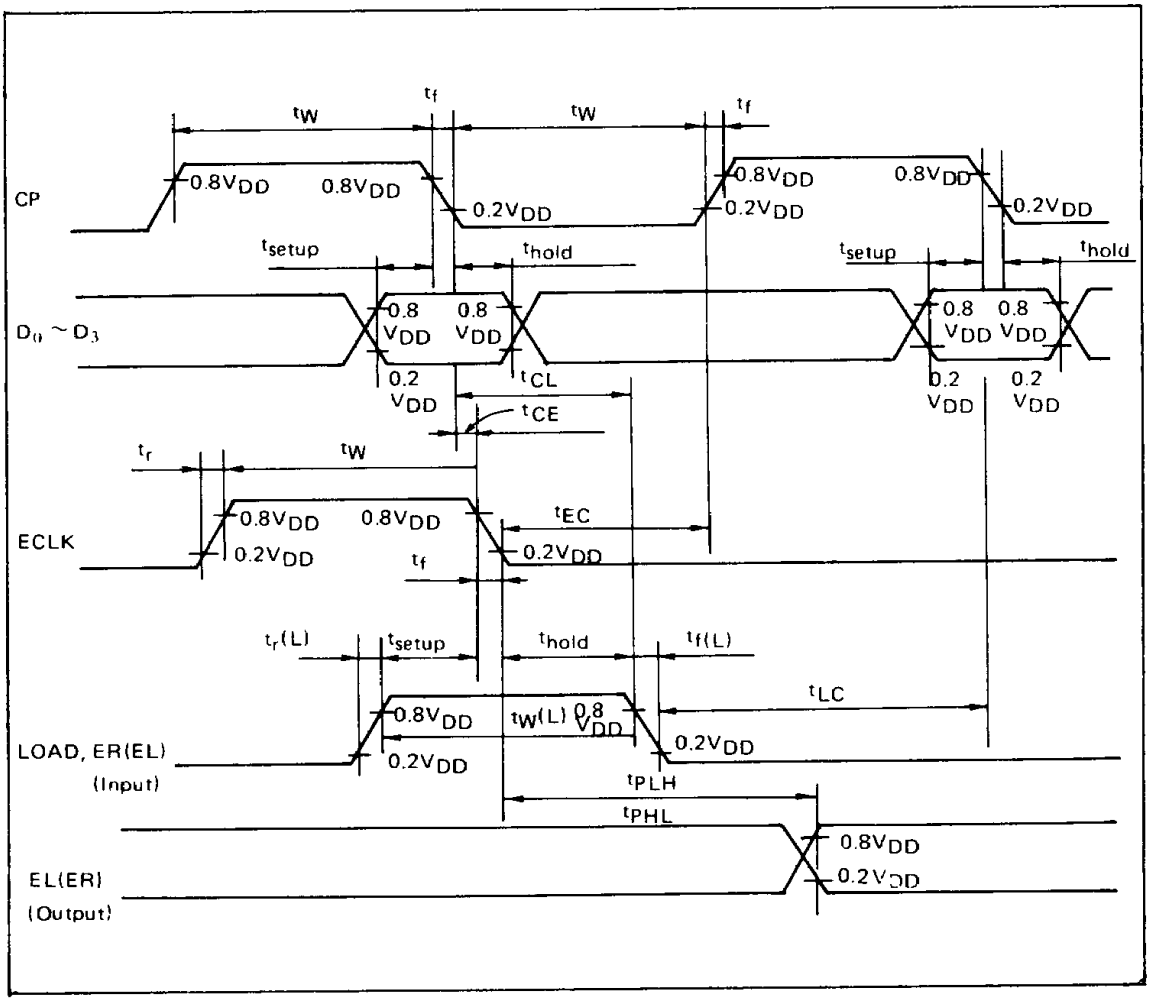
Parameter	Symbol	Condition	MIN	TYP	MAX	Unit
"H" Input voltage	V_{IH}*1	—	0.8V_{DD}	–	–	V
"L" Input voltage	V_{IL}*1	—	–	––	0.2V_{DD}	V
"H" Input current	I_{IH}*1	$V_{IH} = V_{DD}$	–	–	1	μA
"L" Input current	I_{IL}*1	V_{IL} = 0V	–	–	−1	μA
"H" Output voltage	V_{OH}*2	I_O = −0.2mA	V_{DD}− 0.4	–	–	V
"L" Output voltage	V_{OL}*2	I_O = 0.2mA	–	–	0.4	V
ON resistance	R_{ON}*4	$V_{DD} - V_{EE}$ = 18V $\lvert V_N - V_O \rvert$ = 0.25V	–	2	4	kΩ
Stand-by current consumption	$I_{DD}SBY$	CP = 1 MHz $V_{DD} - V_{EE}$ = 18V, No load*5	–	–	200	μA
Current consumption (1)	I_{DD1}	CP = 1 MHz $V_{DD} - V_{EE}$ = 18V, No load*6	–	–	4	mA
Current consumption (2)	I_V	CP = 1 MHz $V_{DD} - V_{EE}$ = 18V, No load*7	–	–	±100	μA
Input capacitance	C_I	f = 1 MHz	–	5	–	PF

*1 Applicable to LOAD, CP, $D_0 \sim D_3$, ECLK, EL, ER, SHL, DF terminals.
*2 Applicable to EL, ER terminals.
*3 $V_N = V_{DD} \sim V_{EE}$ $V_3 = \frac{9}{11}(V_{DD} - V_{EE})$, $V_2 = \frac{2}{11}(V_{DD} - V_{EE})$, $V_{DD} = V_1$.
*4 Applicable to $O_1 \sim O_{80}$ terminals.
*5 Display data 1010 – DF = 40Hz, Current from V_{DD} to V_{SS} when the display data is not processing.
*6 Display data 1010 – DF = 40Hz, Current from V_{DD} to V_{SS} when the display data is processing.
*7 Display data 1010 – DF = 40Hz, Current on V_1, V_3, V_4 and V_{EE} terminals.

SWITCHING CHARACTERISTICS

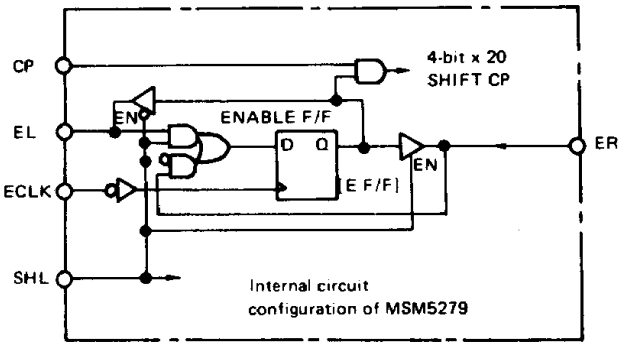
(V_{DD} = 5V ± 10%, T_a = −20 ~ +85°C CL = 15pF)

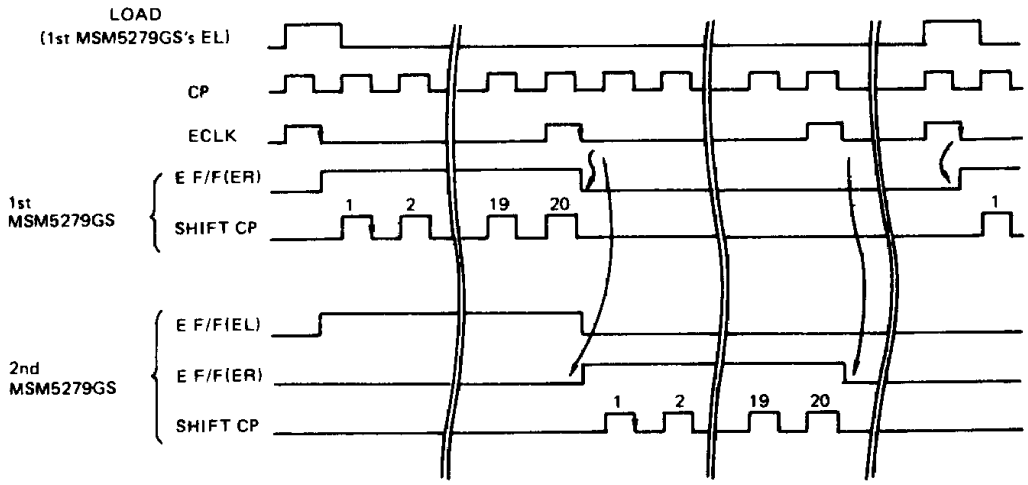
Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
"H", "L" propagation delay time	t_{PLH}, t_{PHL}	—	–	–	250	ns
MAX. clock frequency	f_{CP}	DUTY = 50%	3	–	–	MHz
CP ELCK pulse width	t_W	—	125	–	–	ns
Load pulse width	$t_{W(L)}$	—	125	–	–	ns
Data set-up time	t_{setup}	—	100	–		ns
CP → LOAD time	t_{CL}	—	250	–	–	ns
LOAD → CP time	t_{LC}	—	0	–	–	ns
Data hold time CP → D_0 ~ D_3, ECLK → LOAD	t_{hold}	—	100	–	–	ns
Clock pulse Rising/Falling time	t_r t_f	—	–	–	50	ns
Load pulse Rising/Falling time	$t_{r(L)}$ $t_{f(L)}$	—	–	–	1	μs
CP → ECLK time	t_{CE}	—	0	–	–	ns
ECLK → CP time	t_{EC}	—	150	–	–	ns



POWER DOWN FUNCTION

When more than two MSM5279GSs are being connected in series, cascade connection, power down function of MSM5279GS can be utilized using the ENABLE F/F (flip flop circuit) in individual MSM5279GSs. (Regarding the internal circuit configuration of MSM5279GS, refer to the figure below.) The display data is processed only in the MSM5279GS, the ENABLE F/F of which is being activated by setting its ER and EL at high level, while the display data is not processed in the MSM5279GS, the ENABLE F/F of which is not being activated and the low power consumption condition (I_{DD} SBY) is being held. The activated condition of this ENABLE F/F is being shifted to next MSM5279GS one after another so that the ENABLE F/F of only one MSM5279GS out of the cascade connected MSM5279GSs should be being activated.





SHL = "H" (EL = Input ER = Output)
First MSM5279GS's ER should be
connected to second MSM5279GS's EL

Timing chart when MSM5279GS's are connected in series (cascade connection)

PIN DESCRIPTION

- **ER, EL**

Pin	Input/Output	SHL	Description
ER	Input	L	Input pin to ENABLE F/F of MSM5279GS.
EL	Output		Output pin of ENABLE F/F. EL is connected to next MSM5279GS's ER when MSM5279GSs are connected in series (cascade connection).
EL	Input	H	Input pin to ENABLE F/F of MSM5279GS.
ER	Output		Output pin of ENABLE F/F. ER is connected to next MSM5279GS's EL when MSM5279GSs are connected in series (cascade connection).

- **ELCK**
  Clock pulse input pin for ENABLE F/F. The active condition of ENABLE F/F is shifted to next MSM5279GS's ENABLE F/F at the falling edge of the clock pulse. ELCK is required every 20 CP. (Clock Pulse).

- **CP**
  Clock pulse input pin for the 4-bit parallel shift register. The data is shifted to 80-bit latch at the falling edge of the clock pulse. The clock pulse, which was input when the ENABLE F/F is not active condition, is invalid.

- **SHL**
  ER and EL can be used as either input pin or output pin according to the H/L condition of SHL. The shifting direction of each data, $D_0 \sim D_3$, the Input/Output condition of ER and EL and the H/L condition of SHL are described in the table below.

SHL	ER	EL	Shifting direction
L	Input	Output	$D_0 \rightarrow O_1 \rightarrow O_5 \longrightarrow O_{77}$ $D_1 \rightarrow O_2 \rightarrow O_6 \longrightarrow O_{78}$ $D_2 \rightarrow O_3 \rightarrow O_7 \longrightarrow O_{79}$ $D_3 \rightarrow O_4 \rightarrow O_8 \longrightarrow O_{80}$
H	Output	Input	$D_0 \rightarrow O_{80} \rightarrow O_{76} \longrightarrow O_4$ $D_1 \rightarrow O_{79} \rightarrow O_{75} \longrightarrow O_3$ $D_2 \rightarrow O_{78} \rightarrow O_{74} \longrightarrow O_2$ $D_3 \rightarrow O_{77} \rightarrow O_{73} \longrightarrow O_1$ ↑ end data ↑ start data

- **D_0, D_1, D_2, D_3**
  Data input pins for 4-bit parallel shift register and it is input synchronized with the clock pulse. The combination of $D_0 \sim D_3$ level, DF signal, display data output level and the display on the LCD panel is described on the table below.

$D_0 \sim D_3$	DF	Display data output level	Display on the LCD
L	L	V_3	OFF
H	L	V_1	ON
L	H	V_4	OFF
H	H	V_{EE}	ON

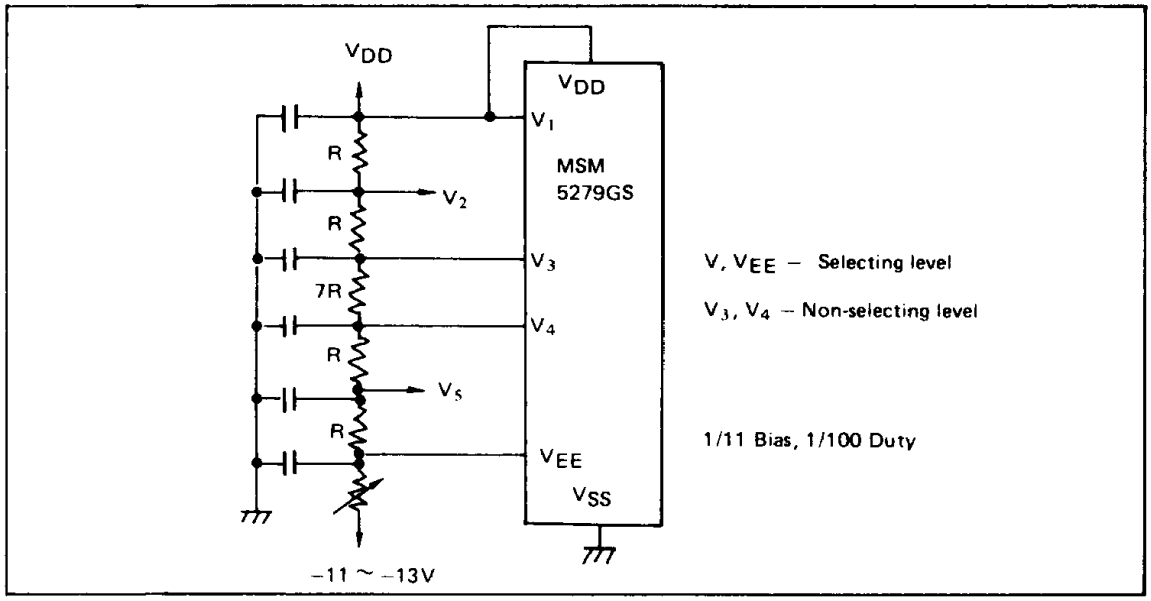
- **LOAD**
  The signal for latching the shift register contents is input from this pin. When LOAD pin is set at "H" level, the shift register contents are transferred to 80-bit latch at the falling edge of the LOAD pulse.

  When more than two MSM5279GSs are connected in series, cascade connection, the first MSM5279GS's EL terminal (when SHL = "H") or ER terminal (when SHL = "L") should be connected with first MSM5279GS's LOAD terminal.

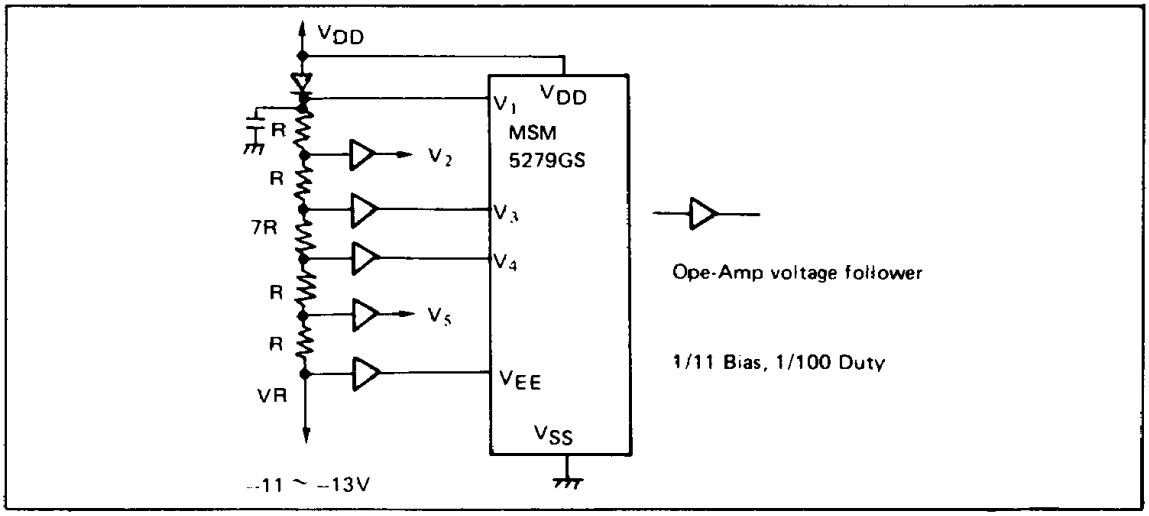
- **DF**
  Alternate signal input pin for LCD driving. Frame inversion signal is input to this terminal.

- **V_{DD}, V_{SS}**
  Supply voltage pins. V_{DD} should be 4.5 ~ 5.5V. V_{SS} is a ground pin (V_{SS} = 0V)

- **V_1, V_3, V_4, V_{EE}**
  Bias supply voltage pin to drive the LCD. Bias voltage divided by the resistance is usually used as supply voltage source. The figure below shows the case when bias voltage, which determines the LCD driving voltage, is supplied from the external source. V_1 is not necessarily connected with V_{DD}.



The figure below shows the case when the bias voltage is supplied by using Ope-Amps, which enables the bias source low impedance and low power consumption.



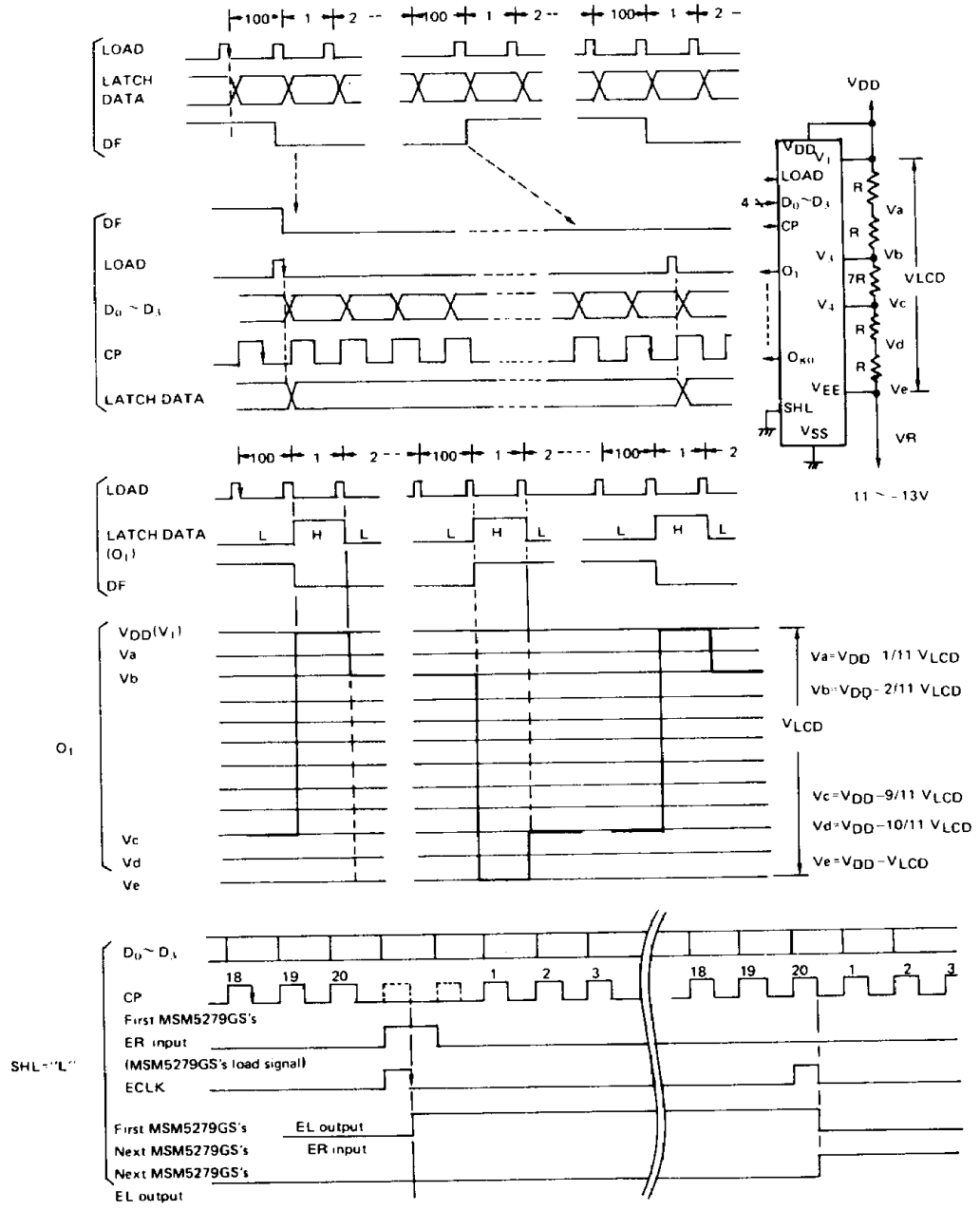
- **O_1 ~ O_{80}**
  Display data output pin which corresponds to the respective latch contents. One of V_1, V_3, V_4 and V_{EE} is selected as a display driving voltage source according to the combination of the latched data level and DF signal. (Refer to the truth table on the right).

DF	Latched data	Display data output level
L	L	V_3
L	H	V_1
H	L	V_4
H	H	V_{EE}

Truth table

TIMING CHART

1/100 duty, 1/11 Bias



Interface with MSM6255GS

APPLICATION CIRCUIT