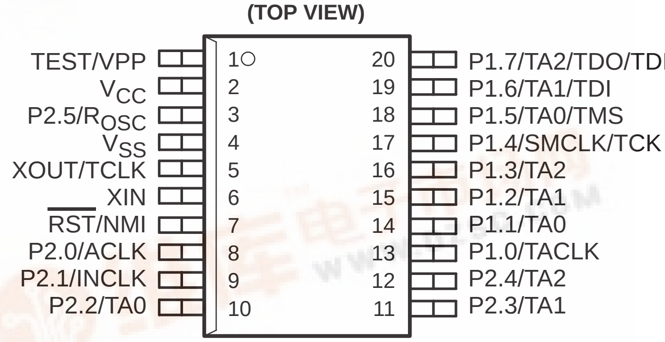
- **Low Supply Voltage Range 2.5 V to 5.5 V**
- **Ultralow-Power Consumption:**
  - **Active Mode: 330 µA at 1 MHz, 3 V**
  - **Standby Mode: 1.5 µA**
  - **Off Mode (RAM Retention): 0.1 µA**
- **Wake-up From Standby Mode in less than 6 µs**
- **16-Bit RISC Architecture, 200 ns Instruction Cycle Time**
- **Basic Clock Module Configurations:**
  - **Various Internal Resistors**
  - **Single External Resistor**
  - **32 kHz Crystal**
  - **High Frequency Crystal**
  - **Resonator**
  - **External Clock Source**
- **16-Bit Timer_A With Three Capture/Compare Registers**
- **Serial Onboard Programming**
- **Program Code Protection by Security Fuse**
- **Family Members Include:**
  MSP430C111: 2k Byte ROM, 128 Byte RAM
  MSP430C112: 4k Byte ROM, 256 Byte RAM
  MSP430P112: 4k Byte OTP, 256 Byte RAM
- **EPROM Version Available for Prototyping:**
  - **PMS430E112: 4k Byte EPROM, 256 Byte RAM**
- **Available in a 20-Pin Plastic Small-Outline Wide Body (SOWB) Package, 20-Pin Ceramic Dual-In-Line (CDIP) Package (EPROM Only)**
- **For Complete Module Descriptions, Refer to the *MSP430x1xx Family User's Guide*, Literature Number SLAU049**

description

DW PACKAGE
(TOP VIEW)



The Texas Instruments MSP430 family of ultralow power microcontrollers consist of several devices featuring different sets of peripherals targeted for various applications. The architecture, combined with five low power modes is optimized to achieve extended battery life in portable measurement applications. The device features a powerful 16-bit RISC CPU, 16-bit registers, and constant generators that attribute to maximum code efficiency. The digitally controlled oscillator (DCO) allows wake-up from low-power modes to active mode in less than 6µs.

The MSP430x11x series is an ultra low-power mixed signal microcontroller with a built in 16-bit timer and fourteen I/O pins.

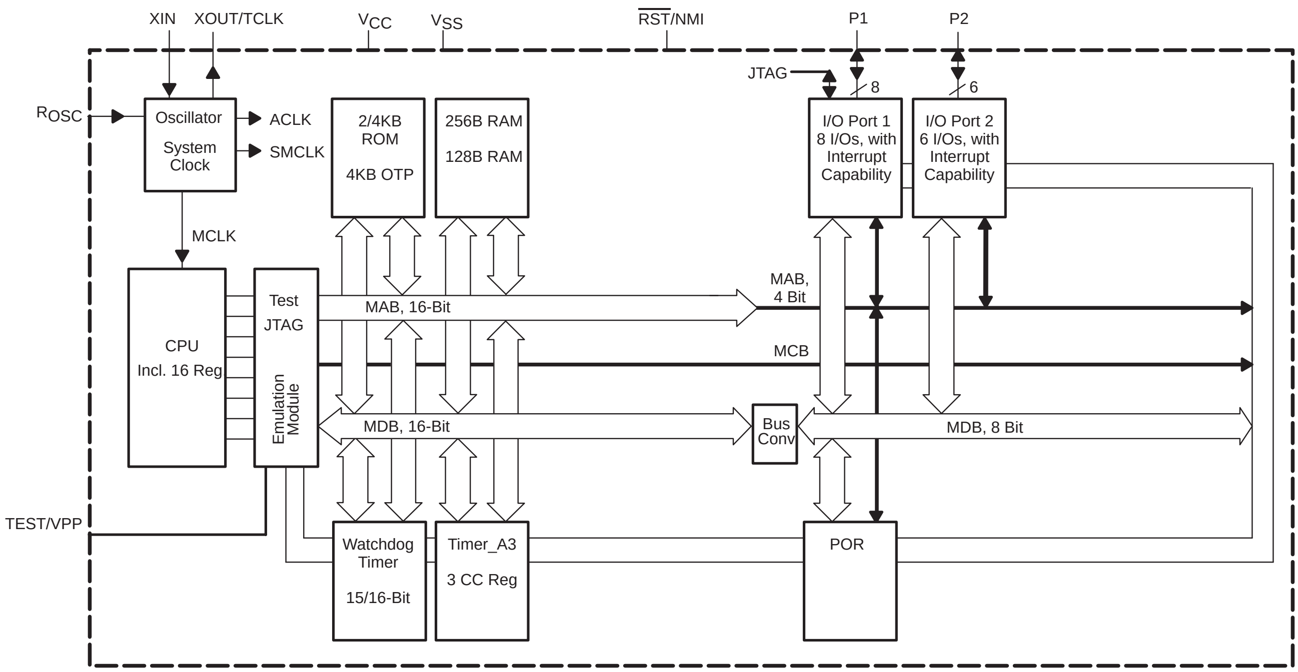
Typical applications include sensor systems that capture analog signals, convert them to digital values, and then process the data and display them or transmit them to a host system. Stand alone RF sensor front-end is another area of application.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

AVAILABLE OPTIONS

T_A	PACKAGED DEVICES	
	SOWB 20-Pin (DW)	**CDIP 20-Pin (JL)**
−40°C to 85°C	MSP430C111IDW MSP430C112IDW MSP430P112IDW	
25°C	—	PMS430E112JL

functional block diagram



Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
P1.0/TACLK	13	I/O	General-purpose digital I/O pin/Timer_A, clock signal TACLK input
P1.1/TA0	14	I/O	General-purpose digital I/O pin/Timer_A, Capture: CCI0A input, Compare: Out0 output
P1.2/TA1	15	I/O	General-purpose digital I/O pin/Timer_A, Capture: CCI1A input, Compare: Out1 output
P1.3/TA2	16	I/O	General-purpose digital I/O pin/Timer_A, Capture: CCI2A input, Compare: Out2 output
P1.4/SMCLK/TCK	17	I/O	General-purpose digital I/O pin/SMCLK signal output/Test clock, input terminal for device programming and test
P1.5/TA0/TMS	18	I/O	General-purpose digital I/O pin/Timer_A, Compare: Out0 output/test mode select, input terminal for device programming and test.
P1.6/TA1/TDI	19	I/O	General-purpose digital I/O pin/Timer_A, Compare: Out1 output/test data input terminal.
P1.7/TA2/TDO/TDI	20	I/O	General-purpose digital I/O pin/Timer_A, Compare: Out2 output/test data output terminal or data input during programming.
P2.0/ACLK	8	I/O	General-purpose digital I/O pin/ACLK output
P2.1/INCLK	9	I/O	General-purpose digital I/O pin/Timer_A, clock signal at INCLK
P2.2/TA0	10	I/O	General-purpose digital I/O pin/Timer_A, Capture: CCI0B input, Compare: Out0 output
P2.3/TA1	11	I/O	General-purpose digital I/O pin/Timer_A, Capture: CCI1B input, Compare: Out1 output
P2.4/TA2	12	I/O	General-purpose digital I/O pin/Timer_A, Compare: Out2 output
P2.5/R_{OSC}	3	I/O	General-purpose digital I/O pin/Input for external resistor that defines the DCO nominal frequency
$\overline{RST}$/NMI	7	I	Reset or nonmaskable interrupt input
TEST/VPP	1	I	Selects test mode for JTAG pins on Port1/programming voltage input during EPROM programming
V_{CC}	2		Supply voltage
V_{SS}	4		Ground reference
XIN	6	I	Input terminal of crystal oscillator
XOUT/TCLK	5	I/O	Output terminal of crystal oscillator or test clock input

short-form description

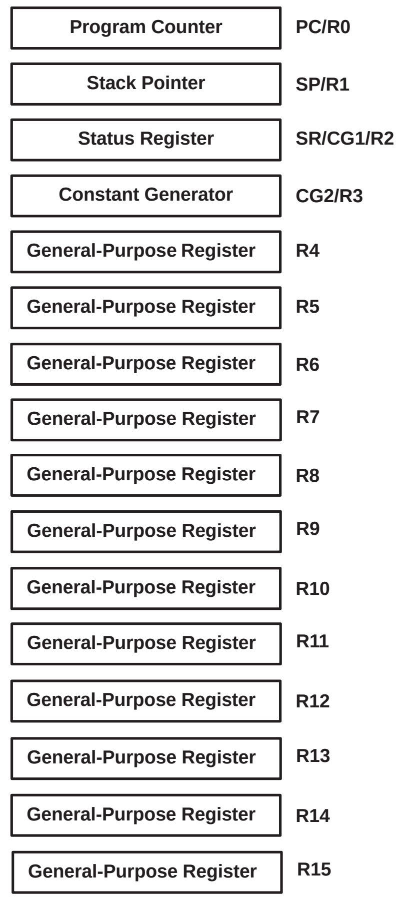
CPU

The MSP430 CPU has a 16-bit RISC architecture that is highly transparent to the application. All operations, other than program-flow instructions, are performed as register operations in conjunction with seven addressing modes for source operand and four addressing modes for destination operand.

The CPU is integrated with 16 registers that provide reduced instruction execution time. The register-to-register operation execution time is one cycle of the CPU clock.

Four of the registers, R0 to R3, are dedicated as program counter, stack pointer, status register, and constant generator respectively. The remaining registers are general-purpose registers.

Peripherals are connected to the CPU using data, address, and control buses, and can be handled with all instructions.



instruction set

The instruction set consists of 51 instructions with three formats and seven address modes. Each instruction can operate on word and byte data. Table 1 shows examples of the three types of instruction formats; the address modes are listed in Table 2.

Table 1. Instruction Word Formats

Dual operands, source-destination	e.g. ADD R4,R5	R4 + R5 −−−> R5
Single operands, destination only	e.g. CALL R8	PC −−>(TOS), R8−−> PC
Relative jump, un/conditional	e.g. JNE	Jump-on-equal bit = 0

Table 2. Address Mode Descriptions

ADDRESS MODE	S	D	SYNTAX	EXAMPLE	OPERATION
Register	●	●	MOV Rs,Rd	MOV R10,R11	R10 −−> R11
Indexed	●	●	MOV X(Rn),Y(Rm)	MOV 2(R5),6(R6)	M(2+R5)−−> M(6+R6)
Symbolic (PC relative)	●	●	MOV EDE,TONI		M(EDE) −−> M(TONI)
Absolute	●	●	MOV &MEM,&TCDAT		M(MEM) −−> M(TCDAT)
Indirect	●		MOV @Rn,Y(Rm)	MOV @R10,Tab(R6)	M(R10) −−> M(Tab+R6)
Indirect autoincrement	●		MOV @Rn+,Rm	MOV @R10+,R11	M(R10) −−> R11 R10 + 2−−> R10
Immediate	●		MOV #X,TONI	MOV #45,TONI	#45 −−> M(TONI)

NOTE: S = source D = destination

operating modes

The MSP430 has one active mode and five software selectable low-power modes of operation. An interrupt event can wake up the device from any of the five low-power modes, service the request and restore back to the low-power mode on return from the interrupt program.

The following six operating modes can be configured by software:

- Active mode AM;
  - All clocks are active
- Low-power mode 0 (LPM0);
  - CPU is disabled
    ACLK and SMCLK remain active. MCLK is disabled
- Low-power mode 1 (LPM1);
  - CPU is disabled
    ACLK and SMCLK remain active. MCLK is disabled
    DCO's dc-generator is disabled if DCO not used in active mode
- Low-power mode 2 (LPM2);
  - CPU is disabled
    MCLK and SMCLK are disabled
    DCO's dc-generator remains enabled
    ACLK remains active
- Low-power mode 3 (LPM3);
  - CPU is disabled
    MCLK and SMCLK are disabled
    DCO's dc-generator is disabled
    ACLK remains active
- Low-power mode 4 (LPM4);
  - CPU is disabled
    ACLK is disabled
    MCLK and SMCLK are disabled
    DCO's dc-generator is disabled
    Crystal oscillator is stopped

interrupt vector addresses

The interrupt vectors and the power-up starting address are located in the ROM with an address range of 0FFFFh-0FFE0h. The vector contains the 16-bit address of the appropriate interrupt handler instruction sequence.

INTERRUPT SOURCE	INTERRUPT FLAG	SYSTEM INTERRUPT	WORD ADDRESS	PRIORITY
Power-up, external reset, watchdog	WDTIFG (see Note1)	Reset	0FFFEh	15, highest
NMI, oscillator fault	NMIIFG, OFIFG (see Note 1)	(non)-maskable, (non)-maskable	0FFFCh	14
			0FFFAh	13
			0FFF8h	12
			0FFF6h	11
Watchdog Timer	WDTIFG	maskable	0FFF4h	10
Timer_A3	TACCR0 CCIFG (see Note 2)	maskable	0FFF2h	9
Timer_A3	TACCR1 and TACCR2 CCIFGs, TAIFG (see Notes 1 and 2)	maskable	0FFF0h	8
			0FFEEh	7
			0FFECh	6
			0FFEAh	5
			0FFE8h	4
I/O Port P2 (eight flags − see Note 3)	P2IFG.0 to P2IFG.7 (see Notes 1 and 2)	maskable	0FFE6h	3
I/O Port P1 (eight flags)	P1IFG.0 to P1IFG.7 (see Notes 1 and 2)	maskable	0FFE4h	2
			0FFE2h	1
			0FFE0h	0, lowest

NOTES: 1. Multiple source flags
2. Interrupt flags are located in the module
3. There are eight Port P2 interrupt flags, but only six Port P2 I/O pins (P2.0−5) are implemented on the ’11x devices.

special function registers

Most interrupt and module enable bits are collected into the lowest address space. Special function register bits that are not allocated to a functional purpose are not physically present in the device. Simple software access is provided with this arrangement.

interrupt enable 1

Address	7	6	5	4	3	2	1	0
0h				NMIIE			OFIE	WDTIE
				rw-0			rw-0	rw-0

WDTIE: Watchdog Timer interrupt enable. Inactive if watchdog mode is selected. Active if Watchdog Timer is configured in interval timer mode.
OFIE: Oscillator fault enable
NMIIE: (Non)maskable interrupt enable

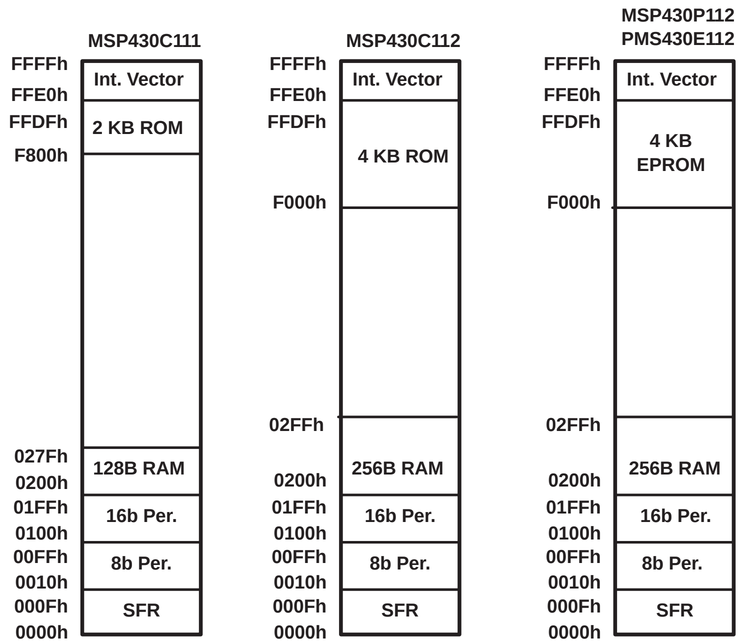
interrupt flag register 1

Address	7	6	5	4	3	2	1	0
02h				NMIIFG			OFIFG	WDTIFG
				rw-0			rw-1	rw-(0)

WDTIFG: Set on Watchdog Timer overflow (in watchdog mode) or security key violation.
Reset on V_{CC} power-up or a reset condition at $\overline{RST}$/NMI pin in reset mode.
OFIFG: Flag set on oscillator fault
NMIIFG: Set via $\overline{RST}$/NMI-pin

Legend		
	rw:	Bit can be read and written.
	rw-0,1:	Bit can be read and written. It is Reset or Set by PUC
	rw-(0,1):	Bit can be read and written. It is Reset or Set by POR
	(shaded box)	SFR bit is not present in device.

memory organization



peripherals

Peripherals are connected to the CPU through data, address, and control busses and can be handled using all instructions. For complete module descriptions, refer to the MSP430x1xx Family User's Guide, literature number SLAU049.

oscillator and system clock

The clock system is supported by the basic clock module that includes support for a 32768-Hz watch crystal oscillator, an internal digitally-controlled oscillator (DCO) and a high frequency crystal oscillator. The basic clock module is designed to meet the requirements of both low system cost and low-power consumption. The internal DCO provides a fast turn-on clock source and stabilizes in less than 6 µs. The basic clock module provides the following clock signals:

- Auxiliary clock (ACLK), sourced from a 32768-Hz watch crystal or a high frequency crystal.
- Main clock (MCLK), the system clock used by the CPU.
- Sub-Main clock (SMCLK), the sub-system clock used by the peripheral modules.

digital I/O

There are two 8-bit I/O ports implemented—ports P1 and P2 (only six P2 I/O signals are available on external pins):

- All individual I/O bits are independently programmable.
- Any combination of input, output, and interrupt conditions is possible.
- Edge-selectable interrupt input capability for all the eight bits of port P1 and six bits of port P2.
- Read/write access to port-control registers is supported by all instructions.

NOTE:

Six bits of Port P2, P2.0 to P2.5, are available on external pins − but all control and data bits for Port P2 are implemented.

watchdog timer

The primary function of the watchdog timer (WDT) module is to perform a controlled system restart after a software problem occurs. If the selected time interval expires, a system reset is generated. If the watchdog function is not needed in an application, the module can be configured as an interval timer and can generate interrupts at selected time intervals.

timer_A3

Timer_A3 is a 16-bit timer/counter with three capture/compare registers. Timer_A3 can support multiple capture/compares, PWM outputs, and interval timing. Timer_A3 also has extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each of the capture/compare registers.

Timer_A3 Signal Connections

Input Pin Number	Device Input Signal	Module Input Name	Module Block	Module Output Signal	Output Pin Number
13 - P1.0	TACLK	TACLK	Timer	NA	
	ACLK	ACLK			
	SMCLK	SMCLK			
9 - P2.1	INCLK	INCLK			
14 - P1.1	TA0	CCI0A	CCR0	TA0	14 - P1.1
10 - P2.2	TA0	CCI0B			18 - P1.5
	DV_{SS}	GND			10 - P2.2
	DV_{CC}	V_{CC}			
15 - P1.2	TA1	CCI1A	CCR1	TA1	15 - P1.2
11 - P2.3	TA1	CCI1B			19 - P1.6
	DV_{SS}	GND			11 - P2.3
	DV_{CC}	V_{CC}			
16 - P1.3	TA2	CCI2A	CCR2	TA2	16 - P1.3
	ACLK (internal)	CCI2B			20 - P1.7
	DV_{SS}	GND			12 - P2.4
	DV_{CC}	V_{CC}			

peripheral file map

PERIPHERALS WITH WORD ACCESS			
Watchdog	Watchdog/Timer Control	WDTCTL	0120h
Timer_A	Timer_A Interrupt Vector Timer_A Control Cap/Com Control Cap/Com Control Cap/Com Control Reserved Reserved Reserved Reserved Timer_A Register Cap/Com Register Cap/Com Register Cap/Com Register Reserved Reserved Reserved Reserved	TAIV TACTL TACCTL0 TACCTL1 TACCTL2 TAR TACCR0 TACCR1 TACCR2	012Eh 0160h 0162h 0164h 0166h 0168h 016Ah 016Ch 016Eh 0170h 0172h 0174h 0176h 0178h 017Ah 017Ch 017Eh
PERIPHERALS WITH BYTE ACCESS			
Basic Clock	Basic Clock Sys. Control2 Basic Clock Sys. Control1 DCO Clock Freq. Control	BCSCTL2 BCSCTL1 DCOCTL	058h 057h 056h
EPROM	EPROM Control	EPCTL	054h
Port P2	Port P2 Selection Port P2 Interrupt Enable Port P2 Interrupt Edge Select Port P2 Interrupt Flag Port P2 Direction Port P2 Output Port P2 Input	P2SEL P2IE P2IES P2IFG P2DIR P2OUT P2IN	02Eh 02Dh 02Ch 02Bh 02Ah 029h 028h
Port P1	Port P1 Selection Port P1 Interrupt Enable Port P1 Interrupt Edge Select Port P1 Interrupt Flag Port P1 Direction Port P1 Output Port P1 Input	P1SEL P1IE P1IES P1IFG P1DIR P1OUT P1IN	026h 025h 024h 023h 022h 021h 020h
Special Function	SFR Interrupt Flag1 SFR Interrupt Enable1	IFG1 IE1	002h 000h

absolute maximum ratings†

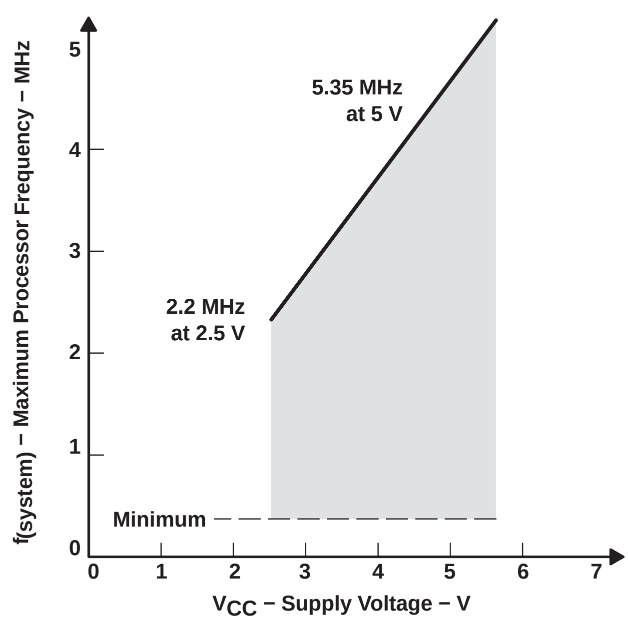
Voltage applied at V_{CC} to V_{SS} . . . . −0.3 V to 6 V
Voltage applied to any pin (see Note) . . . . −0.3 V to V_{CC}+0.3 V
Diode current at any device terminal . . . . ±2 mA
Storage temperature, T_{stg} (unprogrammed device) . . . . −55°C to 150°C
Storage temperature, T_{stg} (programmed device) . . . . −40°C to 85°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE: All voltages referenced to V_{SS}. The JTAG fuse-blow voltage, V_{FB}, is allowed to exceed the absolute maximum rating. The voltage is applied to the TEST pin when blowing the JTAG fuse.

recommended operating conditions

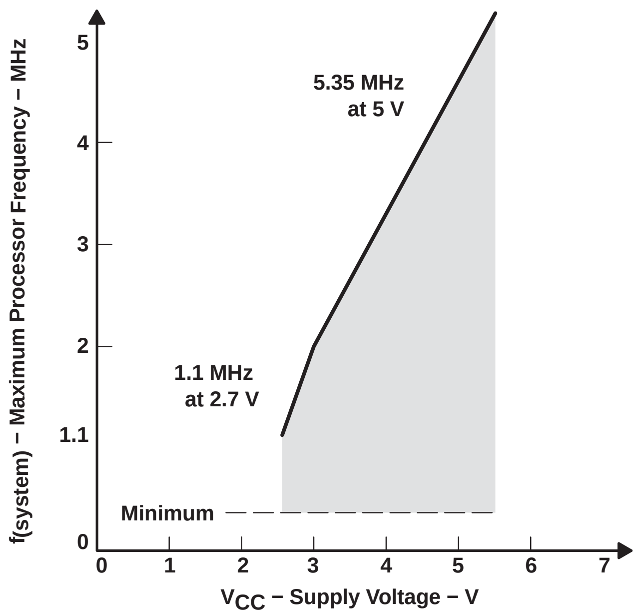
		MIN	NOM	MAX	UNITS
Supply voltage, V_{CC}	MSP430C11x	2.5		5.5	V
	MSP430P112	2.7		5.5	
	PMS430E112	2.7		5.5	V
Supply voltage during programming, V_{CC}	MSP430P112	4.5	5	5.5	V
	MSP430E112	4.5	5	5.5	V
Operating free-air temperature range, T_A	MSP430C11x	−40		85	°C
	MSP430P112				
	PMS430E112		25		
XTAL frequency, $f_{(XTAL)}$,(ACLK signal)			32768		Hz
Processor frequency $f_{(system)}$ (PMS430P/E112) (MCLK signal)	V_{CC} = 3 V	dc		2	MHz
	V_{CC} = 5 V	dc		5.35	
Processor frequency $f_{(system)}$ (MCLK signal) (MSP430C11x)	V_{CC} = 3 V	dc		2.73	MHz
	V_{CC} = 5 V	dc		5.35	



NOTE: Minimum processor frequency is defined by system clock.

Figure 1. C Version Frequency vs Supply Voltage

recommended operating conditions (continued)



NOTE: Minimum processor frequency is defined by system clock.

Figure 2. P/E Version Frequency vs Supply Voltage

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

supply current (into V_{CC}) excluding external current

PARAMETER			TEST CONDITIONS			MIN	NOM	MAX	UNIT
$I_{(AM)}$	Active mode	C11x	T_A = −40°C +85°C, $f_{(MCLK)} = f_{(SMCLK)}$ = 1 MHz, $f_{(ACLK)}$ = 32,768 Hz		V_{CC} = 3 V		330	400	µA
					V_{CC} = 5 V		630	700	
			T_A = −40°C +85°C, $f_{(MCLK)} = f_{(SMCLK)} = f_{(ACLK)}$ = 4096 Hz		V_{CC} = 3 V		3.4	4	µA
					V_{CC} = 5 V		7.8	10	
		P112	T_A = −40°C +85°C, $f_{MCLK} = f_{(SMCLK)}$ = 1 MHz, $f_{(ACLK)}$ = 32,768 Hz		V_{CC} = 3 V		400	500	µA
					V_{CC} = 5 V		730	900	
			T_A = −40°C +85°C, $f_{(MCLK)} = f_{(SMCLK)} = f_{(ACLK)}$ = 4096 Hz		V_{CC} = 3 V		3.4	4	µA
					V_{CC} = 5 V		7.8	10	
$I_{(CPUOff)}$	Low power mode, (LPM0)	C11x	T_A = −40°C +85°C, f_{MCLK} = 0 MHz, $f_{(SMCLK)}$ = 1 MHz, $f_{(ACLK)}$ = 32,768 Hz		V_{CC} = 3 V		51	60	µA
					V_{CC} = 5 V		120	150	
		P112	T_A = −40°C +85°C, $f_{(MCLK)}$ = 0 MHz, $f_{(SMCLK)}$ = 1 MHz, $f_{(ACLK)}$ = 32,768 Hz		V_{CC} = 3 V		70	85	
					V_{CC} = 5 V		125	170	
$I_{(LPM2)}$	Low power mode, (LPM2)		T_A = −40°C +85°C, $f_{(MCLK)} = f_{(SMCLK)}$ = 0 MHz, $f_{(ACLK)}$ = 32,768 Hz, SCG0 = 0, Rsel = 3		V_{CC} = 3 V		8	22	µA
					V_{CC} = 5 V		16	35	
$I_{(LPM3)}$	Low power mode, (LPM3)		T_A = −40°C	$f_{(MCLK)} = f_{(SMCLK)}$ = 0 MHz, $f_{(ACLK)}$ = 32,768 Hz, SCG0 = 1	V_{CC} = 3 V		2	2.6	µA
			T_A = 25°C				1.5	2.2	
			T_A = 85°C				1.85	2.2	
			T_A = −40°C	$f_{(MCLK)} = f_{(SMCLK)}$ = 0 MHz, $f_{(ACLK)}$ = 32,768 Hz, SCG0 = 1	V_{CC} = 5 V		6.3	8	
			T_A = 25°C				5.1	7	
			T_A = 85°C				5.1	7	
$I_{(LPM4)}$	Low power mode, (LPM4)		T_A = −40°C	$f_{(MCLK)} = f_{(SMCLK)}$ = 0 MHz, $f_{(ACLK)}$ = 0 Hz, SCG0 = 1	V_{CC} = 3 V/ 5 V		0.1	0.8	µA
			T_A = 25°C				0.1	0.8	
			T_A = 85°C				0.4	1	

NOTE: All inputs are tied to V_{SS} or V_{CC}. Outputs do not source or sink any current.

current consumption of active mode versus system frequency

$$I_{AM} = I_{AM[1\ MHz]} \times f_{system}\ [MHz]$$

current consumption of active mode versus supply voltage

$$I_{AM} = I_{AM[3\ V]} + 175\ \mu A/V \times (V_{CC} - 3\ V)$$

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

Schmitt-trigger inputs Port 1 to Port P2; P1.0 to P1.7, P2.0 to P2.5

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
V_{IT+}	Positive-going input threshold voltage	V_{CC} = 3 V	1.2		2.1	V
		V_{CC} = 5 V	2.3		3.4	
V_{IT-}	Negative-going input threshold voltage	V_{CC} = 3 V	0.7		1.5	V
		V_{CC} = 5 V	1.4		2.3	
V_{hys}	Input voltage hysteresis, ($V_{IT+} - V_{IT-}$)	V_{CC} = 3 V	0.3		1	V
		V_{CC} = 5 V	0.6		1.4	

standard inputs $\overline{RST}$/NMI, TCK, TMS, TDI

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
V_{IL}	Low-level input voltage	V_{CC} = 3 V/5 V	V_{SS}		V_{SS}+0.8	V
V_{IH}	High-level input voltage		0.7xV_{CC}		V_{CC}	

inputs Px.x, TAx

PARAMETER		TEST CONDITIONS	VCC	MIN	NOM	MAX	UNIT
$t_{(int)}$	External Interrupt timing	Port P1, P2: P1.x to P2.x, External trigger signal for the interrupt flag, (see Note 1)	3 V/ 5 V	1.5			cycle
			3 V	540			ns
			5 V	270			
$t_{(cap)}$	Timer_A, capture timing	TA0, TA1, TA2. (see Note 2)	3 V/ 5 V	1.5			cycle
			3 V	540			ns
			5 V	270			

NOTES: 1. The external signal sets the interrupt flag every time the minimum t_{int} cycle and time parameters are met. It may be set even with trigger signals shorter than t_{int}. Both the cycle and timing specifications must be met to ensure the flag is set.
2. The external capture signal triggers the capture event every time when the minimum t_{cap} cycles and time parameters are met. A capture may be triggered with capture signals even shorter than t_{cap}. Both the cycle and timing specifications must be met to ensure a correct capture of the 16-bit timer value and to ensure the flag is set.

internal signals TAx, SMCLK at Timer_A

PARAMETER		TEST CONDITIONS	VCC	MIN	NOM	MAX	UNIT
$f_{(IN)}$	Input frequency	Internal TA0, TA1, TA2, $t_H = t_L$	3 V	dc		10	MHz
			5 V	dc		15	
$f_{(TAint)}$	Timer_A clock frequency	Internally, SMCLK signal applied	3 V/5 V	dc		f_{System}	

leakage current (see Note 1)

PARAMETER		TEST CONDITIONS		MIN	NOM	MAX	UNIT
$I_{lkg(Px.x)}$	High-impendance leakage current	Port P1: P1.x, 0 ≤ × ≤ 7 (see Note 2)	V_{CC} = 3 V/5 V,			±50	nA
		Port P2: P2.x, 0 ≤ × ≤ 5 (see Note 2)	V_{CC} = 3 V/5 V,			±50	

NOTES: 1. The leakage current is measured with V_{SS} or V_{CC} applied to the corresponding pin(s), unless otherwise noted.
2. The leakage of the digital port pins is measured individually. The port pin must be selected for input and there must be no optional pullup or pulldown resistor.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

outputs P2x, TAx

PARAMETER		TEST CONDITIONS		VCC	MIN	NOM	MAX	UNIT
$f_{(P20)}$	Output frequency	P2.0/ACLK,	C_L = 20 pF	3 V/5 V			1.1	MHz
$f_{(TAx)}$	Output frequency	TA0, TA1, TA2,	C_L = 20 pF	3 V/5 V	dc		f_{System}	MHz
$t_{(Xdc)}$	Duty cycle of O/P frequency	P2.0/ACLK, C_L = 20 pF	f_{P20} = 1.1 MHz	3 V/ 5 V	40%		60%	
			$f_{P20} = f_{XTCLK}$		35%		65%	
			$f_{P20} = f_{XTCLK/n}$			50%		
$t_{(TAdc)}$		TA0, TA1, TA2, Duty cycle = 50%	C_L = 20 pF,	3 V/ 5 V		0	±50	ns

outputs Port 1 to P2; P1.0 to P1.7, P2.0 to P2.5

PARAMETER		TEST CONDITIONS			MIN	NOM	MAX	UNIT
V_{OH}	High-level output voltage	$I_{(OH)}$ = − 1.5 mA,	V_{CC} = 3 V/5 V,	See Note 1	V_{CC}−0.4		V_{CC}	V
		$I_{(OH)}$ = − 4.5 mA,	V_{CC} = 3 V/5 V,	See Note 2	V_{CC}-0.6		V_{CC}	
V_{OL}	Low-level output voltage	$I_{(OL)}$ = 1.5 mA,	V_{CC} = 3 V/5 V,	See Note 1	V_{SS}		V_{SS}+0.4	V
		$I_{(OL)}$ = 4.5 mA,	V_{CC} = 3 V/5 V,	See Note 2	V_{SS}		V_{SS}+0.6	

NOTES: 1. The maximum total current, I_{OH} and I_{OL}, or all outputs combined, should not exceed ±12 mA to hold the maximum voltage drop specified.
2. The maximum total current, I_{OH} and I_{OL}, or all outputs combined, should not exceed ±36 mA to hold the maximum voltage drop specified.

optional resistors, individually programmable with ROM code (see Note 1)

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
$R_{(opt1)}$	Resistors, individually programmable with ROM code, all port pins, values applicable for pulldown and pullup	V_{CC} = 3 V/5 V	2.1	4.1	6.2	kΩ
$R_{(opt2)}$		V_{CC} = 3 V/5 V	3.1	6.2	9.3	kΩ
$R_{(opt3)}$		V_{CC} = 3 V/5 V	6	12	18	kΩ
$R_{(opt4)}$		V_{CC} = 3 V/5 V	10	19	29	kΩ
$R_{(opt5)}$		V_{CC} = 3 V/5 V	19	37	56	kΩ
$R_{(opt6)}$		V_{CC} = 3 V/5 V	38	75	113	kΩ
$R_{(opt7)}$		V_{CC} = 3 V/5 V	56	112	168	kΩ
$R_{(opt8)}$		V_{CC} = 3 V/5 V	94	187	281	kΩ
$R_{(opt9)}$		V_{CC} = 3 V/5 V	131	261	392	kΩ
$R_{(opt10)}$		V_{CC} = 3 V/5 V	167	337	506	kΩ

NOTE 1: Optional resistors R_{optx} for pulldown or pullup are not programmed in standard OTP or EPROM devices MSP430P112 or PMS430E112.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

PUC/POR

PARAMETER		TEST CONDITIONS		MIN	NOM	MAX	UNIT
$t_{(POR\_Delay)}$	POR		V_{CC} = 3 V/5 V		150	250	µs
V_{POR}	POR	T_A = −40°C	V_{CC} = 3 V/5 V	1.5		2.4	V
		T_A = 25°C		1.2		2.1	V
		T_A = 85°C		0.9		1.8	V
$V_{(min)}$	POR		V_{CC} = 3 V/5 V	0		0.4	V
$t_{(reset)}$	PUC/POR	Reset is accepted internally	V_{CC} = 3 V/5 V	2			µs

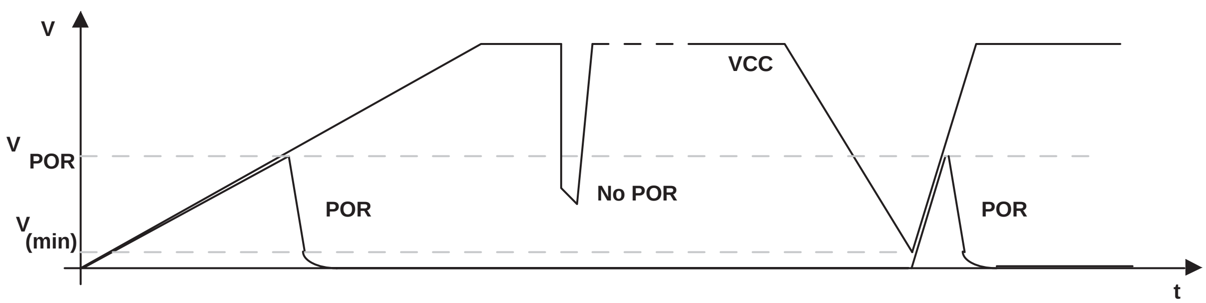


Figure 3. Power-On Reset (POR) vs Supply Voltage

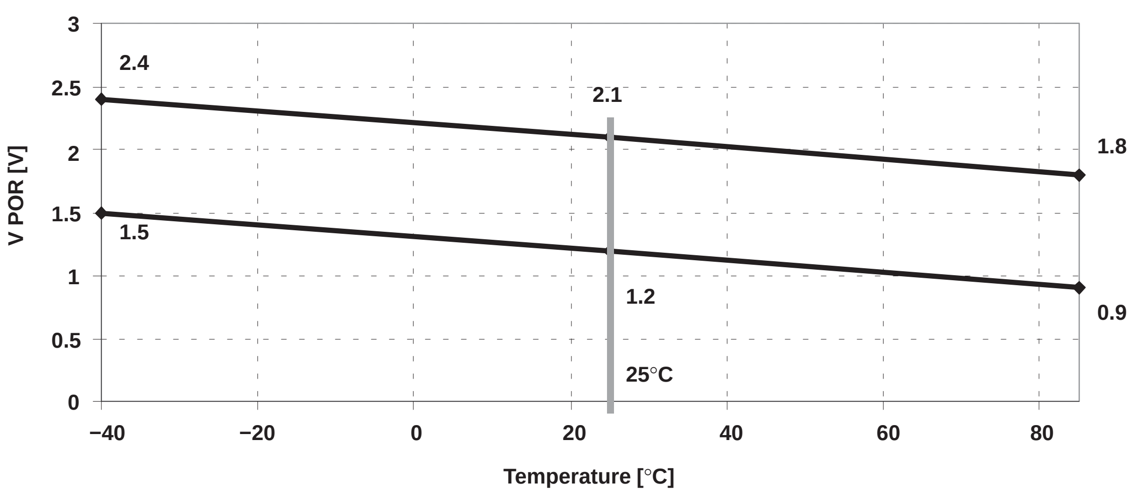


Figure 4. V_{POR} vs Temperature

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

wake-up from lower power modes (LPMx)

PARAMETER		TEST CONDITIONS		MIN	NOM	MAX	UNIT
$t_{(LPM0)}$/ $t_{(LPM2)}$	Delay time		V_{CC} = 3 V/5 V		100		ns
$t_{(LPM3)}$		R_{Sel} = 4, DCO = 3, MOD = 0	V_{CC} = 3 V/5 V		2.6	6	µs
$t_{(LPM4)}$		R_{Sel} = 4, DCO = 3, MOD = 0	V_{CC} = 3 V/5 V		2.8	6	µs

RAM

PARAMETER		MIN	NOM	MAX	UNIT
$V_{(RAMh)}$	CPU halted (see Note 1)	1.8			V

NOTE 1: This parameter defines the minimum supply voltage V_{CC} when the data in the program memory RAM remains unchanged. No program execution should happen during this supply voltage condition.

DCO (MSP430P112)

PARAMETER	TEST CONDITIONS		MIN	NOM	MAX	UNIT
$f_{(DCO03)}$	R_{sel} = 0, DCO = 3, MOD = 0, DCOR = 0, T_A = 25°C	V_{CC} = 3 V		0.12		MHz
		V_{CC} = 5 V		0.13		
$f_{(DCO13)}$	R_{sel} = 1, DCO = 3, MOD = 0, DCOR = 0, T_A = 25°C	V_{CC} = 3 V		0.19		MHz
		V_{CC} = 5 V		0.21		
$f_{(DCO23)}$	R_{sel} = 2, DCO = 3, MOD = 0, DCOR = 0, T_A = 25°C	V_{CC} = 3 V		0.31		MHz
		V_{CC} = 5 V		0.34		
$f_{(DCO33)}$	R_{sel} = 3, DCO = 3, MOD = 0, DCOR = 0, T_A = 25°C	V_{CC} = 3 V		0.5		MHz
		V_{CC} = 5 V		0.55		
$f_{(DCO43)}$	R_{sel} = 4, DCO = 3, MOD = 0, DCOR = 0, T_A = 25°C	V_{CC} = 3 V	0.5	0.8	1.1	MHz
		V_{CC} = 5 V	0.6	0.9	1.2	
$f_{(DCO53)}$	R_{sel} = 5, DCO = 3, MOD = 0, DCOR = 0, T_A = 25°C	V_{CC} = 3 V	0.9	1.2	1.55	MHz
		V_{CC} = 5 V	1.1	1.4	1.7	
$f_{(DCO63)}$	R_{sel} = 6, DCO = 3, MOD = 0, DCOR = 0, T_A = 25°C	V_{CC} = 3 V	1.7	2	2.3	MHz
		V_{CC} = 5 V	2.1	2.4	2.7	
$f_{(DCO73)}$	R_{sel} = 7, DCO = 3, MOD = 0, DCOR = 0, T_A = 25°C	V_{CC} = 3 V	2.8	3.1	3.5	MHz
		V_{CC} = 5 V	3.8	4.2	4.5	
$f_{(DCO47)}$	R_{sel} = 4, DCO = 7, MOD = 0, DCOR = 0, T_A = 25°C	V_{CC} = 3 V/5 V	F_{DCO40} x1.8	F_{DCO40} x2.2	F_{DCO40} x2.6	MHz
$S_{(Rsel)}$	$S_R = f_{Rsel+1}/f_{Rsel}$	V_{CC} = 3 V/5 V	1.4	1.65	1.9	ratio
$S_{(DCO)}$	$S_{DCO} = f_{DCO+1}/f_{DCO}$	V_{CC} = 3 V/5 V	1.07	1.12	1.16	
D_t	Temperature drift, R_{sel} = 4, DCO = 3, MOD = 0 (see Note 1)	V_{CC} = 3 V	−0.31	−0.36	−0.40	%/°C
		V_{CC} = 5 V	−0.33	−0.38	−0.43	
D_V	Drift with V_{CC} variation, R_{sel} = 4, DCO = 3, MOD = 0 (see Note 1)	V_{CC} = 3 V to 5 V	0	5	10	%/V

NOTE 1: These parameters are not production tested.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

DCO (MSP430C111, C112)

PARAMETER	TEST CONDITIONS		MIN	NOM	MAX	UNIT
$f_{(DCO03)}$	R_{sel} = 0, DCO = 3, MOD = 0, DCOR = 0, T_A = 25°C	V_{CC} = 3 V	0.04	0.07	0.10	MHz
		V_{CC} = 5 V	0.04	0.07	0.10	
$f_{(DCO13)}$	R_{sel} = 1, DCO = 3, MOD = 0, DCOR = 0, T_A = 25°C	V_{CC} = 3 V	0.08	0.13	0.18	MHz
		V_{CC} = 5 V	0.08	0.13	0.18	
$f_{(DCO23)}$	R_{sel} = 2, DCO = 3, MOD = 0, DCOR = 0, T_A = 25°C	V_{CC} = 3 V	0.15	0.22	0.30	MHz
		V_{CC} = 5 V	0.15	0.22	0.30	
$f_{(DCO33)}$	R_{sel} = 3, DCO = 3, MOD = 0, DCOR = 0, T_A = 25°C	V_{CC} = 3 V	0.26	0.36	0.47	MHz
		V_{CC} = 5 V	0.26	0.36	0.47	
$f_{(DCO43)}$	R_{sel} = 4, DCO = 3, MOD = 0, DCOR = 0, T_A = 25°C	V_{CC} = 3 V	0.4	0.6	0.8	MHz
		V_{CC} = 5 V	0.4	0.6	0.8	
$f_{(DCO53)}$	R_{sel} = 5, DCO = 3, MOD = 0, DCOR = 0, T_A = 25°C	V_{CC} = 3 V	0.8	1.1	1.4	MHz
		V_{CC} = 5 V	0.8	1.1	1.4	
$f_{(DCO63)}$	R_{sel} = 6, DCO = 3, MOD = 0, DCOR = 0, T_A = 25°C	V_{CC} = 3 V	1.3	1.7	2.1	MHz
		V_{CC} = 5 V	1.5	1.9	2.3	
$f_{(DCO73)}$	R_{sel} = 7, DCO = 3, MOD = 0, DCOR = 0, T_A = 25°C	V_{CC} = 3 V	2.4	2.9	3.4	MHz
		V_{CC} = 5 V	3.1	3.8	4.5	
$f_{(DCO47)}$	R_{sel} = 4, DCO = 7, MOD = 0, DCOR = 0, T_A = 25°C	V_{CC} = 3 V/5 V	F_{DCO40} x1.8	F_{DCO40} x2.2	F_{DCO40} x2.6	MHz
$S_{(Rsel)}$	$S_R = f_{Rsel+1}/f_{Rsel}$	V_{CC} = 3 V/5 V	1.4	1.65	1.9	ratio
$S_{(DCO)}$	$S_{DCO} = f_{DCO+1}/f_{DCO}$	V_{CC} = 3 V/5 V	1.07	1.12	1.16	
D_t	Temperature drift, R_{sel} = 4, DCO = 3, MOD = 0 (see Note 1)	V_{CC} = 3 V	−0.31	−0.36	−0.40	%/°C
		V_{CC} = 5 V	−0.33	−0.38	−0.43	
D_V	Drift with V_{CC} variation, R_{sel} = 4, DCO = 3, MOD = 0 (see Note 1)	V_{CC} = 3 V to 5 V	0	5	10	%/V

NOTE 1: These parameters are not production tested.

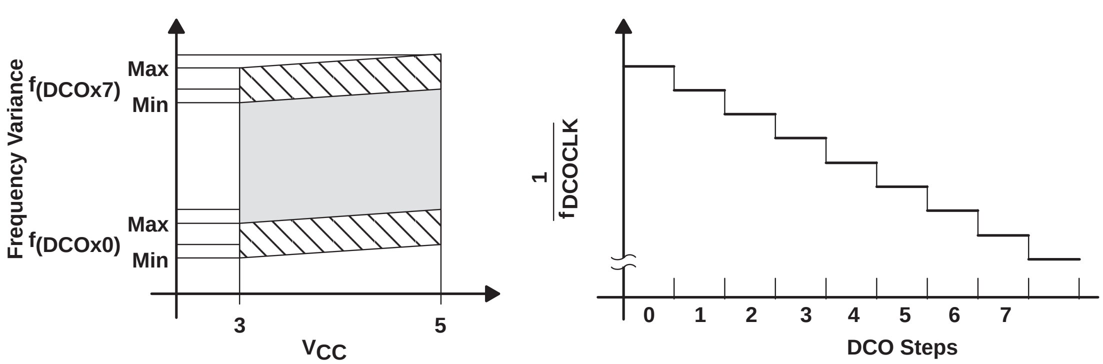


Figure 5. DCO Characteristics

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

main DCO characteristics

- Individual devices have a minimum and maximum operation frequency. The specified parameters for $f_{(DCOx0)}$ to $f_{(DCOx7)}$ are valid for all devices.
- All ranges selected by Rsel(n) overlap with Rsel(n+1): Rsel0 overlaps Rsel1, ... Rsel6 overlaps Rsel7.
- DCO control bits DCO0, DCO1, and DCO2 have a step size as defined by parameter S_{DCO}.
- Modulation control bits MOD0 to MOD4 select how often $f_{(DCO+1)}$ is used within the period of 32 DCOCLK cycles. The frequency $f_{(DCO)}$ is used for the remaining cycles. The frequency is an average equal to:

$$f_{average} = \frac{32 \times f_{(DCO)} \times f_{(DCO+1)}}{MOD \times f_{(DCO)} + (32 - MOD) \times f_{(DCO+1)}}$$

crystal oscillator, XIN, XOUT

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
C_{XIN}	Capacitance at input	V_{CC} = 3 V/5 V		12		pF
C_{XOUT}	Capacitance at output	V_{CC} = 3 V/5 V		12		pF
V_{IL}	Input levels at XIN	V_{CC} = 3 V/5 V (see Note 2)	V_{SS}		$0.2 \times V_{CC}$	V
V_{IH}			$0.8 \times V_{CC}$		V_{CC}	

NOTES: 1. The oscillator needs capacitors at both terminals, with values specified by the crystal manufacturer.
2. Applies only when using an external logic-level clock source. Not applicable when using a crystal or resonator.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

EPROM Memory, P- and E- versions only (see Note 1)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	NOM	MAX	UNIT
$V_{(PP)}$	Programming voltage, applied to TEST/VPP			12	12.5	13	V
$I_{(PP)}$	Current from programming voltage source					70	mA
$t_{(pps)}$	Programming time, single pulse			5			ms
$t_{(ppf)}$	Programming time, fast algorithm				100		µs
$P_{(n)}$	Number of pulses for successful programming			4		100	Pulse
$t_{(erase)}$	Erase time: Wave length 2537 Å at 15 Ws/cm^2 (UV lamp of 12 mW/ cm^2)			30			min
	Write/erase cycles			1000			cycles
	Data retention Tj < 55°C			10			Year

NOTES: 1. Refer to the Recommended Operating Conditions for the correct V_{CC} during programming.

JTAG Interface

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	NOM	MAX	UNIT
f_{TCK}	TCK input frequency	see Note 1	3 V	DC		5	MHz
			5 V	DC		10	

NOTES: 1. f_{TCK} may be restricted to meet the timing requirements of the module selected.

JTAG Fuse (see Note 1)

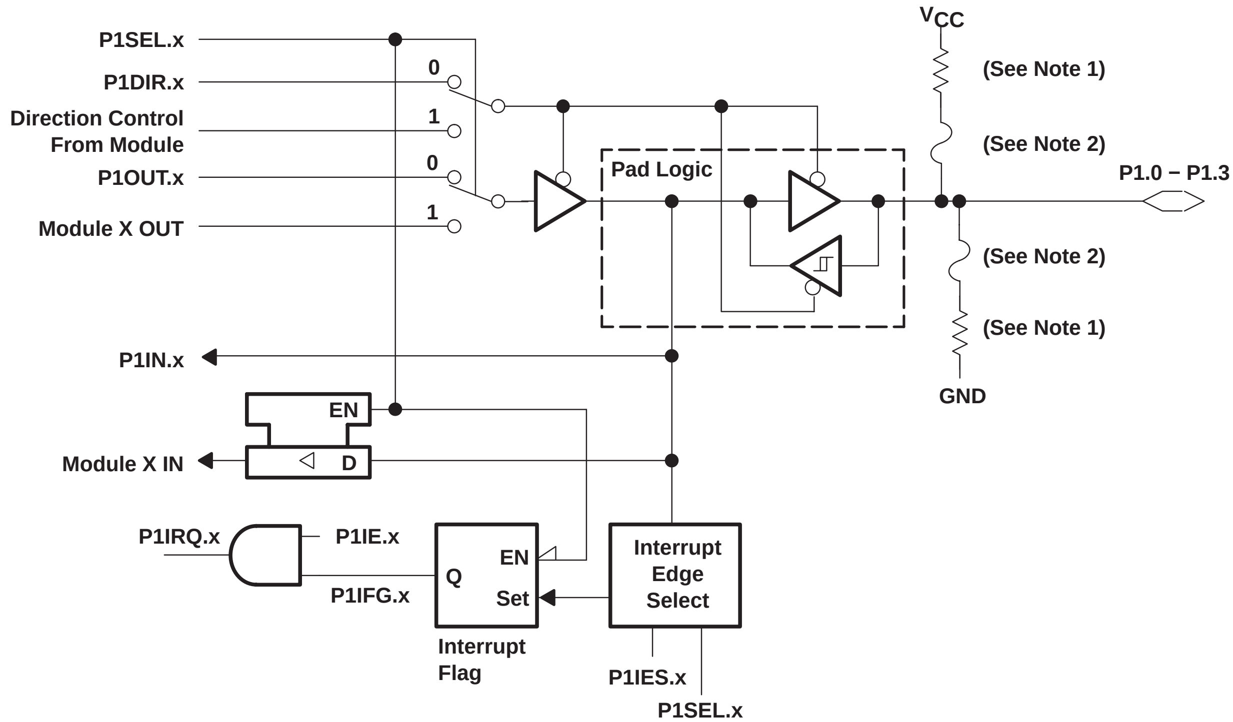
PARAMETER		TEST CONDITIONS	V_{CC}	MIN	NOM	MAX	UNIT
V_{FB}	Fuse blow voltage, C versions (see Note 2)		3 V/ 5 V	5.5		6	V
	Fuse blow voltage, E/P versions (see Note 2)		3 V/ 5 V	11		13	
I_{FB}	Supply current into TEST/VPP during fuse blow					100	mA
t_{FB}	Time to blow fuse					1	ms

NOTES: 1. Once the fuse is blown, no further access to the MSP430 JTAG/Test and emulation features is possible. The JTAG block is switched to bypass mode.
2. The fuse blow voltage is applied to the TEST/VPP pin.

APPLICATION INFORMATION

input/output schematic

Port P1, P1.0 to P1.3, input/output with Schmitt-trigger

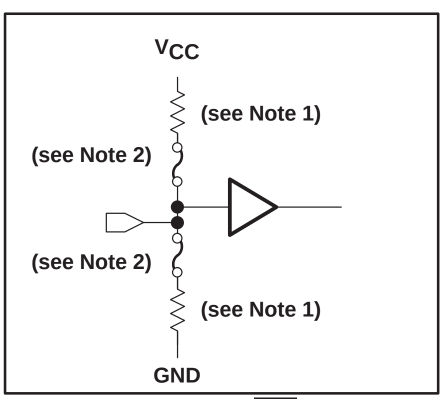


NOTE: x = Bit Identifier, 0 to 3 For Port P1

PnSel.x	PnDIR.x	Dir. Control from module	PnOUT.x	Module X OUT	PnIN.x	Module X IN	PnIE.x	PnIFG.x	PnIES.x
P1Sel.0	P1DIR.0	P1DIR.0	P1OUT.0	V_{SS}	P1IN.0	TACLK†	P1IE.0	P1IFG.0	P1IES.0
P1Sel.1	P1DIR.1	P1DIR.1	P1OUT.1	Out0 signal†	P1IN.1	CCI0A†	P1IE.1	P1IFG.1	P1IES.1
P1Sel.2	P1DIR.2	P1DIR.2	P1OUT.2	Out1 signal†	P1IN.2	CCI1A†	P1IE.2	P1IFG.2	P1IES.2
P1Sel.3	P1DIR.3	P1DIR.3	P1OUT.3	Out2 signal†	P1IN.3	CCI2A†	P1IE.3	P1IFG.3	P1IES.3

† Signal from or to Timer_A

NOTES: 1. Optional selection of pullup or pulldown resistors with ROM (masked) versions.
2. Fuses for optional pullup and pulldown resistors can only be programmed at the factory.

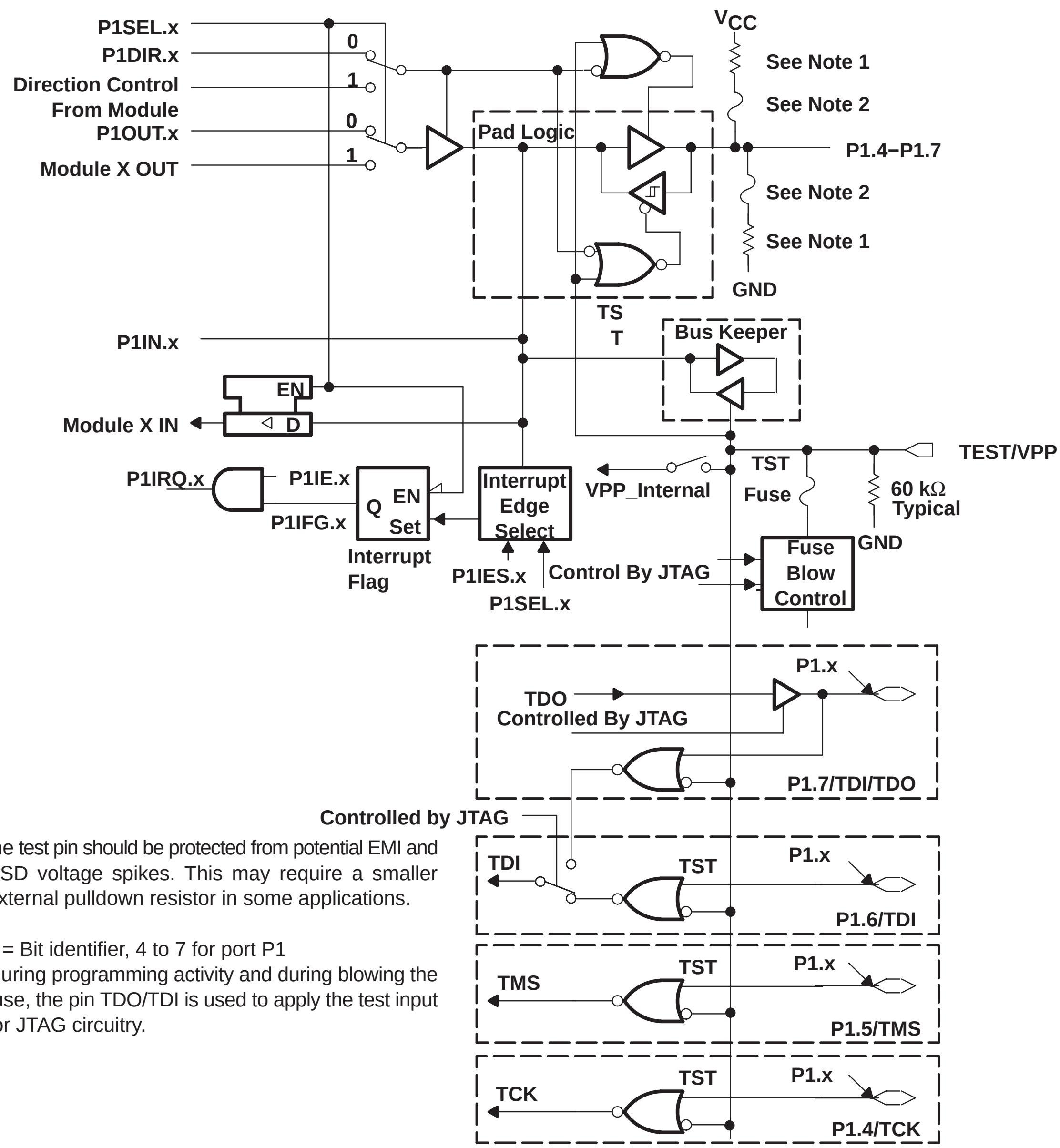


CMOS INPUT ($\overline{RST}$/NMI)

APPLICATION INFORMATION

input/output schematic (continued)

Port P1, P1.4 to P1.7, input/output with Schmitt-trigger and in-system access features



NOTES: The test pin should be protected from potential EMI and ESD voltage spikes. This may require a smaller external pulldown resistor in some applications.

x = Bit identifier, 4 to 7 for port P1

During programming activity and during blowing the fuse, the pin TDO/TDI is used to apply the test input for JTAG circuitry.

PnSel.x	PnDIR.x	Dir. Control from module	PnOUT.x	Module X OUT	PnIN.x	Module X IN	PnIE.x	PnIFG.x	PnIES.x
P1Sel.4	P1DIR.4	P1DIR.4	P1OUT.4	SMCLK	P1IN.4	unused	P1IE.4	P1IFG.4	P1IES.4
P1Sel.5	P1DIR.5	P1DIR.5	P1OUT.5	Out0 signal†	P1IN.5	unused	P1IE.5	P1IFG.5	P1IES.5
P1Sel.6	P1DIR.6	P1DIR.6	P1OUT.6	Out1 signal†	P1IN.6	unused	P1IE.6	P1IFG.6	P1IES.6
P1Sel.7	P1DIR.7	P1DIR.7	P1OUT.7	Out2 signal†	P1IN.7	unused	P1IE.7	P1IFG.7	P1IES.7

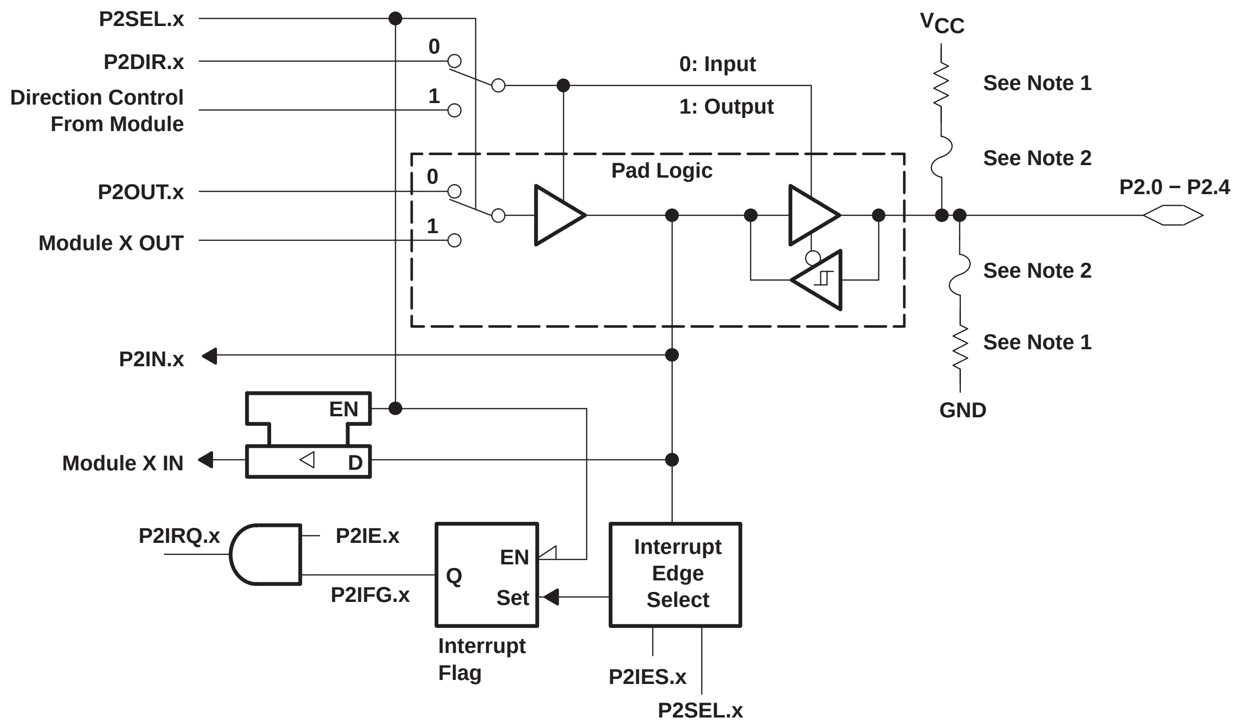
† Signal from or to Timer_A

NOTES: 1. Optional selection of pullup or pulldown resistors with ROM (masked) versions.
2. Fuses for optional pullup and pulldown resistors can only be programmed at the factory.

APPLICATION INFORMATION

input/output schematic (continued)

Port P2, P2.0 to P2.4, input/output with Schmitt-trigger



NOTE: x = Bit Identifier, 0 to 4 For Port P2

PnSel.x	PnDIR.x	Dir. Control from module	PnOUT.x	Module X OUT	PnIN.x	Module X IN	PnIE.x	PnIFG.x	PnIES.x
P2Sel.0	P2DIR.0	P2DIR.0	P2OUT.0	ACLK	P2IN.0	unused	P2IE.0	P2IFG.0	P1IES.0
P2Sel.1	P2DIR.1	P2DIR.1	P2OUT.1	V_{SS}	P2IN.1	INCLK†	P2IE.1	P2IFG.1	P1IES.1
P2Sel.2	P2DIR.2	P2DIR.2	P2OUT.2	Out0 signal†	P2IN.2	CCI0B†	P2IE.2	P2IFG.2	P1IES.2
P2Sel.3	P2DIR.3	P2DIR.3	P2OUT.3	Out1 signal†	P2IN.3	CCI1B†	P2IE.3	P2IFG.3	P1IES.3
P2Sel.4	P2DIR.4	P2DIR.4	P2OUT.4	Out2 signal†	P2IN.4	unused	P2IE.4	P2IFG.4	P1IES.4

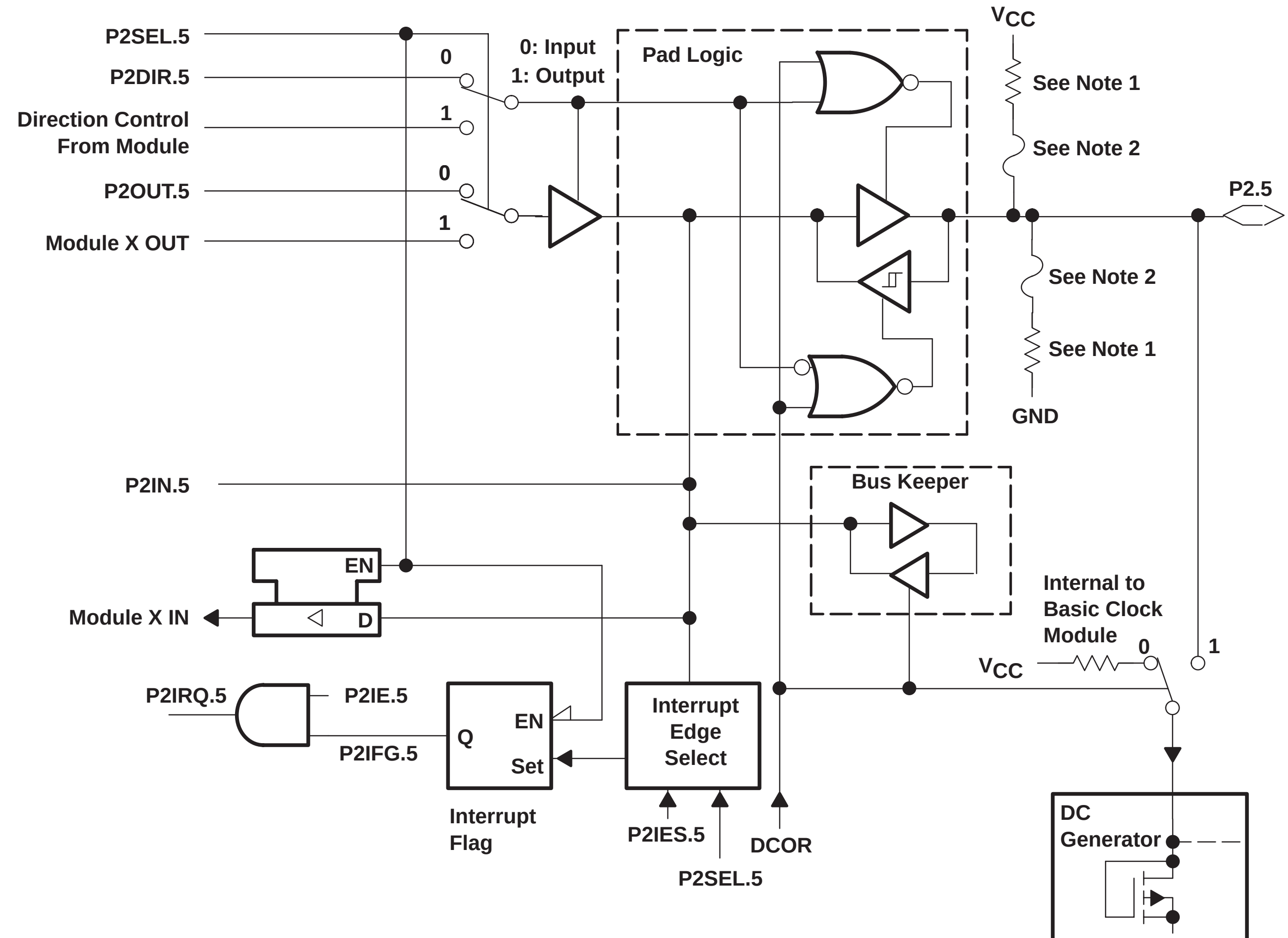
† Signal from or to Timer_A

NOTES: 1. Optional selection of pullup or pulldown resistors with ROM (masked) versions.
2. Fuses for optional pullup and pulldown resistors can only be programmed at the factory.

APPLICATION INFORMATION

input/output schematic (continued)

Port P2, P2.5, input/output with Schmitt-trigger and R_{OSC} function for the Basic Clock module



NOTE: DCOR: Control bit from basic clock module if it is set, P2.5 is disconnected from P2.5 pad

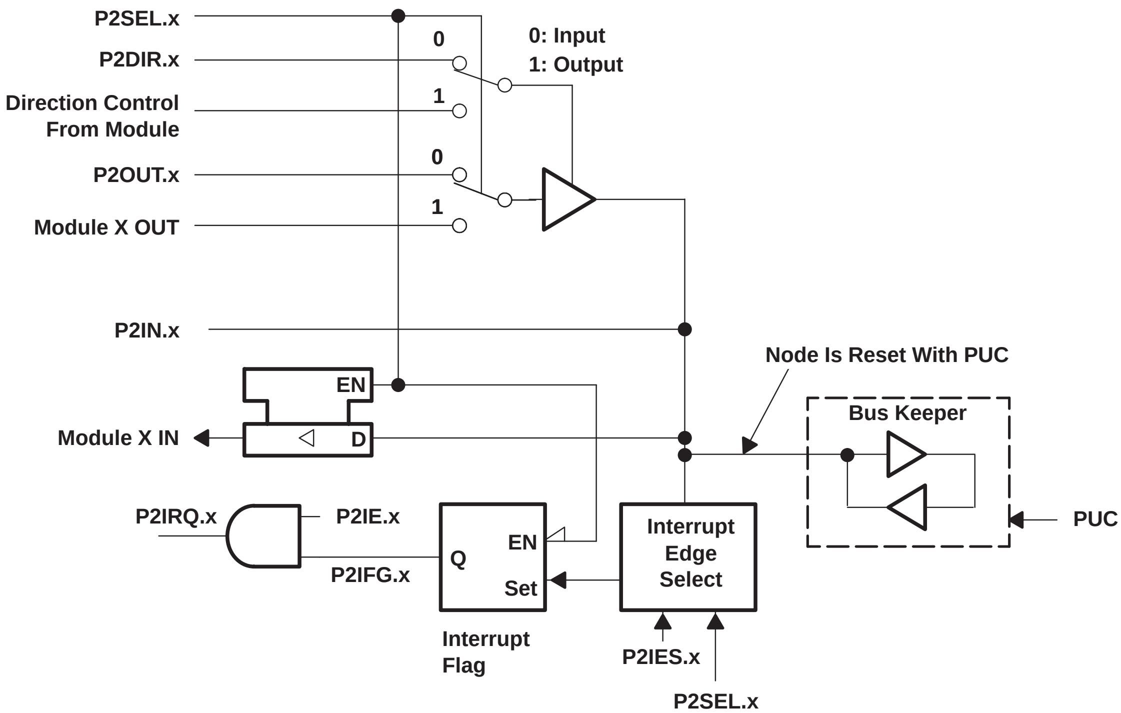
PnSel.x	PnDIR.x	Director Control from module	PnOUT.x	Module X OUT	PnIN.x	Module X IN	PnIE.x	PnIFG.x	PnIES.x
P2Sel.5	P2DIR.5	P2DIR.5	P2OUT.5	V_{SS}	P2IN.5	unused	P2IE.5	P2IFG.5	P2IES.5

NOTES: 1. Optional selection of pullup or pulldown resistors with ROM (masked) versions.
2. Fuses for optional pullup and pulldown resistors can only be programmed at the factory.

APPLICATION INFORMATION

input/output schematic (continued)

Port P2, un-bonded bits P2.6 and P2.7



NOTE: x = Bit identifier, 6 to 7 for Port P2 without external pins

P2Sel.x	P2DIR.x	Dir. Control from module	P2OUT.x	Module X OUT	P2IN.x	Module X IN	P2IE.x	P2IFG.x	P2IES.x
P2Sel.6	P2DIR.6	P2DIR.6	P2OUT.6	V_{SS}	P2IN.6	unused	P2IE.6	P2IFG.6	P2IES.6
P2Sel.7	P2DIR.7	P2DIR.7	P2OUT.7	V_{SS}	P2IN.7	unused	P2IE.7	P2IFG.7	P2IES.7

NOTE: A good use of the unbonded bits 6 and 7 of port P2 is to use the interrupt flags. The interrupt flags can not be influenced from any signal other than from software. They work then as soft interrupt.

APPLICATION INFORMATION

JTAG fuse check mode

MSP430 devices that have the fuse on the TEST terminal have a fuse check mode that tests the continuity of the fuse the first time the JTAG port is accessed after a power-on reset (POR). When activated, a fuse check current, I_{TF}, of 1 mA at 3 V, 2.5 mA at 5 V can flow from the TEST pin to ground if the fuse is not burned. Care must be taken to avoid accidentally activating the fuse check mode and increasing overall system power consumption.

When the TEST pin is taken back low after a test or programming session, the fuse check mode and sense currents are terminated.

Activation of the fuse check mode occurs with the first negative edge on the TMS pin after power up or if TMS is being held low during power up. The second positive edge on the TMS pin deactivates the fuse check mode. After deactivation, the fuse check mode remains inactive until another POR occurs. After each POR the fuse check mode has the potential to be activated.

The fuse check current will only flow when the fuse check mode is active and the TMS pin is in a low state (see Figure 6). Therefore, the additional current flow can be prevented by holding the TMS pin high (default condition).

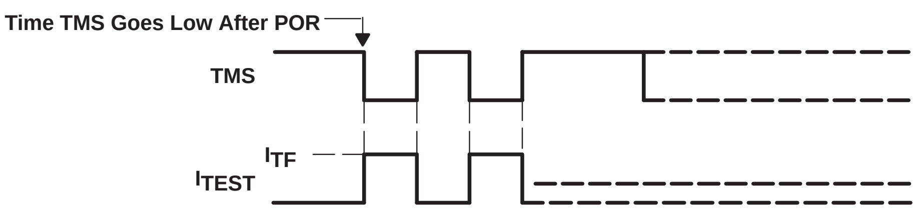
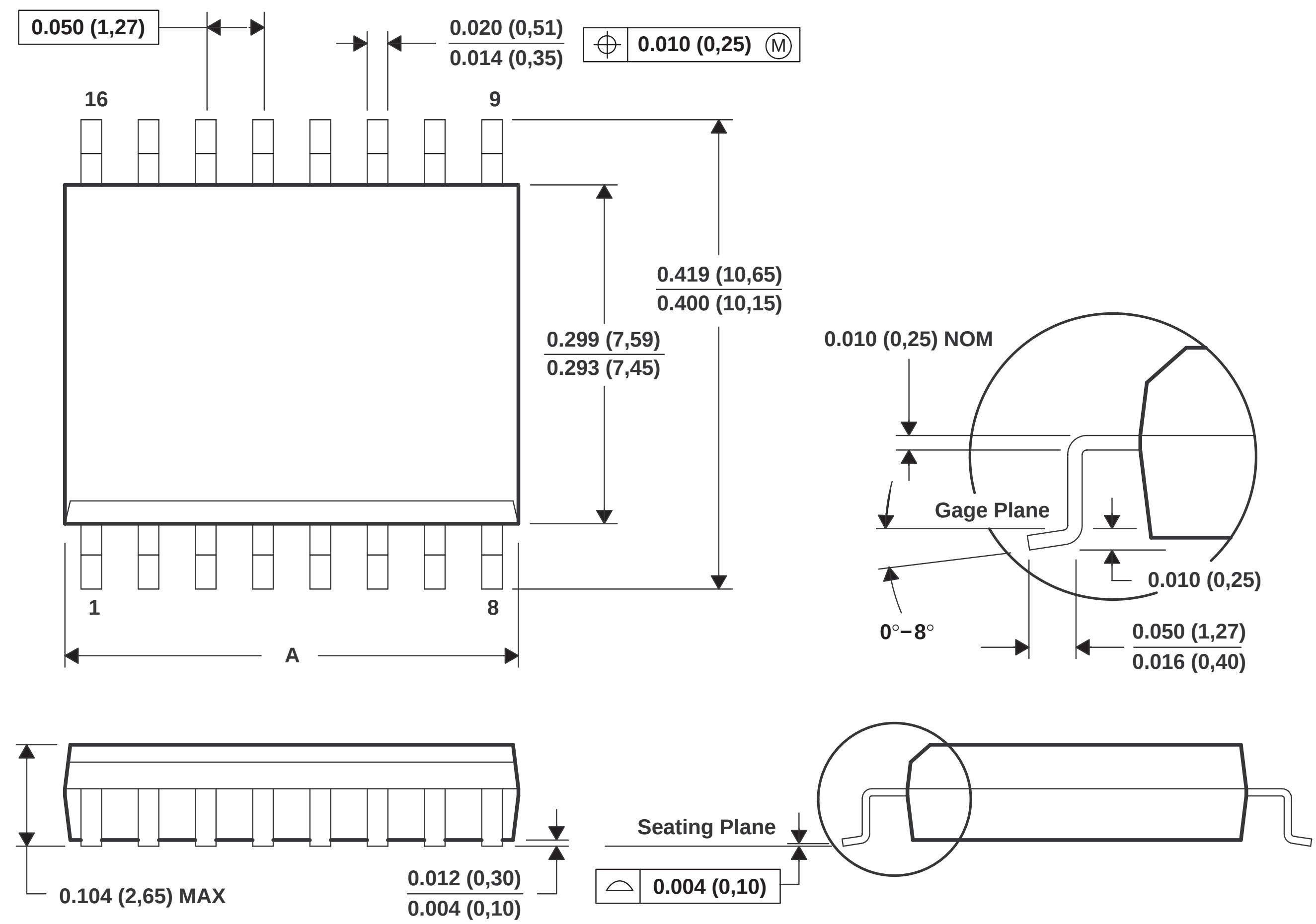


Figure 6. Fuse Check Mode Current, MSP430x11x

MECHANICAL DATA

DW (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

16 PIN SHOWN

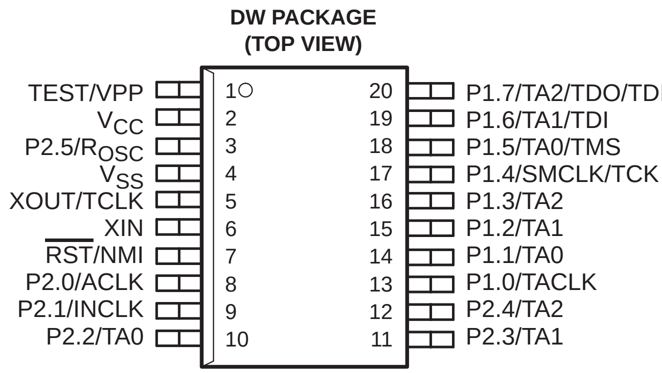


PINS ** / DIM	16	20	24
A MAX	0.410 (10,41)	0.510 (12,95)	0.610 (15,49)
A MIN	0.400 (10,16)	0.500 (12,70)	0.600 (15,24)

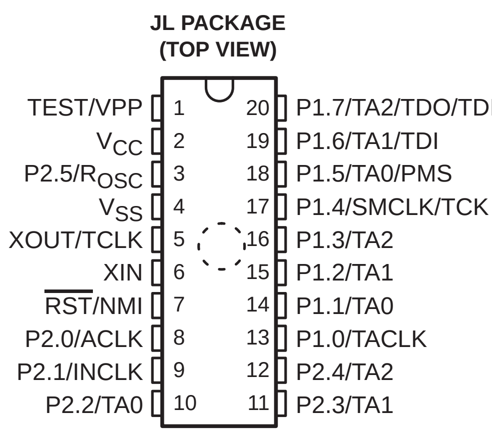
4040000/D 02/98

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS-013

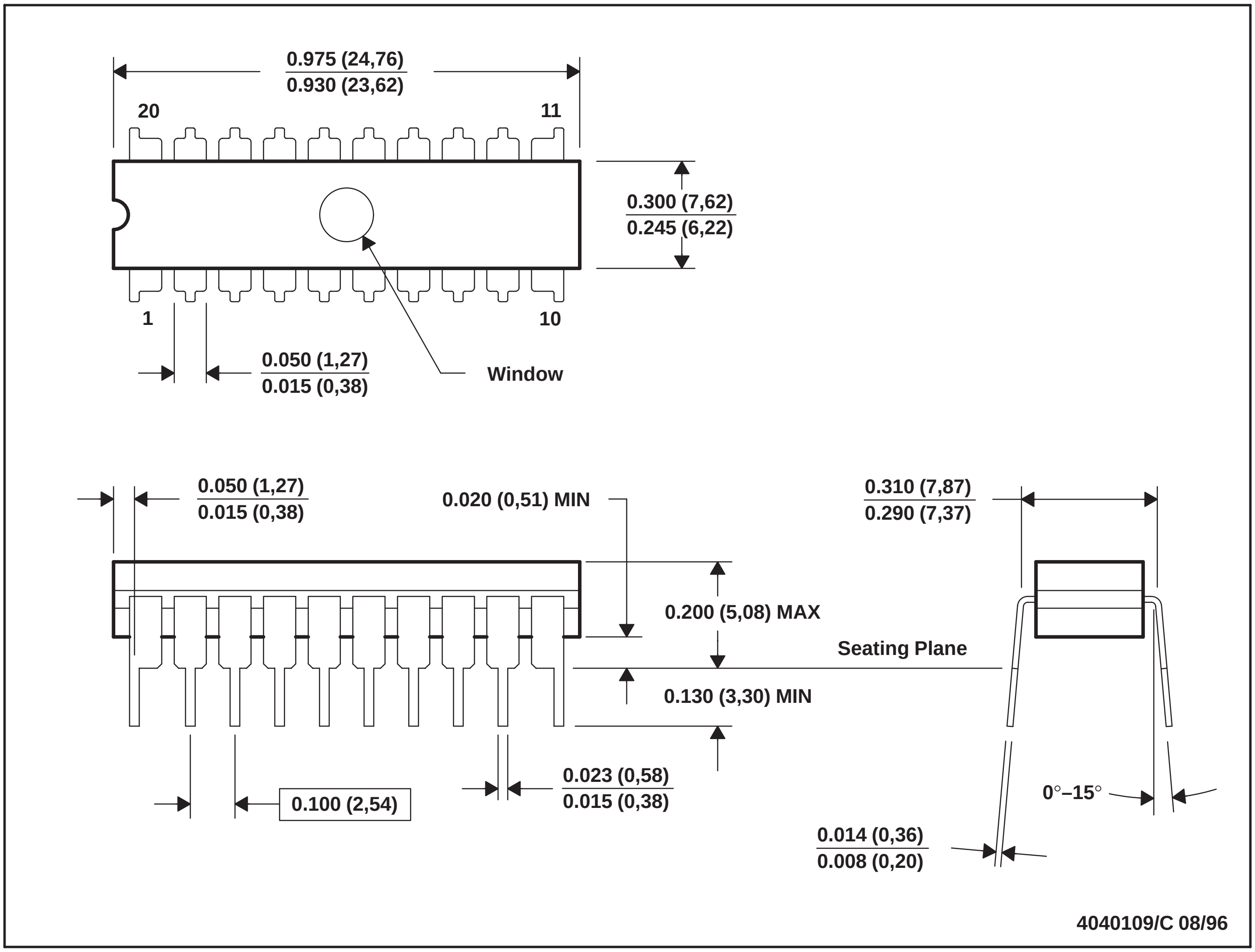
MSP430C111IDW, MSP430C112IDW, MSP430P112IDW pin out



PMS430E112 pin out

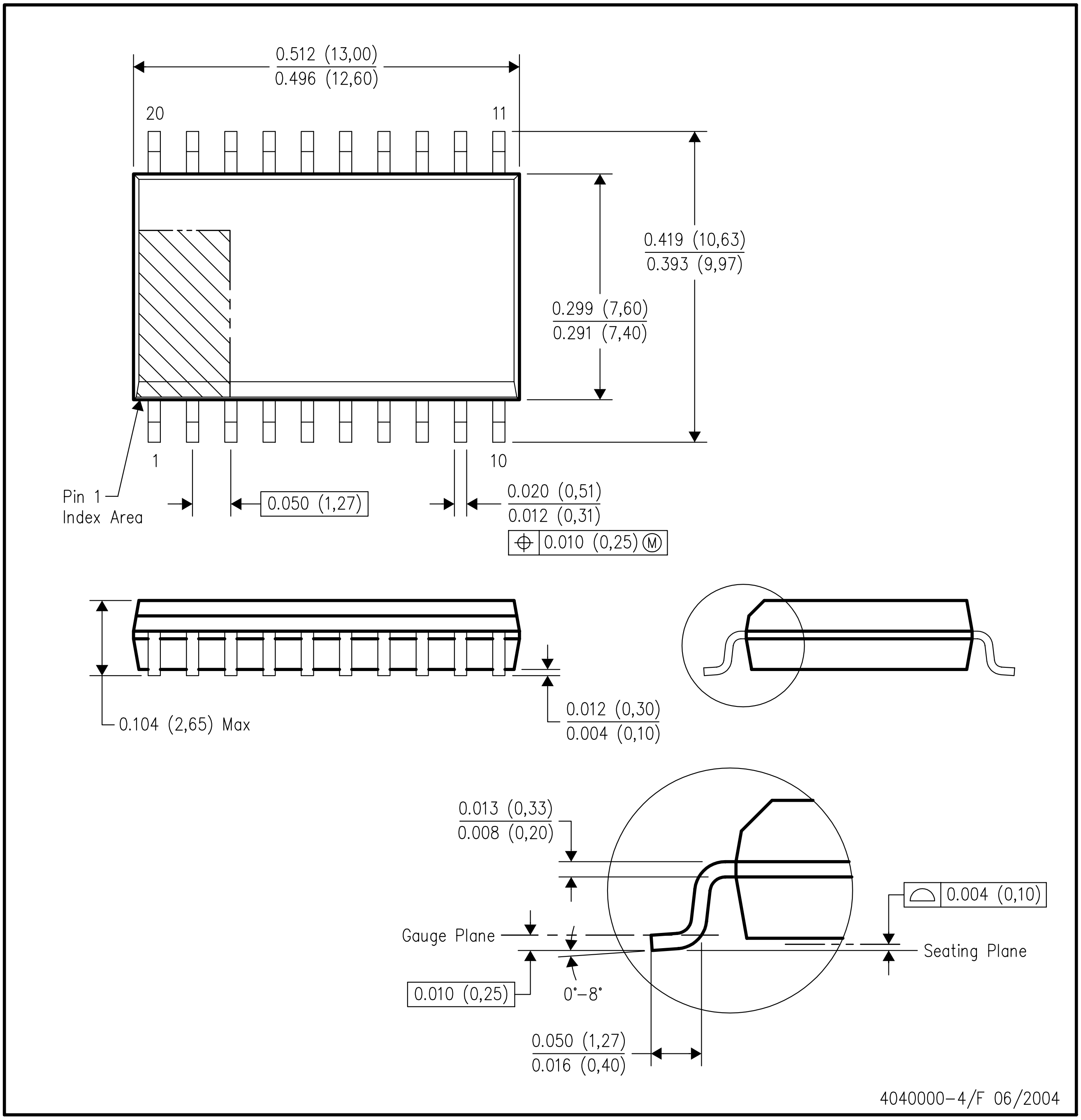


JL (R-GDIP-T20) **CERAMIC DUAL-IN-LINE PACKAGE**



NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only
- E. Falls within MIL-STD-1835 GDIP1-T20

DW (R-PDSO-G20) PLASTIC SMALL-OUTLINE PACKAGE



NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
- D. Falls within JEDEC MS-013 variation AC.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products		**Applications**	
Amplifiers	amplifier.ti.com	Audio	www.ti.com/audio
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Logic	logic.ti.com	Military	www.ti.com/military
Power Mgmt	power.ti.com	Optical Networking	www.ti.com/opticalnetwork
Microcontrollers	microcontroller.ti.com	Security	www.ti.com/security
		Telephony	www.ti.com/telephony
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