MSP430F43x/43x1/44x Device Erratasheet

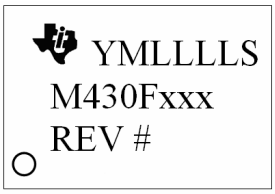
Current Version

Devices	Rev:	ADC9	ADC10	ADC13	ADC18	CPU4	FLL3	PORT3	TA12	TA16	TB2	TB14	TB15	TB16	US13	US15	WDG2
MSP430F4351IPN	I					✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
MSP430F4351IPZ	H					✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
MSP430F435IPN	I	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
MSP430F435IPZ	H	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
MSP430F4361IPN	I					✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
MSP430F4361IPZ	H					✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
MSP430F436IPN	I	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
MSP430F436IPZ	H	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
MSP430F4371IPN	I					✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
MSP430F4371IPZ	H					✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
MSP430F437IPN	I	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
MSP430F437IPZ	H	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
MSP430F447	G	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓		✓	✓	✓	✓
MSP430F448	G	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓		✓	✓	✓	✓
MSP430F449	G	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓		✓	✓	✓	✓

Note: See Appendix for prior revisions

Package Markings

PN80: LQFP(PN) 80-pin



YM = Year and Month Date Code
LLLL = LOT Trace Code
S = Assembly Site Code
# = DIE Revision
o = PIN 1

PZ100: LQFP(PZ) 100-pin

YM = Year and Month Date Code
LLLL = LOT Trace Code
S = Assembly Site Code
# = DIE Revision
o = PIN 1

Detailed Bug Description

ADC9 ADC9 - Bug description:

Module: ADC12, Function: Interrupt vector register

If the ADC12 uses a different clock than the CPU (MCLK) and more than one ADC interrupt is enabled, the ADC12IV register content may be unpredictable for one clock cycle. This will happen, if during the execution of an ADC interrupt another ADC interrupt with higher priority occurs.

Workaround:
- read out ADC12IV twice and use only when values are equal
- use ADC12IFG to determine which interrupt has occurred

ADC10 ADC10 - Bug description:

Module: ADC12: Function: Unintended start of conversion

Accessing ADC12OVIE or ADC12TOVIE at the end of an ADC12 conversion with BIS/BIC commands can cause the ADC12SC bit to be set again right after it was cleared. This might start another conversion if ADC12SC is configured to trigger the ADC (SHS = 0).

Workaround:
If ADC12SC is configured to trigger the ADC, the control bits ADC12OVIE and ADC12TOVIE should only be modified when the ADC is not busy (ADC12BUSY = 0).

ADC13 ADC13 - Bug description:

Module: ADC12, Function: Current consumption after clearing ADC12ON while ADC is busy

If the ADC12ON bit is cleared while the ADC is busy, the ADC core might not be completely turned off and still consume current.

Workaround:
Wait until ADC12BUSY is reset before clearing the ADC12ON bit. This is recommended for all protected bits in the ADC12CTLx registers. Or: Clear CONSEQx bits. With CONSEQx=0 and ENC=0 the ADC12 is reset.

Detailed Bug Description (continued)

ADC18 ADC18 - Bug description:

Module: ADC12, incorrect conversion result in extended sample mode

The ADC12 conversion result can be incorrect in case where the extended sample mode is selected (SHP=0), the conversion clock is not the internal ADC12 oscillator (ADC12SSEL>0), and one of the following two conditions is true:

1.) The extended sample input signal SHI is asynchronous to the clock source used for ADC12CLK and the undivided ADC12 input clock frequency exceeds 3.15MHz
Or
2.) The extended sample input signal SHI is synchronous to the clock source used for ADC12CLK and the undivided ADC12 input clock frequency exceeds 6.3MHz.

Workaround:
1.) Use the pulse sample mode (SHP=1)
Or
2.) Use the ADC12 internal oscillator as the ADC12 clock source
Or
3.) Limit the undivided ADC12 input clock frequency to 3.15MHz
Or
4.) Use the same clock source (such as ACLK or SMCLK) to derive both SHI and ADC12CLK in order to achieve synchronous operation, and also limit the undivided ADC12 input clock frequency to 6.3MHz

CPU4 CPU4 - Bug description:

Module: CPU, Function: PUSH #4, PUSH #8

The single operand instruction PUSH cannot use the internal constants (CG) 4 and 8. The other internal constants (0, 1, 2, -1) can be used. The Assembler version 1.08 and higher produces correct code. The number of clock cycles is different:
PUSH #CG uses address mode 00, requiring 3 cycles, 1 word instruction
PUSH #4/#8 uses address mode 11, requiring 5 cycles, 2 word instruction

Workaround implemented in assembler.
No fix planned.

FLL3 FLL3 – Bug description:

Module: FLL+, Function: FLLDx = 11 for /8 may generate an unstable MCLK frequency

When setting the FLL to higher frequencies using FLLDx = 11 (/8) the output frequency of the FLL may have a larger frequency variation (e.g. averaged over 2sec) as well as a lower average output frequency than expected when compared to the other FLLDx bit settings.

Workaround:
None

Detailed Bug Description (continued)

PORT3 Port3 - Bug description:

Module: PORT1/2, Function: Port interrupts can get lost

Port interrupts can get lost if they occur during CPU access of the P1IFG and P2IFG registers.

Workaround:
None

TA12 TA12 - Bug description:

Module: TimerA, Function: Interrupt is lost (slow ACLK)

TimerA counter is running with slow clock (external TACLK or ACLK) compared to MCLK. The compare mode is selected for the capture/compare channel and the CCRx register is incremented by 1 with the occurring compare interrupt (if TAR = CCRx).
Due to the fast MCLK the CCRx register increment (CCRx = CCRx+1) happens before the TimerA counter has incremented again. Therefore the next compare interrupt should happen at once with the next TimerA counter increment (if TAR = CCRx + 1). This interrupt gets lost.

Workaround:
Switch capture/compare mode to capture mode before the CCRx register increment. Switch back to compare mode afterwards.

TA16 TA16 - Bug description:

Module: TimerA, Function: First increment of TAR erroneous when IDx > 00

The first increment of TAR after any timer clear event (POR/TACLR) happens immediately following the first positive edge of the selected clock source (INCLK, SMCLK, ACLK or TACLK). This is independent of the clock input divider settings (ID0, ID1). All following TAR increments are performed correctly with the selected IDx settings.

Workaround:
None

Detailed Bug Description (continued)

TB2 TB2 - Bug description:

Module: TimerB, Interrupt is lost (slow ACLK)

TimerB counter is running with slow clock (external TBCLK or ACLK) compared to MCLK. The compare mode is selected for the capture/compare channel and the CCRx register is incremented by 1 with the occurring compare interrupt (if TBR = CCRx).
Due to the fast MCLK the CCRx register increment (CCRx = CCRx+1) happens before the TimerB counter has incremented again. Therefore the next compare interrupt should happen at once with the next TimerB counter increment (if TBR = CCRx + 1). This interrupt gets lost.

Workaround:
Switch capture/compare mode to capture mode before the CCRx register increment. Switch back to compare mode afterwards.

TB14 TB14 - Bug description:

Module: TimerB, PWM output

The PWM output unit may behave erroneously if the condition for changing the PWM output (EQUx or EQU0) and the condition for loading the shadow register TBCLx happens at the same time. Depending on the load condition for the shadow registers (CLLD bits in TBCCTLx) there are four different possible error conditions:

1. Change CCRx register from any value to CCRx=0
   (e.g. sequence for CCRx = 4 3 2 0 0 0)
2. Change CCRx register from CCRx=0 to any value
   (e.g. sequence for CCRx = 0 0 0 2 3 4)
3. Change CCRx register from any value to current SHD0 (CCR0) value
   (e.g. sequence for CCRx = 4 2 5 SHD0 3 8)
4. Change CCRx register from current SHD0 (CCR0) value to any value
   (e.g. sequence for CCRx = 4 2 SHD0 5 3 8)

SW workaround:
No general workaround available.

TB15 TB15 - Bug description:

Module: TimerB3, 'Grouping Compare Latch' modes with TBCLx=2 or 3 are not useable

For TimerB3, 'Grouping Compare Latch' modes with control bits TBCLx=10 or 11 (Bits 14, 13 in TBCTL register) are not useable.
If one of these settings are used, no load of any Compare Latch TBCLx will happen.

Workaround:
None (Use only TBCLx = 00 or 01 for reliable module operation.)

Detailed Bug Description (continued)

TB16 TB16 - Bug description:

Module: TimerB, Function: First increment of TBR erroneous when IDx > 00

The first increment of TBR after any timer clear event (POR/TBCLR) happens immediately following the first positive edge of the selected clock source (INCLK, SMCLK, ACLK or TBCLK). This is independent of the clock input divider settings (ID0, ID1). All following TBR increments are performed correctly with the selected IDx settings.

Workaround:
None

US13 US13 - Bug description:

Module: USART0, USART1, Function: Unpredictable program execution

USART interrupts requested by URXS can result in unpredictable program execution if this request is not served within two bit times of the received data.

Workaround:
Ensure that the interrupt service routine is entered within two bit times of the received data.

US15 US15 - Bug description:

Module: USART0, USART1, Function: UART receive with two stop bits

USART hardware does not detect a missing second stop bit when SPB = 1. The Framing Error Flag (FE) will not be set under this condition and erroneous data reception may occur.

Workaround:
None (Configure USART for a single stop bit, SPB = 0)

WDG2 WDG2 - Bug description:

If a key violation is caused by incorrectly accessing a flash control register, the watchdog interrupt flag is set in addition to a correctly generated PUC.

Workaround:
None

Appendix: Prior Versions

None

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Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265