MOSEL VITELIC

MSS1506

DECEMBER

VOICE ROM

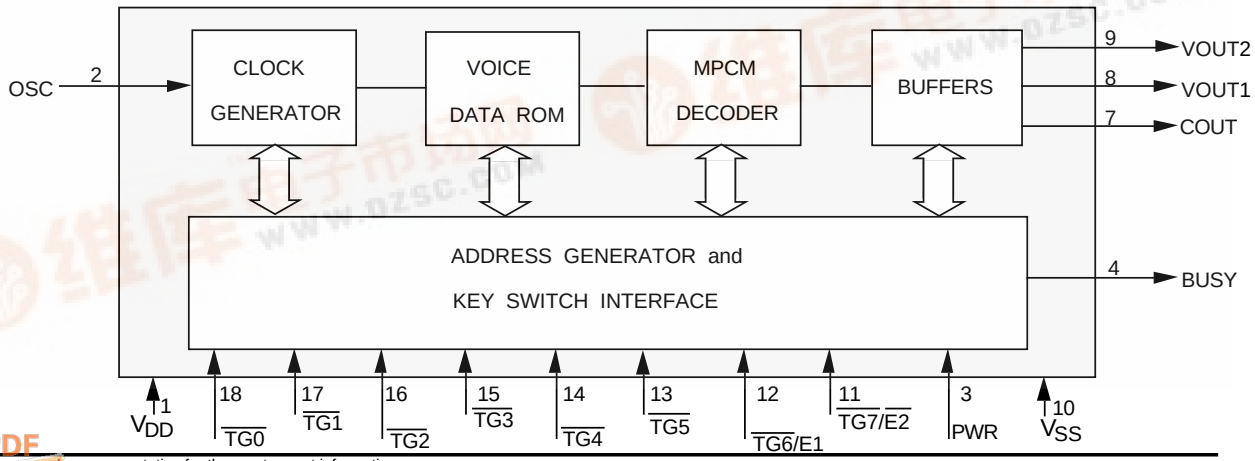
Features

- Single power can operate at 2.4 V through 6V.
- Current output could drive 8 ohm speaker with a transistor, Vout could drive buzzer directly.
- The voice content is stored up to 15 seconds and can be separated to 64 sections.
- Duration of each section can be different.
- Mute is available for each section up to 48 seconds totally.
- A Forever Play function is available.
- Four addressing interface modes are provided for versatile applications: CPU, Stand alone, Ring Trigger and Table Trigger.
- Stand alone mode:
  8 sections can be accessed by 8 trigger input pins individually.
- Table trigger mode:
  a. A phrase is accessed by $\overline{TG0}$, low active.
  b. This phrase is composed of 16 elements contiguously as the table content.
  c. These 16 elements are chosen from 8 sections.
  d. Section is located and numbered by 0 through 7.
- Ring trigger mode:
  a. A section-by-section phrase is accessed by $\overline{TG0}$, low active.
  b. This phrase is composed of 16 element (section)s contiguously as the table content.
  c. Each single trigger plays next one element (section) following above sequence.
  d. These 16 elements are chosen from 8 sections.
  e. Section is located and numbered by 0 through 7.
- CPU addressing mode:
  a. 64 sections can be accessed by 6 address bits with enable strobe trigger.
  b. Section is located and numbered by 0 through 63.
  c. The address bit is high true.
- Mask option for either retriggerable output or not.
- Mask option for either Level or Edge trigger type.
- For all four modes, retrigger action restarts playing from the beginning.
- One BUSY output signal is available.
- Automatic power down function(selected by external input, pwr).

General Description

The MSS1506 is a single-chip CMOS LSI ROM that can memorize voice up to 15 seconds using MOSEL qualified coding method (MPCM).
Four addressing interfaces are provided: CPU mode, Stand Alone mode, Ring Trigger mode and Table Trigger mode for versatile applications. The voice content can be stored separatly into 64 or 8 or 16 sections or 1 phrase with arbitary length. With minimum external components, this chip can be applied to various application. Customer voice is edited and programmed into ROM by changing one mask during fabrication.

Block Diagram



Absolute Maximum Rating

Symbol	Rating	Unit
V_{DD} ~ V_{SS}	-0.5 ~ +7.0	V
V_{IN} (TG) all input pins	V_{SS} -0.3 < V_{IN} < V_{DD}+0.3	V
V_{OUT} (STS) all output pins	V_{SS} <V_{OUT} < V_{DD}	V
T (Operating)	-10 ~ +60	°C
T (Storage)	-55 ~ +125	°C

Pad Description

Pad No.	Signal Name	I/O	Function
1	V_{DD}	Power	Positive power supply
2	OSC	I	Oscillator input
3	PWR	I	Active high for non-power down, Internal pull low
4	BUSY	O	Busy signal output, active high
5	NC		
6	NC		
7	C_{OUT}	O	Audio signal current output (for speaker)
8	V_{OUT1}	O	Audio signal voltage output (for buzzer)
9	V_{OUT2}	O	Audio signal voltage output (for buzzer)
10	V_{SS}	Power	Negative power supply
11	$\overline{E2}$, $\overline{TG7}$	NC/I	No connection (RT,TT);Trigger 7, active low(SA); Enable 2, active low (CPU)
12	E1, $\overline{TG6}$	NC/I	No connection (RT,TT);Trigger 6, active low (SA); Enable 1, active high (CPU)
13	$\overline{TG5}$	NC/I	No connection (RT, TT); Trigger 1 ~ 5, active low (SA); address 1 ~ 5, high true (CPU)
14	$\overline{TG4}$	NC/I	
15	$\overline{TG3}$	NC/I	
16	$\overline{TG2}$	NC/I	
17	$\overline{TG1}$	NC/I	
18	$\overline{TG0}$	I	Trigger 0, active low (RT TT, SA); address 0 high true (CPU)

AC Characteristics

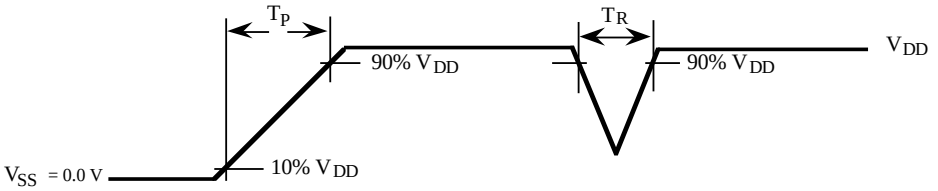
Timing	Parameter	Min.	Typ.	Max.	Unit.
T_T	Trigger pulse width	10	—	—	ms
T_W	Write Enable pulse width	300	—	—	ns
T_H	Trigger address hold time	80	—	—	ns
T_P	Power rise up time	—	—	1	ms
T_R	Power Ripple width	—	—	1	ms

DC Characteristics

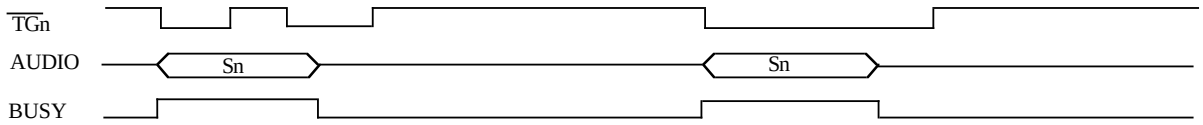
Symbol	Parameter		Min.	Typ.	Max.	Unit	Condition
I_{SB}	Supply Current	Stand by	—	1	—	μA	V_{DD} = 4.5V, I/O Open
I_{OP}		Operating	—	—	200		
V_{IH}	Input Voltage ($\overline{T0}$~$\overline{T7}$, E1,$\overline{E2}$, PWR)		4	4.5	5	V	V_{DD} = 4.5V
V_{IL}			-0.3	0	0.3		
I_{IH}	Input Current ($\overline{T0}$~$\overline{T7}$)		—	0	—	μA	V_{DD} = 4.5V
I_{IL}			—	—	-15		
I_{IH}	Input Current for PWR		—	—	20	μA	V_{DD} = 4.5V
I_{IL}			—	0	—		
I_{OH}	O/P Current V_{OUT1} ,V_{OUT2}	Drive	-8	-13	-18	mA	V_{DD} = 4.5V, $V_{O/P}$ = 0V
I_{OL}		Sink	8	13	18		V_{DD} = 4.5V, $V_{O/P}$ = 4.5V
I_{OH}	Output Current (BUSY)		—	2	—	mA	V_{DD} = 4.5V, $V_{O/P}$ = 0V
I_{OL}			—	4	—		V_{DD} = 4.5V, $V_{O/P}$ = 4.5V
I_{CO}	Output Current (C_{OUT})		2.4	3	3.6	mA	V_{DD} = 4.5V
ΔF/F	Frequency Stability		—	—	5	%	[Fosc(4.5V) - Fosc(4V)]/Fosc(4.5V)
ΔF/F	Frequency Variation		—	—	10	%	V_{DD} = 4.5V, Rosc = 1.2MΩ

Timing Diagram

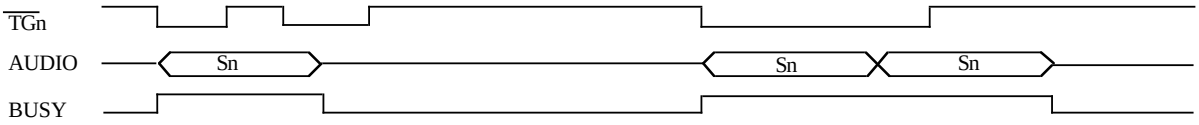
I.1. Acceptable Power On Signal & Ripple



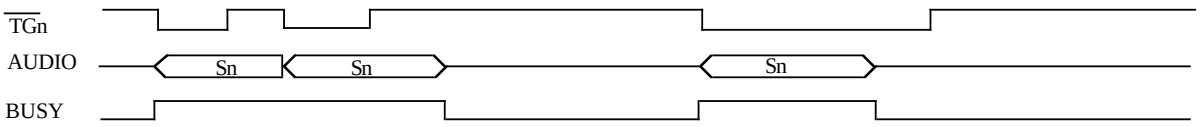
II.1. Stand Alone mode, No Retrigger function, Edge Trigger Mask, low active, single trigger input



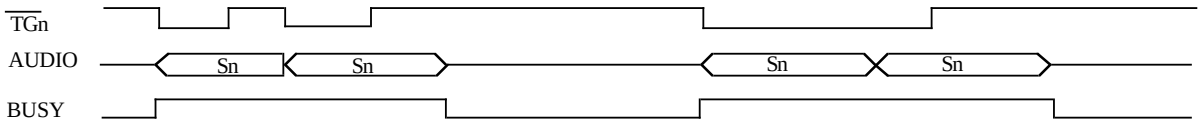
II.2. Stand Alone mode, No Retrigger function, Level Trigger Mask, low active, single trigger input



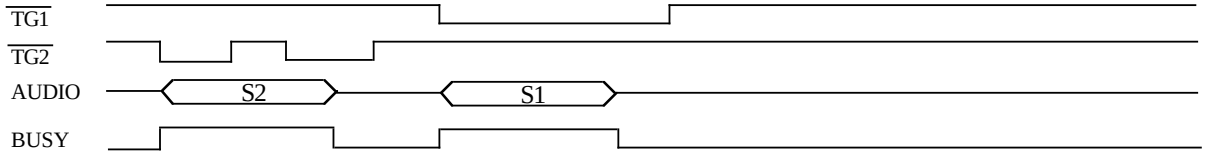
III.1. Stand Alone mode, Retrigger function, Edge Trigger Mask, low active, single trigger input



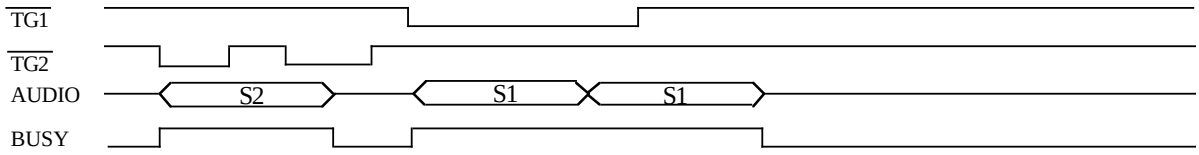
III.1. Stand Alone mode, Retrigger function, Level Trigger Mask, low active, single trigger input



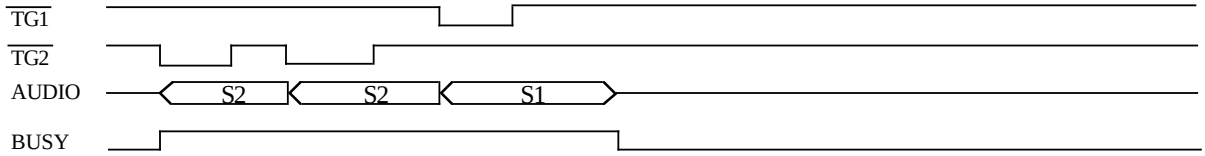
IV. 1. Stand Alone mode, No Retrigger function, Edge Trigger Mask, low active, two non - overlap trigger inputs



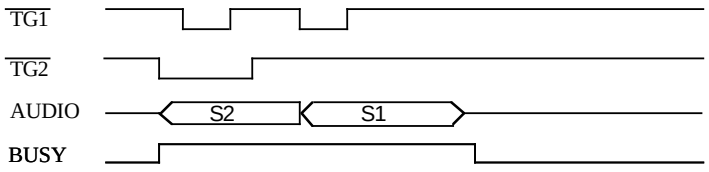
IV. 2. Stand Alone mode, No Retrigger function, Level Trigger Mask, low active, two non - overlap trigger inputs



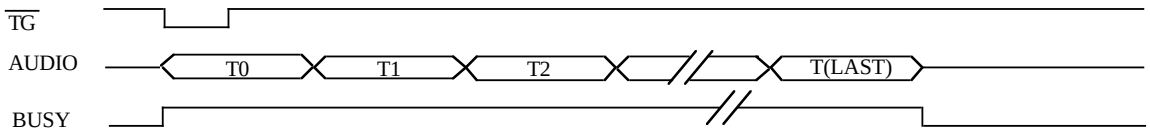
IV. 3. Stand Alone mode, Retrigger function, low active, two non - overlap trigger inputs



V. 4. Retrigger function , Trigger Mask = Edge or Level, Overlap trigger inputs

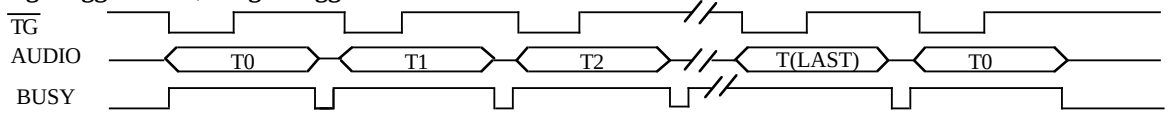


V. Table Trigger Mask



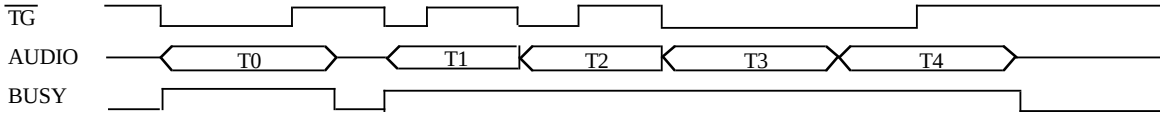
NOTE: Tn = nth element of Table content.

VII. Ring Trigger mode, Edge Trigger Mask

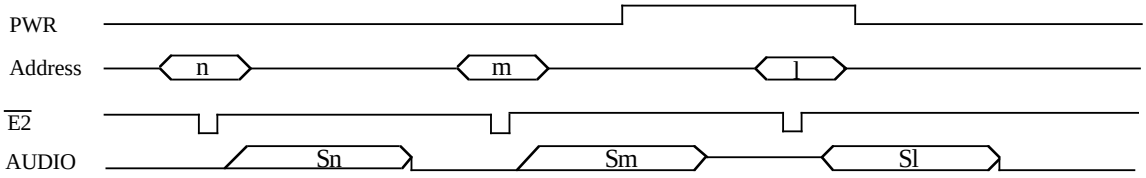


VIII. Ring Trigger mode, Level Trigger Mask

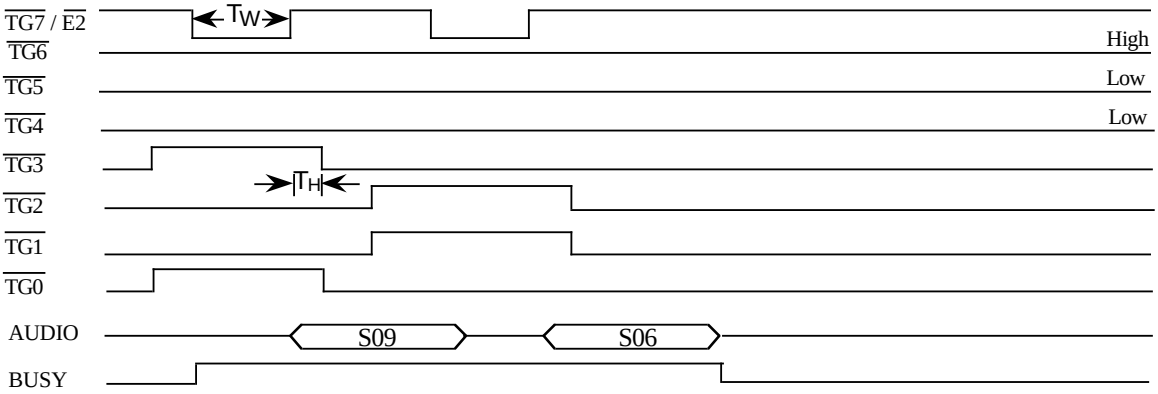
a. When trigger is shorter than a whole section output b. When trigger is longer than a whole section output



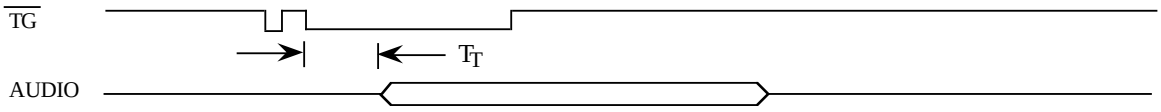
IX. Power keep function



X. Mask as Retrigger / CPU mode (6 - bit address)



XI. Debounce Time

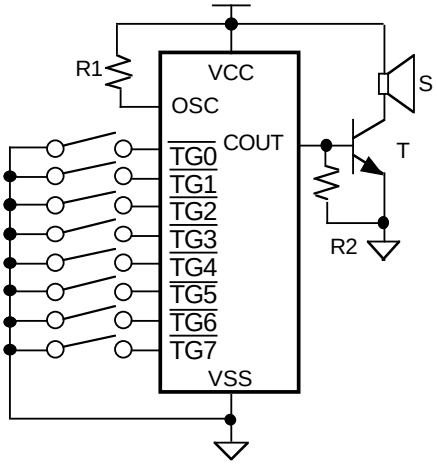


Note: 1. AUDIO means cout, vout1, vout2.
2. $\overline{TG0}$ ~ $\overline{TG5}$, E1/$\overline{TG6}$, $\overline{E2}$/$\overline{TG7}$ are all internal pull high.
3. For standalone mode, $\overline{TG0}$ ~ $\overline{TG7}$ are used as section trigger input (active low).
4. Every retrigger action will reload address and play the audio output from the beginning.
5. In CPU mode to avoid unwanted noise caused by abrupt change between different sections of messages, it is recommended to program PWR pin to high (V_{DD}) during voice processing.

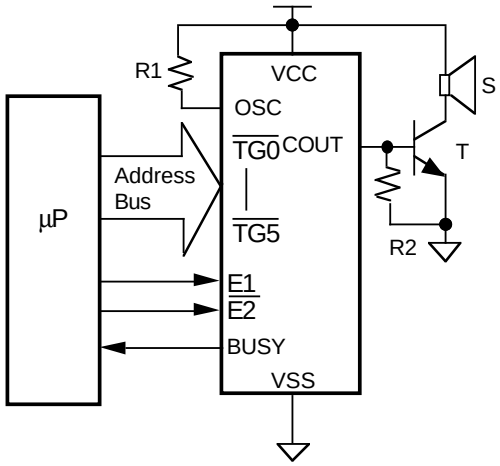
Application Circuit

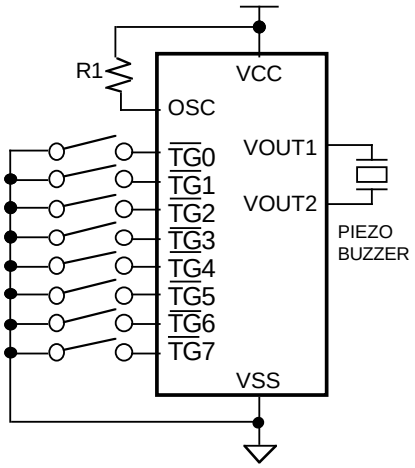
1.Typical Application

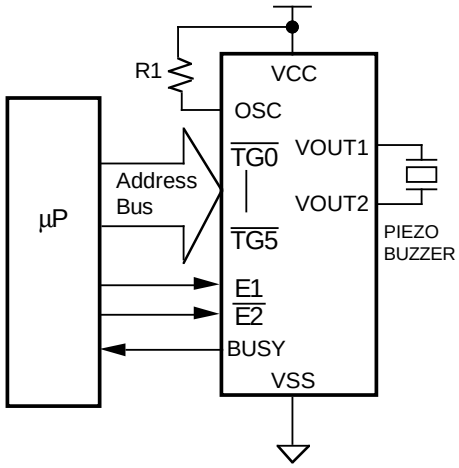
a.Standalone



b.CPU Mode

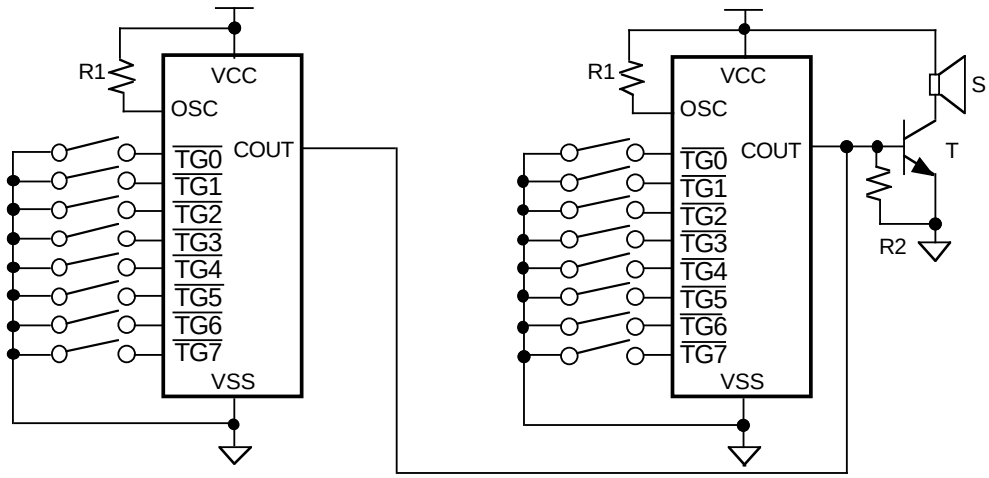


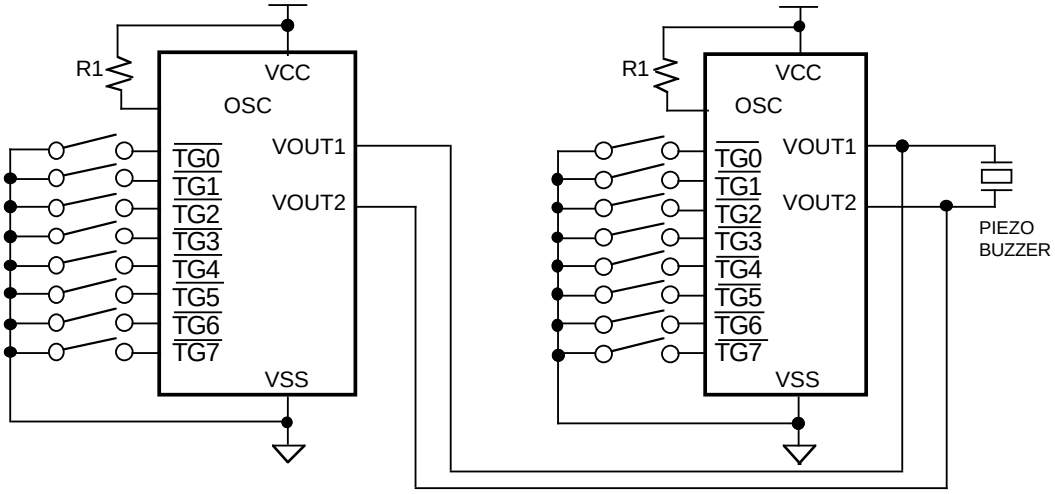




2.Parallel Application

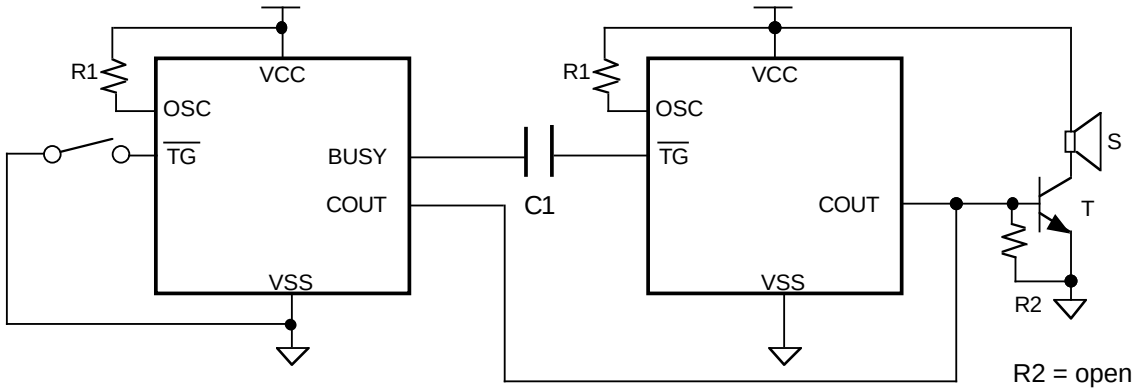
(Could extend depth to desired section number in parallel arrangement)



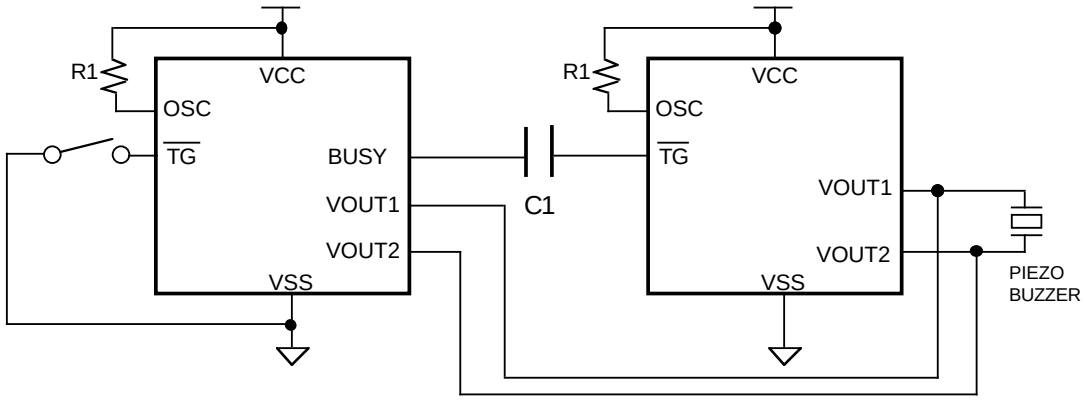


3.Cascade Application

(Could extend length to desired length in serial arrangement)



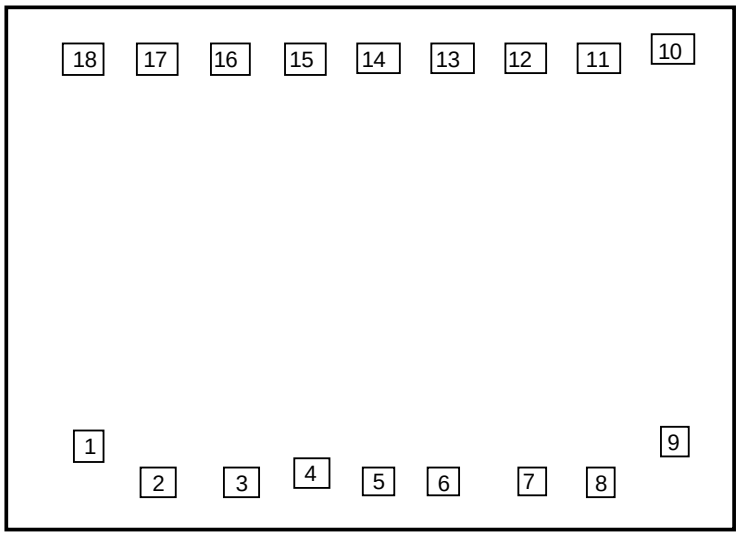
R2 = open is better.



Note: 1. R1 = 1.2 M Ω, C1 = 0.1 µf, T(transistor) = ß > 150, R2 =open, S(speaker) = 1/4 w, 8 Ω; all typical.
2. Piezo buzzer resonant frequency being around 1K Hz in recommended.
3. Input switch could be replaced by CDS.
4. Cout,Vout1,Vout2 are tristate during stand by state.
5. Both cascade and parallel application are applied in CPU mode.

Bonding Diagram

Pad No.	Designation
1	V_{DD}
2	OSC
3	PWR
4	BUSY
5	NC
6	NC
7	C_{OUT}
8	V_{OUT1}
9	V_{OUT2}
10	V_{SS}
11	$\overline{TG_7}$
12	$\overline{TG_6}$
13	$\overline{TG_5}$
14	$\overline{TG_4}$
15	$\overline{TG_3}$
16	$\overline{TG_2}$
17	$\overline{TG_1}$
18	$\overline{TG_0}$



Note: Substrate is V_{DD}