DDR SDRAM Small-Outline DIMM

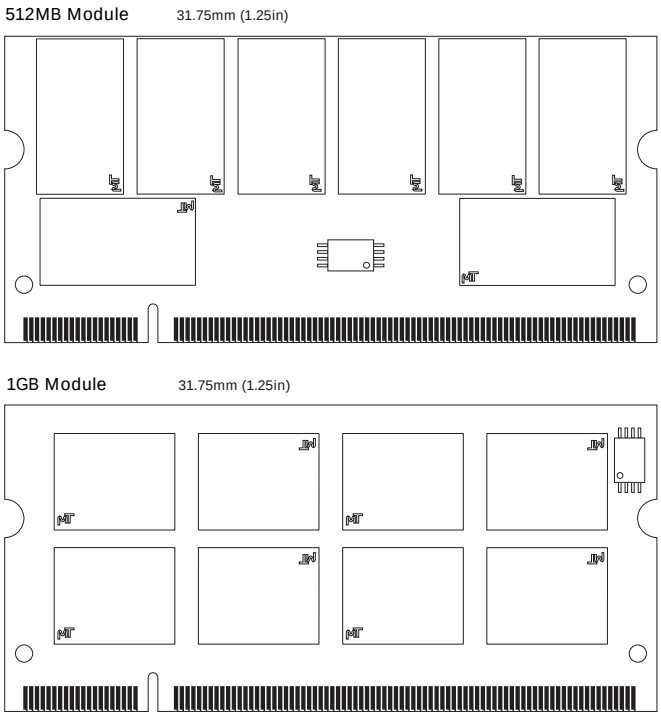
MT16VDDF6464H – 512MB
MT16VDDF12864H – 1GB

For the latest component data sheet, refer to the Micron's Web site: www.micron.com/products/modules

Features

- 200-pin, small-outline, dual in-line memory module (SODIMM)
- Fast data transfer rates: PC3200
- Utilizes 400 MT/s DDR SDRAM components
- 512MB (64 Meg x 64), 1GB (128 Meg x 64)
- V_{DD} = $V_{DD}Q$ = +2.6V
- 2.6V I/O (SSTL_2 compatible)
- V_{DDSPD} = +2.3V to +3.6V
- Commands entered on each positive CK edge
- DQS edge-aligned with data for READs; center-aligned with data for WRITEs
- Internal, pipelined double data rate (DDR) architecture; two data accesses per clock cycle
- Bidirectional data strobe (DQS) transmitted/ received with data—i.e., source-synchronous data capture
- Differential clock inputs CK and CK#
- Four internal device banks for concurrent operation
- Programmable burst lengths: 2, 4, or 8
- Auto precharge option
- Auto refresh and self refresh modes
- 7.8125µs maximum average periodic refresh interval
- Serial presence detect (SPD) with EEPROM
- Programmable READ CAS latency (CL)
- Gold edge contacts

Figure 1: 200-Pin SODIMM (MO-224)



Options	Marking
• Package	
200-pin SODIMM (standard)[1]	G
200-pin SODIMM (lead-free)	Y
• Memory clock, speed, CAS latency[2]	
5ns (200 MHz), 400 MT/s, CL = 3	-40B
• PCB height	
31.75mm (1.25in)	

Notes: 1. Contact Micron for product availability.
2. CL = CAS (READ) latency.

Table 1: Address Table

	512MB	1GB
Refresh count	8K	8K
Device row addressing	8K (A0–A12)	8K (A0–A12)
Device bank addressing	4 (BA0, BA1)	4 (BA0, BA1)
Device configuration	256Mb (32 Meg x 8)	512Mb (64 Meg x 8)
Device column addressing	1K (A0–A9)	2K (A0–A9, A11)
Module rank addressing	2 (S0#, S1#)	2 (S0#, S1#)

Table 2: Part Numbers and Timing Parameters – 512MB

Part Number	Module Density	Configuration	Transfer Rate	Memory Clock/ Data Rate	Latency (CL - ^{t}RCD - ^{t}RP)
MT16VDDF6464HG-40B__	512MB	64 Meg x 64	3.2 GB/s	5ns/400 MT/s	3-3-3
MT16VDDF6464HY-40B__	512MB	64 Meg x 64	3.2 GB/s	5ns/400 MT/s	3-3-3

Table 3: Part Numbers and Timing Parameters – 1GB

Part Number	Module Density	Configuration	Transfer Rate	Memory Clock/ Data Rate	Latency (CL - ^{t}RCD - ^{t}RP)
MT16VDDF12864HG-40B__	1GB	128 Meg x 64	3.2 GB/s	5ns/400 MT/s	3-3-3
MT16VDDF12864HY-40B__	1GB	128 Meg x 64	3.2 GB/s	5ns/400 MT/s	3-3-3

Note: All part numbers end with a two-place code (not shown), designating component and PCB revisions. Consult factory for current Revision codes. Example: MT16VDDF6464HG-40BA1.

Pin Assignments and Descriptions

Table 4: Pin Assignments

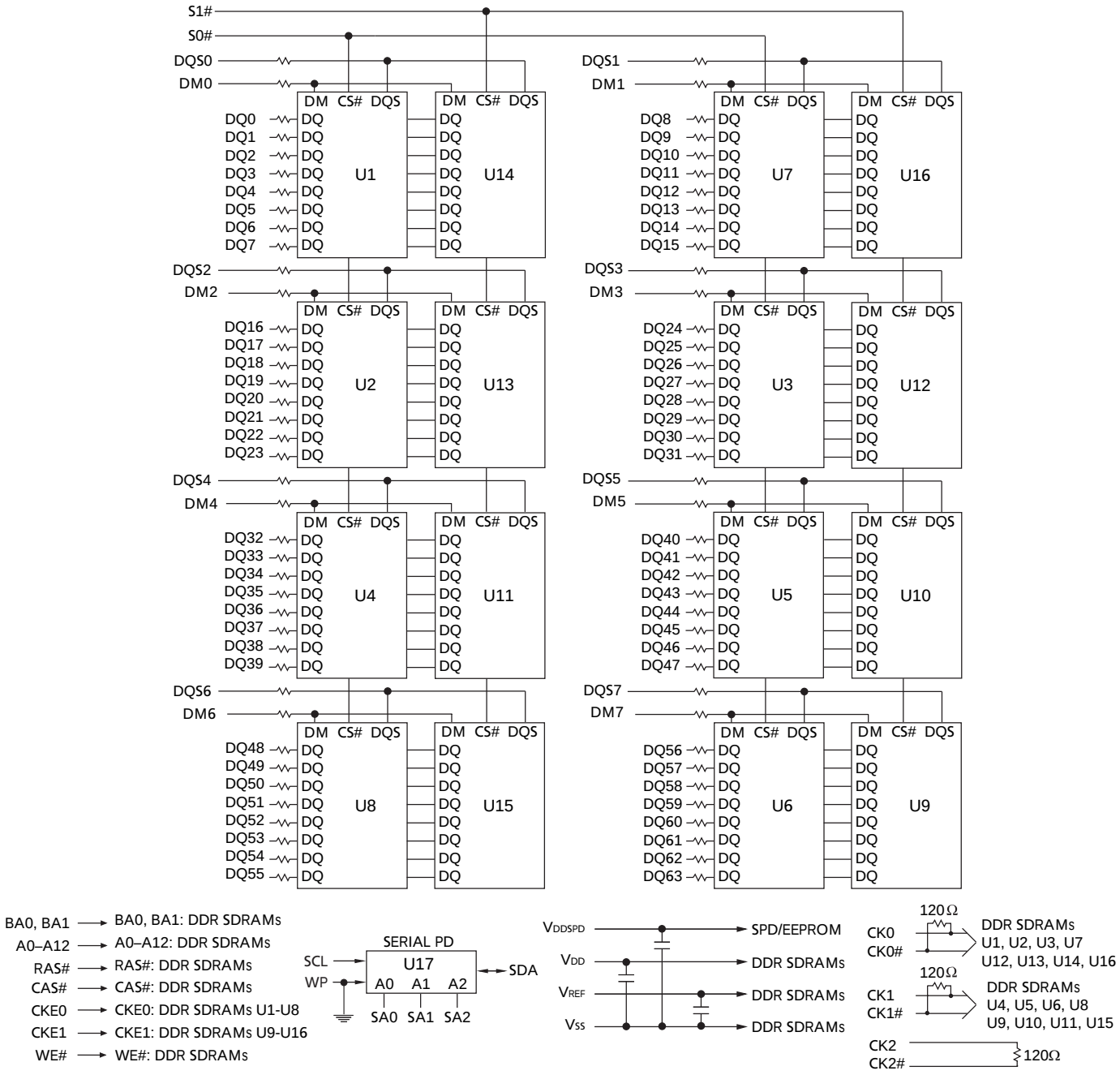
200-Pin SODIMM Front								200-Pin SODIMM Back							
Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
1	VREF	51	VSS	101	A9	151	DQ42	2	VREF	52	VSS	102	A8	152	DQ46
3	VSS	53	DQ19	103	VSS	153	DQ43	4	VSS	54	DQ23	104	VSS	154	DQ47
5	DQ0	55	DQ24	105	A7	155	VDD	6	DQ4	56	DQ28	106	A6	156	VDD
7	DQ1	57	VDD	107	A5	157	VDD	8	DQ5	58	VDD	108	A4	158	CK1#
9	VDD	59	DQ25	109	A3	159	VSS	10	VDD	60	DQ29	110	A2	160	CK1
11	DQS0	61	DQS3	111	A1	161	VSS	12	DM0	62	DM3	112	A0	162	VSS
13	DQ2	63	VSS	113	VDD	163	DQ48	14	DQ6	64	VSS	114	VDD	164	DQ52
15	VSS	65	DQ26	115	A10	165	DQ49	16	VSS	66	DQ30	116	BA1	166	DQ53
17	DQ3	67	DQ27	117	BA0	167	VDD	18	DQ7	68	DQ31	118	RAS#	168	VDD
19	DQ8	69	VDD	119	WE#	169	DQS6	20	DQ12	70	VDD	120	CAS#	170	DM6
21	VDD	71	DNU	121	S0#	171	DQ50	22	VDD	72	DNU	122	S1#	172	DQ54
23	DQ9	73	DNU	123	NC	173	VSS	24	DQ13	74	DNU	124	NC	174	VSS
25	DQS1	75	VSS	125	VSS	175	DQ51	26	DM1	76	VSS	126	VSS	176	DQ55
27	VSS	77	DNU	127	DQ32	177	DQ56	28	VSS	78	DNU	128	DQ36	178	DQ60
29	DQ10	79	DNU	129	DQ33	179	VDD	30	DQ14	80	DNU	130	DQ37	180	VDD
31	DQ11	81	VDD	131	VDD	181	DQ57	32	DQ15	82	VDD	132	VDD	182	DQ61
33	VDD	83	DNU	133	DQS4	183	DQS7	34	VDD	84	DNU	134	DM4	184	DM7
35	CK0	85	NC	135	DQ34	185	VSS	36	VDD	86	DNU	136	DQ38	186	VSS
37	CK0#	87	VSS	137	VSS	187	DQ58	38	VSS	88	VSS	138	VSS	188	DQ62
39	VSS	89	DNU	139	DQ35	189	DQ59	40	VSS	90	VSS	140	DQ39	190	DQ63
41	DQ16	91	DNU	141	DQ40	191	VDD	42	DQ20	92	VDD	142	DQ44	192	VDD
43	DQ17	93	VDD	143	VDD	193	SDA	44	DQ21	94	VDD	144	VDD	194	SA0
45	VDD	95	CKE1	145	DQ41	195	SCL	46	VDD	96	CKE0	146	DQ45	196	SA1
47	DQS2	97	NC	147	DQS5	197	VDDSPD	48	DM2	98	NC	148	DM5	198	SA2
49	DQ18	99	A12	149	VSS	199	NC	50	DQ22	100	A11	150	VSS	200	VSS

Table 5: Pin Descriptions

Symbol	Type	Description
WE#, CAS#,RAS#	Input	Command inputs: RAS#, CAS#, and WE# (along with S#) define the command being entered.
CK0, CK0# CK1, CK1#	Input	Clock: CK, CK# are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK, and negative edge of CK#. Output data (DQs and DQS) is referenced to the crossings of CK and CK#.
CKE0, CKE1	Input	Clock enable: CKE HIGH activates and CKE LOW deactivates the internal clock, input buffers and output drivers. Taking CKE LOW provides precharge power-down and SELF REFRESH operations (all device banks idle), or active power-down (row ACTIVE in any device bank). CKE is synchronous for power-down entry and exit, and for SELF REFRESH entry. CKE is asynchronous for SELF REFRESH exit and for disabling the outputs. CKE must be maintained HIGH throughout read and write accesses. Input buffers (excluding CK, CK# and CKE) are disabled during power-down. Input buffers (excluding CKE) are disabled during SELF REFRESH. CKE is an SSTL_2 input but will detect an LVCMOS LOW level after V_{DD} is applied and until CKE is first brought HIGH. After CKE is brought HIGH, it becomes an SSTL_2 input only.
S0#, S1#	Input	Chip selects: S# enables (registered LOW) and disables (registered HIGH) the command decoder. All commands are masked when S# is registered HIGH. S# is considered part of the command code.
BA0, BA1	Input	Bank address: BA0 and BA1 define to which device bank an ACTIVE, READ, WRITE, or PRECHARGE command is being applied.
A0–A12	Input	Address inputs: Provide the row address for ACTIVE commands, and the column address and auto precharge bit (A10) for READ/WRITE commands, to select one location out of the memory array in the respective device bank. A10 sampled during a PRECHARGE command determines whether the PRECHARGE applies to one device bank (A10 LOW, device bank selected by BA0, BA1) or all device banks (A10 HIGH). The address inputs also provide the op-code during a MODE REGISTER SET command. BA0 and BA1 define which mode register (mode register or extended mode register) is loaded during the LOAD MODE REGISTER command.
SCL	Input	Serial clock for presence-detect: SCL is used to synchronize the presence-detect data transfer to and from the module.
SA0–SA2	Input	Presence-Detect address inputs: These pins are used to configure the presence-detect device.
DM0–DM7	Input	Data write mask. DM LOW allows WRITE operation. DM HIGH blocks WRITE operation. DM lines do not affect READ operation.
SDA	Input/ Output	Serial presence-detect data: SDA is a bidirectional pin used to transfer addresses and data into and out of the presence-detect portion of the module.
DQS0–DQS7	Input/ Output	Data strobe: Output with READ data, input with WRITE data. DQS is edge-aligned with READ data, centered in WRITE data. Used to capture data.
DQ0–DQ63	Input/ Output	Data I/Os: Data bus.
V_{REF}	Supply	SSTL_2 reference voltage.
V_{DD}	Supply	Power supply: +2.6V ±0.1V.
V_{SS}	Supply	Ground.
V_{ddSPD}	Supply	Serial EEPROM positive power supply: +2.3V to +3.6V

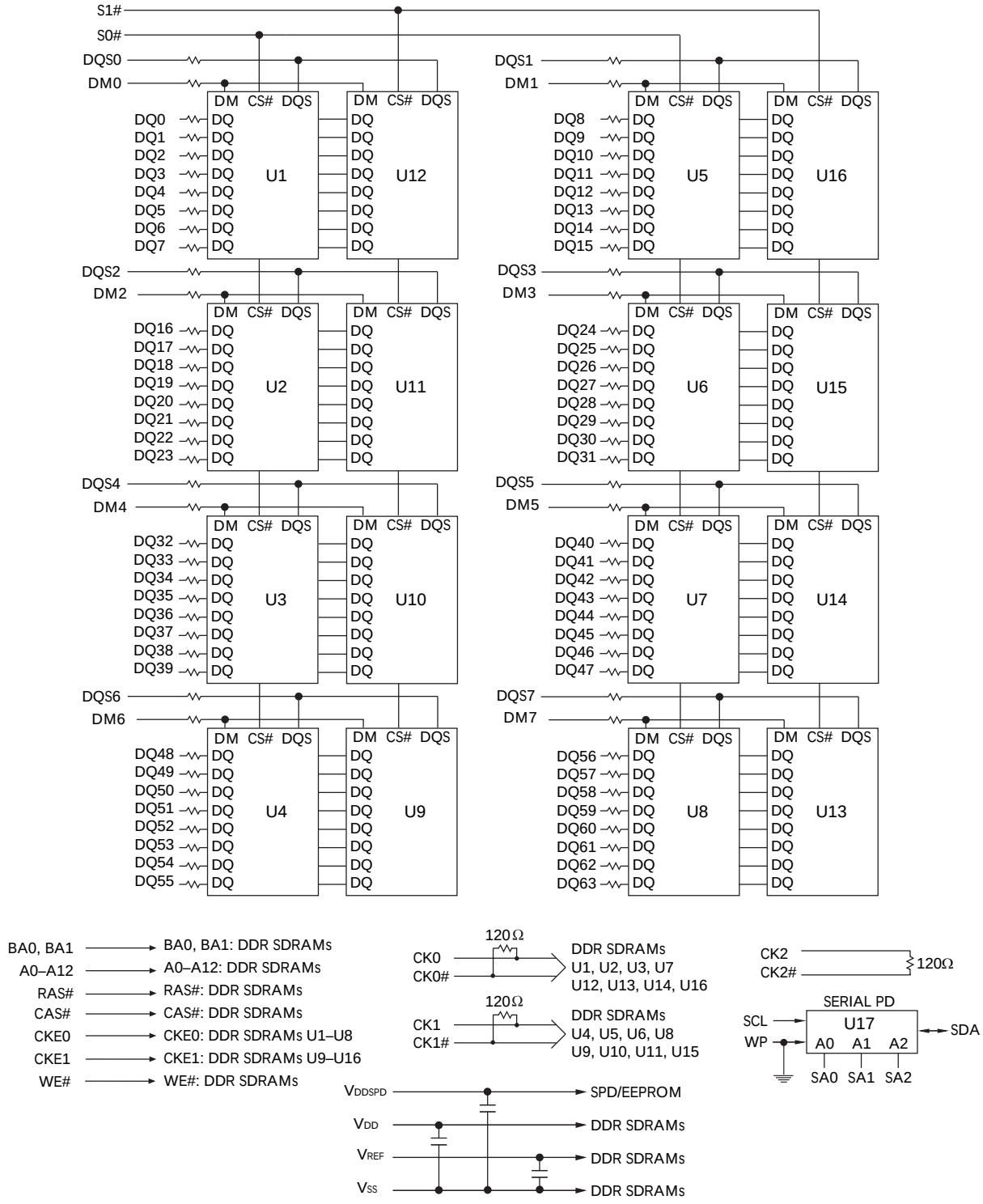
Functional Block Diagrams

Figure 2: Functional Block Diagram – 512MB



Notes: 1. All resistor values are 22Ω unless otherwise specified.

Figure 3: Functional Block Diagram – 1GB



Notes: 1. All resistor values are 22Ω unless otherwise specified.

General Description

The MT16VDDF6464H and MT16VDDF12864H are high-speed CMOS, dynamic random-access, 512MB and 1GB memory modules organized in a x64 configuration. DDR SDRAM modules use internally configured quad-bank DDR SDRAM devices.

DDR SDRAM modules use a double data rate architecture to achieve high-speed operation. The double data rate architecture is essentially a 2*n*-prefetch architecture with an interface designed to transfer two data words per clock cycle at the I/O pins. A single read or write access for the DDR SDRAM module effectively consists of a single 2*n*-bit wide, one-clock-cycle data transfer at the internal DRAM core and two corresponding *n*-bit wide, one-half-clock-cycle data transfers at the I/O pins.

A bidirectional data strobe (DQS) is transmitted externally, along with data, for use in data capture at the receiver. DQS is an intermittent strobe transmitted by the DDR SDRAM during READs and by the memory controller during WRITEs. DQS is edge-aligned with data for READs and center-aligned with data for WRITEs.

DDR SDRAM modules operate from a differential clock (CK and CK#); the crossing of CK going HIGH and CK# going LOW will be referred to as the positive edge of CK. Commands (address and control signals) are registered at every positive edge of CK. Input data is registered on both edges of DQS, and output data is referenced to both edges of DQS, as well as to both edges of CK.

Serial Presence-Detect Operation

DDR SDRAM modules incorporate serial presence-detect (SPD). The SPD function is implemented using a 2,048-bit EEPROM. This nonvolatile storage device contains 256 bytes. The first 128 bytes can be programmed by Micron to identify the module type and various SDRAM organizations and timing parameters. The remaining 128 bytes of storage are available for use by the customer. System READ/WRITE operations between the master (system logic) and the slave EEPROM device (DIMM) occur via a standard I^2C bus using the DIMM's SCL (clock) and SDA (data) signals, together with SA (2:0), which provide eight unique DIMM/EEPROM addresses. Write protect (WP) is tied to ground on the module, permanently disabling hardware write protect.

Table 6: CAS Latency (CL) Table

Speed	Allowable Operating Clock Frequency (MHz)		
	CL = 2	CL = 2.5	CL = 3
-40B	75 ≤ f ≤ 133	75 ≤ f ≤ 167	133 ≤ f ≤ 200

Electrical Specifications

Stresses greater than those listed in Table 7 may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Table 7: Absolute Maximum Ratings
All voltages are relative to V_{SS}.

Parameter	Min	Max	Units
Voltage on V_{DD} supply	–1	+3.6	V
Voltage on V_{DDQ} supply	–1	+3.6	V
Voltage on V_{REF} and inputs	–1	+3.6	V
Voltage on I/O pins	–0.5	V_{DDQ} +0.5	V
Operating temperature T_A (ambient)	0	+70	°C
Storage temperature (plastic)	–55	+150	°C
DDR SDRAM device operating temperature $T_{JUNCTION}$ (Die temperature)	0	+85	°C
DDR SDRAM device operating temperature T_{CASE} (Case temperature)	0	+80	°C
Short circuit output current	–	50	mA

Notes: 1. For further information refer to Micron Technical Note, TN-00-08 located at www.micron.com/support/designsupport/documents/technotes

Table 8: DC Electrical Characteristics and Operating Conditions
$0°C \le T_A \le +70°C$

Parameter/Condition		Symbol	Min	Max	Units
Supply voltage		V_{DD}	2.5	2.7	V
I/O supply voltage		V_{DDQ}	2.5	2.7	V
I/O reference voltage		V_{REF}	0.49 × V_{DDQ}	0.51 × V_{DDQ}	V
I/O termination voltage (system)		V_{TT}	V_{REF} - 0.04	V_{REF} + 0.04	V
Input high (logic 1) voltage		V_{IH}(DC)	V_{REF} + 0.15	V_{DD} + 0.3	V
Input low (logic 0) voltage		V_{IH}(DC)	-0.3	V_{REF} - 0.15	V
Input leakage current Any input 0V ≤ V_{IN} ≤ V_{DD}, V_{REF} pin 0V ≤ V_{IN} ≤ 1.35V (All other pins not under test = 0V)	Command/Address, RAS#, CAS#, WE#	I_I	–32	32	µA
	S#, CKE, CK, CK#		–16	16	
	DM		–4	4	
Output leakage current (DQs are disabled; 0V ≤ V_{OUT} ≤ V_{DDQ})	DQ, DQS	I_{OZ}	–10	10	µA
Output levels High current (V_{OUT} = V_{DDQ} - 0.373V, minimum V_{REF}, minimum V_{TT})		I_{OH}	–16.8	–	mA
Low current (V_{OUT} = 0.373V, maximum V_{REF}, maximum V_{TT})		I_{OL}	16.8	–	mA

Table 9: AC Input Operating Conditions

0°C ≤ T_A ≤ +70°C; V_{DD} = $V_{DD}Q$ = +2.6V ±0.1V

Parameter/Condition	Symbol	Min	Max	Units
Input high (logic 1) voltage	V_{IH}(AC)	V_{REF} + 0.310	–	V
Input low (logic 0) voltage	V_{IL}(AC)	–	V_{REF} - 0.310	V
I/O reference voltage	V_{REF}(AC)	0.49 × $V_{DD}Q$	0.49 × $V_{DD}Q$	V

Table 10: I_{DD} Specifications and Conditions – 512MB

0°C ≤ T_A ≤ +70°C; V_{DD}, $V_{DD}Q$ = +2.6V ±0.1V

Parameter/Condition		Symbol	Max -40B	Units
Operating current: One device bank; Active-Precharge; ^tRC = ^tRC (MIN); ^tCK = ^tCK (MIN); DQ, DM and DQS inputs changing once per clock cycle; Address and control inputs changing once every two clock cycles		I_{DD0}[a]	1,112	mA
Operating current: One device bank; Active-Read-Precharge; Burst = 4; ^tRC = ^tRC (MIN); ^tCK = ^tCK (MIN); I_{OUT} = 0mA; Address and control inputs changing once per clock cycle		I_{DD1}[a]	1,392	mA
Precharge power-down standby current: All device banks idle; Power-down mode; ^tCK = ^tCK (MIN); CKE = (LOW)		I_{DD2P}[b]	64	mA
Idle standby current: CS# = HIGH; All device banks are idle; ^tCK = ^tCK (MIN); CKE = HIGH; Address and other control inputs changing once per clock cycle. V_{IN} = V_{REF} for DQ, DQS, and DM		I_{DD2F}[b]	960	mA
Active power-down standby current: One device bank active; Power-down mode; ^tCK = ^tCK (MIN); CKE = LOW		I_{DD3P}[b]	640	mA
Active standby current: CS# = HIGH; CKE = HIGH; One device bank active; ^tRC = ^tRAS (MAX); ^tCK = ^tCK (MIN); DQ, DM and DQS inputs changing twice per clock cycle; Address and other control inputs changing once per clock cycle		I_{DD3N}[b]	1,120	mA
Operating current: Burst = 2; Reads; Continuous burst; One device bank active; Address and control inputs changing once per clock cycle; ^tCK = ^tCK (MIN); I_{OUT} = 0mA		I_{DD4R}[a]	1,632	mA
Operating current: Burst = 2; Writes; Continuous burst; One device bank active; Address and control inputs changing once per clock cycle; ^tCK = ^tCK (MIN); DQ, DM, and DQS inputs changing twice per clock cycle		I_{DD4W}[a]	1,592	mA
Auto refresh burst current:	^tREFC = ^tRFC (MIN)	I_{DD5}[b]	4,160	mA
	^tREFC = 7.8125µs	I_{DD5A}[b]	96	mA
Self refresh current: CKE ≤ 0.2V		I_{DD6}[b]	64	mA
Operating current: Four device bank interleaving READs (Burst = 4) with auto precharge, ^tRC = minimum ^tRC allowed; ^tCK = ^tCK (MIN); Address and control inputs change only during Active READ, or WRITE commands		I_{DD7}[a]	3,792	mA

Notes: 1. a: Value calculated as one module rank in this operating condition; all other module ranks are calculated in I_{DD2P} (CKE LOW) mode
b: Value calculated reflects all module ranks in this operating condition.

Table 11: IDD Specifications and Conditions – 1GB
0°C ≤ T_A ≤ +70°C; VDD, VDDQ = +2.6V ±0.1V

Parameter/Condition		Symbol	Max -40B	Units	Notes
Operating current: One device bank; Active-Precharge; tRC = tRC (MIN); tCK = tCK (MIN); DQ, DM and DQS inputs changing once per clock cycle; Address and control inputs changing once every two clock cycles		IDD0	1,280	mA	14, 25
Operating current: One device bank; Active-Read-Precharge; Burst = 4; tRC = tRC (MIN); tCK = tCK (MIN); IOUT = 0mA; Address and control inputs changing once per clock cycle		IDD1	1,520	mA	14, 25
Precharge power-down standby current: All device banks idle; Power-down mode; tCK = tCK (MIN); CKE = (LOW)		IDD2P	80	mA	15, 18, 27
Idle standby current: CS# = HIGH; All device banks are idle; tCK = tCK (MIN); CKE = HIGH; Address and other control inputs changing once per clock cycle. VIN = VREF for DQ, DQS, and DM		IDD2F	880	mA	28
Active power-down standby current: One device bank active; Power-down mode; tCK = tCK (MIN); CKE = LOW		IDD3P	720	mA	15, 18, 27
Active standby current: CS# = HIGH; CKE = HIGH; One device bank active; tRC = tRAS (MAX); tCK = tCK (MIN); DQ, DM and DQS inputs changing twice per clock cycle; Address and other control inputs changing once per clock cycle		IDD3N	960	mA	
Operating current: Burst = 2; Reads; Continuous burst; One device bank active; Address and control inputs changing once per clock cycle; tCK = tCK (MIN); IOUT = 0mA		IDD4R	1,560	mA	14, 25
Operating current: Burst = 2; Writes; Continuous burst; One device bank active; Address and control inputs changing once per clock cycle; tCK = tCK (MIN); DQ, DM, and DQS inputs changing twice per clock cycle		IDD4W	1,600	mA	14
Auto refresh burst current:	tREFC = tRFC (MIN)	IDD5	5,520	mA	14, 27
	tREFC = 7.8125µs	IDD5A	176	mA	16, 27
Self refresh current: CKE ≤ 0.2V		IDD6	80	mA	9
Operating current: Four device bank interleaving READs (Burst = 4) with auto precharge, tRC = minimum tRC allowed; tCK = tCK (MIN); Address and control inputs change only during Active READ, or WRITE commands		IDD7	3,640	mA	14, 26

Notes: 1. a: Value calculated as one module rank in this operating condition, and all other module ranks are calculated in IDD2P (CKE LOW) mode.
b: Value calculated reflects all module ranks in this operating condition.

Capacitance

Micron encourages designers to simulate the performance of the module to achieve optimum values. When inductance and delay parameters associated with trace lengths are used in simulations, they are significantly more accurate and realistic than a gross estimation of module capacitance. Simulations can then render a considerably more accurate result. JEDEC modules are now designed by using simulations to close timing budgets.

AC Timing and Operating Conditions

Recommended AC operating conditions are given in the DDR component data sheets. Component specifications are available on Micron's Web site: www.micron.com/products/dram/ddr. Module speed grades correlate with component speed grades as shown in Table 12.

Table 12: Module and Component Speed Grades

Module Speed Grade	Component Speed Grade
-40B	-5B

Serial Presence-Detect

Table 13: Serial Presence-Detect EEPROM DC Operating Conditions
All voltages referenced to V_{SS}; V_{DDSPD} = +2.3V to +3.6V

Parameter/Condition	Symbol	Min	Max	Units
Supply voltage	V_{DDSPD}	2.3	3.6	V
Input high voltage: Logic 1; All inputs	V_{IH}	$V_{DD} \times 0.7$	V_{DD} + 0.5	V
Input low voltage: Logic 0; All inputs	V_{IL}	-1	$V_{DD} \times 0.3$	V
Output low voltage: I_{OUT} = 3mA	V_{OL}	–	0.4	V
Input leakage current: V_{IN} = GND to V_{DD}	I_{LI}	–	10	µA
Output leakage current: V_{OUT} = GND to V_{DD}	I_{LO}	–	10	µA
Standby current: SCL = SDA = V_{DD} - 0.3V; All other inputs = V_{DD} or V_{SS}	I_{SB}	–	30	µA
Power supply current: SCL clock frequency = 100 KHz	I_{CC}	–	2	mA

Table 14: Serial Presence-Detect EEPROM AC Operating Conditions
All voltages referenced to V_{SS}; V_{DDSPD} = +2.3V to +3.6V

Parameter/Condition	Symbol	Min	Max	Units	Notes
SCL LOW to SDA data-out valid	^{t}AA	0.2	0.9	µs	1
Time the bus must be free before a new transition can start	^{t}BUF	1.3		µs	
Data-out hold time	^{t}DH	200		ns	
SDA and SCL fall time	^{t}F		300	ns	2
Data-in hold time	$^{t}HD:DAT$	0		µs	
Start condition hold time	$^{t}HD:STA$	0.6		µs	
Clock HIGH period	$^{t}HIGH$	0.6		µs	
Noise suppression time constant at SCL, SDA inputs	^{t}I		50	ns	
Clock LOW period	^{t}LOW	1.3		µs	
SDA and SCL rise time	^{t}R		0.3	µs	2
SCL clock frequency	^{f}SCL		400	KHz	
Data-in setup time	$^{t}SU:DAT$	100		ns	
Start condition setup time	$^{t}SU:STA$	0.6		µs	3
Stop condition setup time	$^{t}SU:STO$	0.6		µs	
WRITE cycle time	^{t}WRC		10	ms	4

Notes:
1. To avoid spurious start and stop conditions, a minimum delay is placed between SCL = 1 and the falling or rising edge of SDA.
2. This parameter is sampled.
3. For a restart condition, or following a WRITE cycle.
4. The SPD EEPROM WRITE cycle time (^{t}WRC) is the time from a valid stop condition of a write sequence to the end of the EEPROM internal erase/program cycle. During the WRITE cycle, the EEPROM bus interface circuit is disabled, SDA remains HIGH due to pull-up resistor, and the EEPROM does not respond to its slave address.

Table 15: Serial Presence-Detect Matrix

"1"/"0": Serial Data, "driven to HIGH"/"driven to LOW"

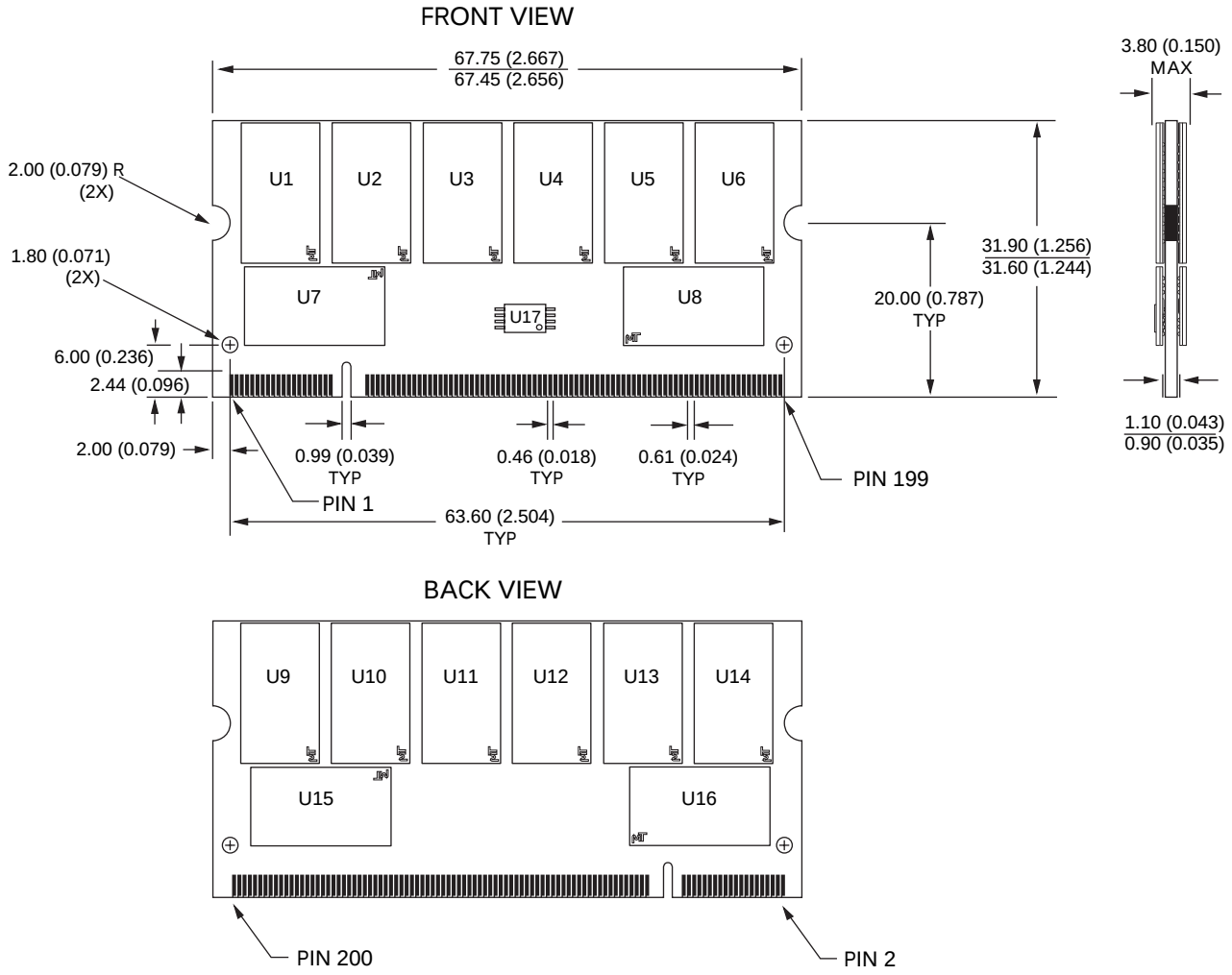
Byte	Description	Entry (Version)	MT16VDDF6464H	MT16VDDF12864H
0	Number of SPD bytes used by micron	128	80	80
1	Total number of bytes in SPD device	256	08	08
2	Fundamental memory type	DDR SDRAM	07	07
3	Number of row addresses on assembly	13	0D	0D
4	Number of column addresses on assembly	10, 11	0A	0B
5	Number of physical ranks on DIMM	2	02	02
6	Module data width	64	40	40
7	Module data width (continued)	0	00	00
8	Module voltage interface levels	SSTL 2.5V	04	04
9	SDRAM cycle time, ^{t}CK (CAS latency = 3)	5ns (-40B)	50	50
10	SDRAM access from clock, ^{t}AC (CAS latency = 3)	0.7ns (-40B)	70	70
11	Module configuration type	Non-ECC	00	00
12	Refresh rate/type	7.8µs/SELF	82	82
13	SDRAM device width (primary DDR SDRAM)	8	08	08
14	Error-checking DDR SDRAM data width	None	00	00
15	Minimum clock delay, back-to-back random column access	1 clock	01	01
16	Burst lengths supported	2, 4, 8	0E	0E
17	Number of Banks on DDR SDRAM device	4	04	04
18	CAS latencies supported	3, 2.5, and 2	1C	1C
19	CS latency	0	01	01
20	WE latency	1	02	02
21	SDRAM module attributes	Unbuffered/Diff. clock	20	20
22	SDRAM device attributes: general	Fast/Concurrent auto precharge	C0	C0
23	SDRAM cycle time, ^{t}CK (CAS latency = 2.5)	6ns (set for PC2700 compatibility)	60	60
24	SDRAM access from clock, ^{t}AC (CAS latency = 2.5)	0.7ns (set for PC2700 compatibility)	70	70
25	SDRAM cycle time, ^{t}CK (CAS latency = 2)	7.5ns (set for PC2100/ PC1600 compatibility)	75	75
26	SDRAM access from CK, ^{t}AC (CAS latency = 2)	0.75ns (set for PC2100/PC1600 compatibility)	75	75
27	Minimum row precharge time, ^{t}RP	15ns (-40B)	3C	3C
28	Minimum row active-to-row active, ^{t}RRD	10ns (-40B)	28	28
29	Minimum RAS#-to-CAS# delay, ^{t}RCD	15ns (-40B)	3C	3C
30	Minimum RAS# pulse width, ^{t}RAS	40ns (-40B)	28	28
31	Module rank density	256MB, 512MB	40	80
32	Address and command setup time, ^{t}IS	0.6ns (-40B)	60	60
33	Address and command hold time, ^{t}IH	0.6ns (-40B)	60	60
34	Data/Data mask input setup time, ^{t}DS	0.40ns (-40B)	40	40
35	Data/Data mask input hold time, ^{t}DH	0.40ns (-40B)	40	40
36-40	Reserved		00	00
41	Minimum active auto refresh time, ^{t}RC	55ns (-40B)	37	37

Table 15: Serial Presence-Detect Matrix (Continued)
"1"/"0": Serial Data, "driven to HIGH"/"driven to LOW"

Byte	Description	Entry (Version)	MT16VDDF6464H	MT16VDDF12864H
42	Minimum AUTO REFRESH to ACTIVE/AUTO REFRESH command period, ^{t}RFC	70ns (-40B)	46	46
43	SDRAM device MAX cycle time, ^{t}CKMAX	12ns (-40B)	30	30
44	SDRAM device MAX DQS-DQ skew time, ^{t}DQSQ	0.4ns (-40B)	28	28
45	SDRAM device MAX read data hold skew factor, ^{t}QHS	0.5ns (-40B)	50	50
46	Reserved		00	00
47	DIMM height		01	01
48–61	Reserved		00	00
62	SPD revision	Release 1.1	11	11
63	Checksum for bytes 0–62	-40B	81	C2
64	Manufacturer's JEDEC ID code	MICRON	2C	2C
65–71	Manufacturer's JEDEC ID code	(Continued)	FF	FF
72	Manufacturing location	01–12	01–0C	01–0C
73–90	Module part number (ASCII)		Variable data	Variable data
91	PCB identification code	1-9	01-09	01-09
92	Identification code (continued)	0	00	00
93	Year of manufacture in BCD	Variable data	Variable data	Variable data
94	Week of manufacture in BCD	Variable data	Variable data	Variable data
95–98	Module serial number	Variable data	Variable data	Variable data
99–127	Manufacturer-Specific data (RSVD)	–	–	–

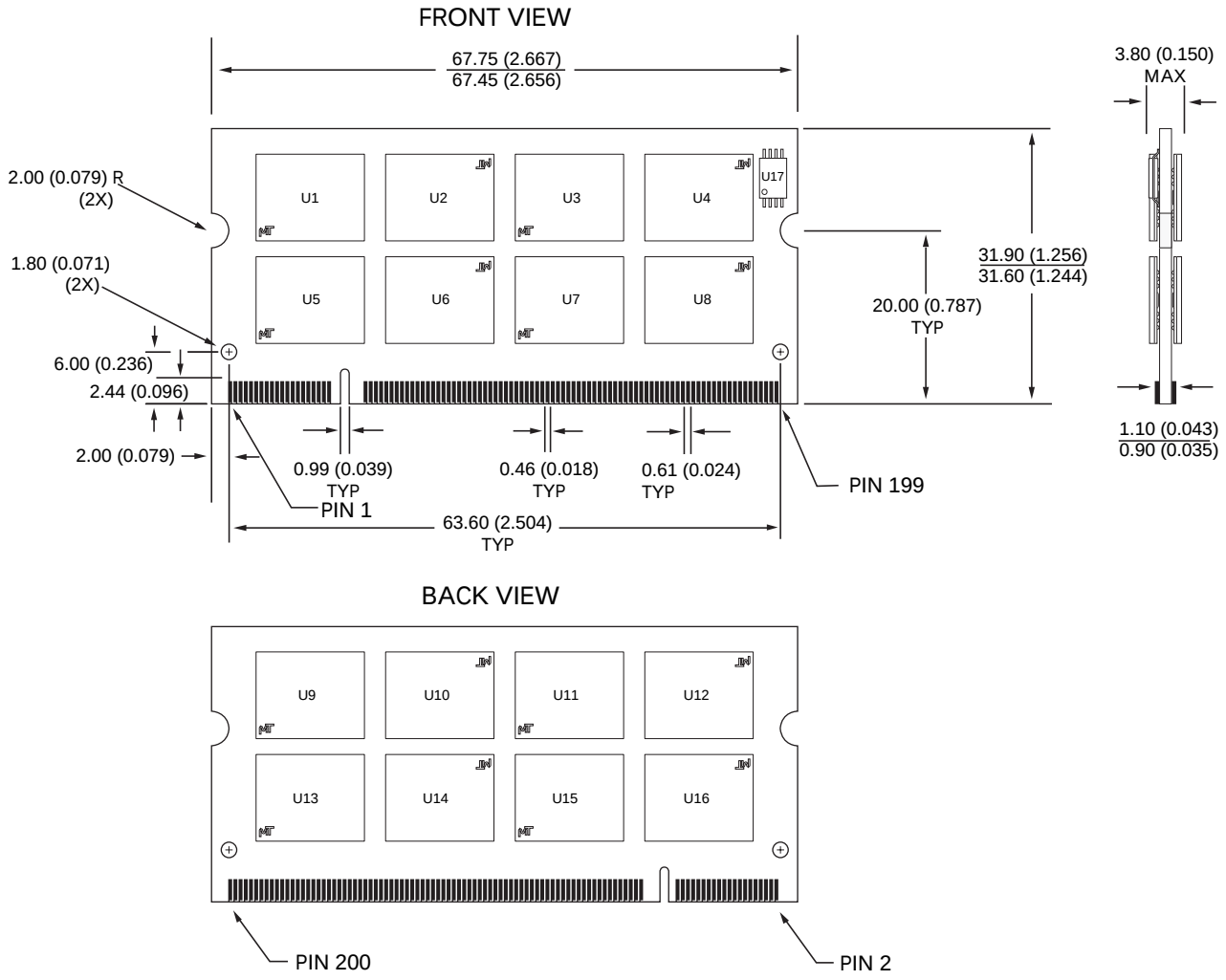
Module Dimensions

Figure 4: 200-Pin SODIMM Dimensions – 512MB



Notes: 1. All dimensions are in millimeters (inches) MIN/MAX or typical where noted.

Figure 5: 200-Pin SODIMM Dimensions – 1GB



Notes: 1. All dimensions are in millimeters (inches) MIN/MAX or typical where noted.

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