DDR2 SDRAM FBDIMM

MT18HTF6472F – 512MB
MT18HTF12872F – 1GB
MT18HTF25672F – 2GB

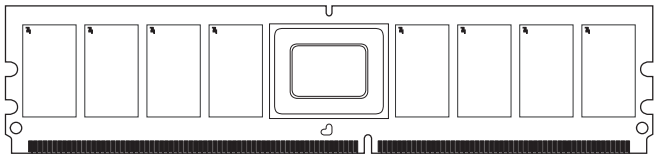
‡JEDEC has not yet adopted and published a final FBDIMM standard.
For the latest data sheets and technical notes, please refer to the Micron Web site: www.micron.com

Features

- 240-pin DDR2 fully buffered, dual in-line memory module (FBDIMM) with ECC to detect and report channel errors to the host memory controller
- Fast data transfer rates: PC2-4200 and PC2-5300, using 533 MT/s and 667 MT/s DDR2 SDRAM components
- 3.2 Gb/s and 4.0 Gb/s link transfer rates
- High-speed differential point-to-point link between host memory controller and the AMB using serial, dual-simplex bit lanes
  - 10-pair southbound (data path to FBDIMM)
  - 14-pair northbound (data path from FBDIMM)
- Fault tolerant; can work around a bad bit lane in each direction
- High density scaling with up to 8 dual-rank modules (288 DDR2 SDRAM devices) per channel
- SMBus interface to AMB for configuration register access
- In-band and out-of-band command access
- Deterministic protocol
  - Enables memory controller to optimize DRAM accesses for maximum performance
  - Delivers precise control and repeatable memory behavior
- Automatic DDR2 SDRAM bus and channel calibration
- Transmitter de-emphasis to reduce ISI
- MBIST and IBIST test functions
- Transparent mode for DDR2 SDRAM test support
- V_{DD} = $V_{DD}Q$ = +1.8V for DDR2 SDRAM
- V_{REF} = 0 .9V SDRAM C/A termination
- V_{CC} = 1.5V for advanced memory buffer (AMB)
- V_{DDSPD} = +1.7V to +3.6V for SPD EEPROM
- Serial presence detect (SPD) with EEPROM
- Gold edge contacts
- Single rank

Figure 1: 240-Pin FBDIMM (MO-256 R/C C)

PCB Height 30.35mm (1.19 in.)



Options	Marking
• Package	
240-pin FBDIMM (lead-free)	Y
• Frequency/CAS Latency[1]	
3.75ns @ CL = 5(DDR2-667)	-667
3.75ns @ CL = 4 (DDR2-533)	-53E
• PCB Height	
30.35mm (1.19 in.)	

Notes: 1. CL = CAS (READ) latency.

Table 1: FBDIMM / DDR2 SDRAM Addressing

Parameter	512MB	1GB	2GB
Refresh Count	8K	8K	8K
Device Bank Addressing	4 (BA0, BA1)	4 (BA0, BA1)	8 (BA0, BA1, BA2)
Device Page Size per Bank	1KB	1KB	1KB
Device Configuration	256Mb (64 Meg x 4)	512Mb (128 Meg x 4)	1Gb (256 Meg x 4)
Row Addressing	8K (A0–A12)	16K (A0–A13)	16K (A0–A13)
Column Addressing	2K (A0-A9, A11)	2K (A0-A9, A11)	2K (A0-A9, A11)
Module Rank Addressing	1 (S0#)	1 (S0#)	1 (S0#)

Table 2: Performance Parameters

Speed Grade	Module Bandwidth	Peak Channel Throughput	Link Transfer Rate	Latency (CL-^{t}RCD-^{t}RP)
-667	PC2-5300	8.0 GB/s	4.0 GT/s	5-5-5
-53E	PC2-4200	6.4 GB/s	3.2 GT/s	4-4-4

Table 3: Part Numbers and Label Markings

Part Number[1]	Module Density	FBDIMM Configuration	Label Key Attributes
MT18HTF6472FY-53E__	512MB	64 Meg x 72	512MB 1Rx4 PC2-4200F-444-10-C_
MT18HTF6472FY-667__	512MB	64 Meg x 72	512MB 1Rx4 PC2-5300F-555-10-C_
MT18HTF12872FY-53E__	1GB	128 Meg x 72	1GB 1Rx4 PC2-4200F-444-10-C_
MT18HTF12872FY-667__	1GB	128 Meg x 72	1GB 1Rx4 PC2-5300F-555-10-C_
MT18HTF25672FY-53E__	2GB	256 Meg x 72	2GB 1Rx4 PC2-4200F-444-10-C_
MT18HTF25672FY-667__	2GB	256 Meg x 72	2GB 1Rx4 PC2-5300F-555-10-C_

NOTE:

1. All part numbers end with a two-place code (not shown), designating component and PCB revisions. Consult factory for current revision codes. Example: MT18HTF12872FY-53EC2.

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Introduction

FBDIMM Specification Details

The entire FBDIMM specification currently in development by JEDEC members consists of the following sections and can be found at the JEDEC website member's area. JEDEC has not yet adopted and published a final FBDIMM standard. Please contact Micron for more detailed information.

Each of these sections contain detailed specification information for the various aspects of an FBDIMM's construction as well as its interfaces and theory of operation. Because the entire specification is simply too long and complex to condense into a single datasheet, minimal references are made throughout this document to give a brief overview. For design guidance and final specification information, designers must refer to the JEDEC FBDIMM specification in progress.

1. **FBDIMM Design Specification**

   This section defines the electrical and mechanical requirements for 240-pin, PC2-4200/PC2-5300/PC2-6400, 72 bit-wide, Fully Buffered Double Data Rate Synchronous DRAM Dual In-Line Memory Modules (DDR2 SDRAM FBDIMMs). These DDR2 SDRAM FBDIMMs are intended for use as main memory when installed in systems such as servers and workstations. PC2-4200/PC2-5300/PC2-6400 refers to the DIMM naming convention in which PC2-4200/PC2-5300/PC2-6400 indicates a 240-pin DDR2 DIMM running at 266/333/400 MHz DDR2 SDRAM clock speed and offering 4.2/5.3/6.4 GB/s bandwidth.

   Reference design examples are included which provide an initial basis for FBDIMM designs. Modifications to these reference designs may be required to meet all system timing, signal integrity, and thermal requirements for PC2-4200/PC2-5300/PC2-6400 support. All FBDIMM implementations must use simulations and lab verification to ensure proper timing requirements and signal integrity in the design.

2. **FBDIMM Architecture and Protocol Specification**

   This section describes the FBD Channel topology, physical signaling, clocking and data flow.

3. **FBDIMM AMB Specification**

   This section is a core specification for a Fully Buffered DIMM (FBDIMM) memory system. This document, along with the other core specifications, must be treated as a whole. Information critical to an AMB design appears in the other specifications, with specific cross-references provided.

4. **FBDIMM Link Signaling Specification**

   This section defines the high-speed differential point-to-point signaling link for FBDIMM, operating at the buffer supply voltage of 1.5V that is provided at the FBDIMM connector. This specification also applies to FBDIMM host chips which may operate with a different supply voltage. The link consists of a transmitter and a receiver and the interconnect in between them. The transmitter sends serialized bits into a lane and the receiver accepts the electrical signals of the serialized bits and transforms them into a serialized bit-stream. The first generation FBDIMM link is being specified to operate from 3.2 to 4.8 Gb/s. The specifications are defined for three distinct bit rates of operation: 3.2 Gb/s, 4.0 Gb/s and 4.8 Gb/s.

   The link utilizes a derived clock approach and transmitter de-emphasis to compensate for channel loss characteristics. The link definition has the flexibility to accommodate future silicon enhancement circuits such as forwarded clocking or advanced equalization techniques to meet future signaling targets.

5. **FBDIMM DFx Specification**

   This section covers Design for Test, Design for Manufacturing and Design for Validation ("DFx") requirements and implementation guidelines for FBDIMM technology.

6. **FBDIMM DIMM Design Specification**

   This section defines the electrical and mechanical requirements for 240-pin, PC2-4200/PC2-5300/PC2-6400, 72 bit-wide, DDR2 SDRAM FBDIMMs. FBDIMMs are intended for use as main memory when installed in systems such as servers and workstations. PC2-4200/PC2-5300/PC2-6400 refers to the FBDIMM naming convention in which PC2-4200/PC2-5300/PC2-6400 indicates a 240-pin DDR2 FBDIMM running at 266/333/400 MHz DDR2 SDRAM clock speed and offering 4.2/5.3/6.4 GB/s bandwidth.

   Reference design examples are included which provide an initial basis for FBDIMM designs. Modifications to these reference designs may be required to meet all system timing, signal integrity, and thermal requirements for PC2-4200/PC2-5300/PC2-6400 support. All FBDIMM implementations must use simulations and lab verification to ensure proper timing requirements and signal integrity in the design.

7. **FBDIMM SPD Specification**

   This section describes the serial presence detect (SPD) values for FBDIMMs. These presence detects are those referenced in the SPD standard document for 'Specific Features'. The SPD fields indicated in this specification will occur in the order presented in section 1.1. *(Note that the descriptions of Bytes 0 and 1 are different from those found in previous SPD standards.)* Further description of Byte 2 is found in Appendix A of the FBDIMM SPD standard. All unused entries wiil be coded as 0x00. All unused bits in defined bytes will be coded as 0 except where noted.

General Description

The Micron® fully buffered DIMM (FBDIMM) adheres to the currently proposed industry specifications for FBDIMMs. This ADVANCE datasheet represents a minimal subset of the FBDIMM and advanced memory buffer (AMB) specification details and will be revised further as the specification matures and is approved and released. Under all circumstances, this document is to be used only as an introduction to the industry specification which will serve as the final reference for any an all design parameters and criteria.

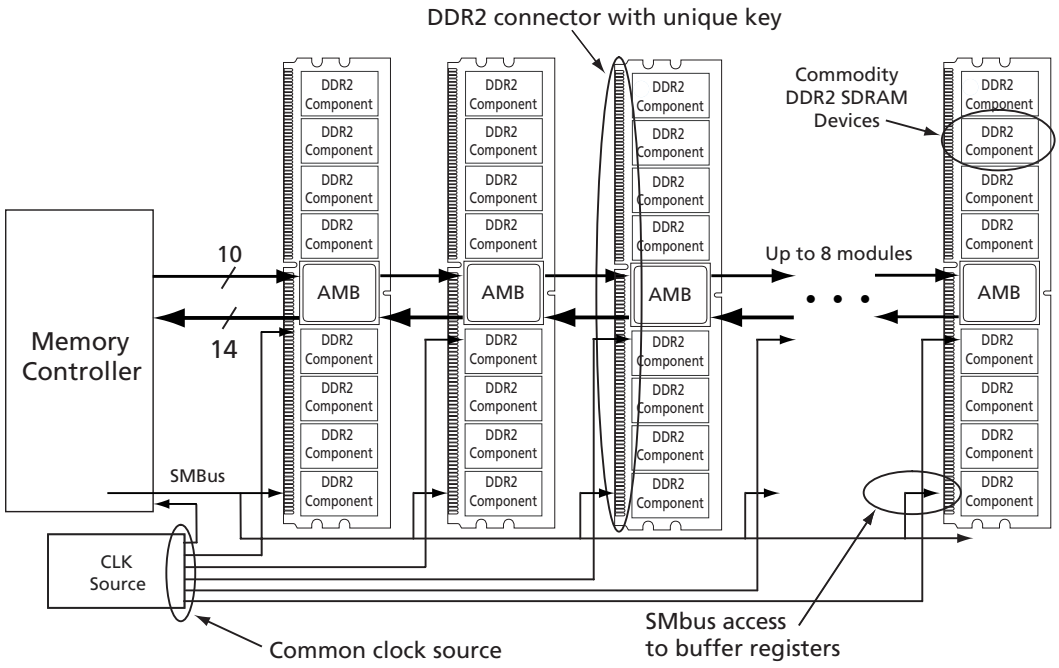
Micron's FBDIMM is a high-bandwidth, large-capacity-channel solution that has a narrow host interface. FBDIMMs use DDR2 SDRAM devices isolated from the channel behind a buffer on the FBDIMM. Memory device capacity remains high and total memory capacity scales with DDR2 SDRAM bit density.

As shown in Figure 2 on page 8, the FBDIMM channel provides a communication path from a host controller to an array of DDR2 SDRAM devices, with the DDR2 SDRAM devices buffered behind an AMB device. The physical isolation of the DDR2 SDRAM devices from the channel enables the flexibility to enhance the communication path to significantly increase the reliability and availability of the memory subsystem.

Micron's FBDIMM features a novel architecture, including the AMB that isolates the DDR2 SDRAMs from the channel. This single-chip component located in the center of each FBDIMM acts as a repeater and buffer for all signals and commands exchanged between the host controller and the DDR2 SDRAM devices, including data input and output. The AMB communicates with the host controller and adjacent FBDIMMs on a system board using an industry-standard, high-speed, differential point-to-point interface at 1.5 V.

The AMB also allows buffering of memory traffic to support large memory capacities. All memory control for the DDR2 SDRAM devices resides in the host, including memory request initiation, timing, refresh, scrubbing, sparing, configuration access, and power management. The AMB interface is responsible for handling channel and memory requests to and from the local FBDIMM and for forwarding requests to other FBDIMMs on the memory channel.

Figure 2: FBDIMM Solution Block Diagram



Functional Description

Advanced Memory Buffer (AMB)

The AMB reference design complies with the "FBDIMM Architecture and Protocol Specification" (JEDEC standard, pending). It is expected that there will be multiple vendors for the AMB which will offer at least the minimum functionality as set forth in the industry specification. To achieve optimal operation and compatibility with DDR2 SDRAM device and host/controller offerings, each vendor's AMB will have a unique set of personality bytes contained in the SPD for setting up and fine tuning their device.

The FBDIMM specification defines a number of options to support the requirements of different applications. The capabilities of the AMB are communicated to the host during the initialization process in the TS2 training pattern and in bits readable in the Features register in the AMB.

The AMB is responsible for handling FBD channel and memory requests to and from the local FBDIMM and for forwarding requests to other FBDIMMs on the channel. A complete and detailed description of the AMB is contained in the proposed FBDIMM AMB Specification. The AMB is a memory interface that connects an array of DDR2 SDRAM devices to the FBDIMM channel. The AMB is a slave device on the channel responding to channel commands directed to this AMB and forwarding channel commands to other FBDIMM's AMB devices on the channel.

All memory control for the DDR2 SDRAM resides in the host, including memory request initiation, timing, refresh, scrubbing, sparing, configuration access, and power management.

The AMB is expected to perform the following functions:

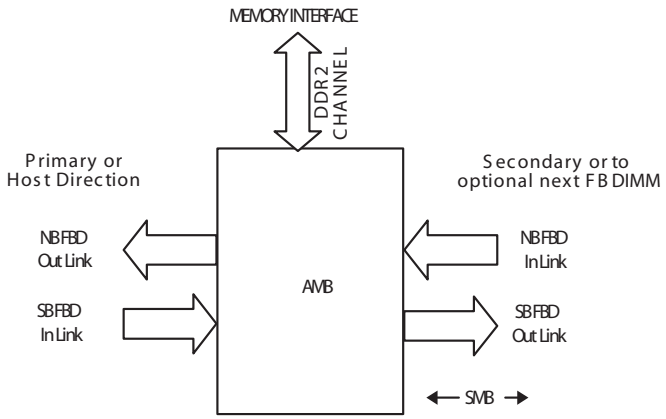
- Support channel initialization procedures as defined in the Initialization Chapter of the FBDIMM Architecture and Protocol Specification to align the clocks and the frame boundaries and verify channel connectivity
- Support the forwarding of southbound and northbound frames, servicing requests directed to a specific FBDIMM's AMB, as defined in the Protocol Chapter of the specification, and merging the return data into the northbound frames
- If the FBDIMM's AMB is the last, southern-most on the channel, initialize northbound frames
- Detect errors on the channel and report them to the host memory controller
- Support the FBD configuration register set as defined in the FBD AMB Specification Register Chapter of the specification
- Act as a DRAM memory buffer for all read, write, and configuration accesses addressed to a specific FBDIMM's AMB
- Provide a read and write buffer FIFO
- Supports an SMBus protocol interface for access to the AMB configuration registers
- Provide features to support MEMBIST and IBIST Test functions
- Provide a register interface for the thermal sensor and status indicator
- Function as a repeater to extend the maximum length of FBDIMM Links
- Reconfigures FBDIMM inputs from differential high speed link receivers to two single ended lower speed receivers (~200 MHz) These inputs directly control DDR2 Command/Address and input data that is replicated to all DDR2 SDRAMs
- Uses low speed FBDIMM outputs to bypass high speed Parallel/Serial circuitry and provide test results back to the tester

AMB Interface

Figure 3, AMB Interface Block Diagram illustrates the AMB and all of its interfaces. They consist of two FBDIMM links, one DDR2 channel and an SMBus interface. Each FBDIMM link connects the AMB to a host memory controller or an adjacent FBDIMM. The DDR2 channel supports direct connection to the DDR2 SDRAMs on an FBDIMM.

The FBDIMM channel uses a daisy-chain topology to provide expansion from a single FBDIMM per channel to up to eight FBDIMMs per channel. The host sends data on the southbound link to the first FBDIMM, where it is received and redriven to the second FBDIMM. On the southbound data path each FBDIMM receives the data and redrives the data to the next FBDIMM, until the last FBDIMM receives the data. The last FBDIMM in the chain initiates the transmission of northbound data in the direction of the host. On the northbound data path, each FBDIMM receives the data and redrives the data to the next FBDIMM until the host is reached.

Figure 3: AMB Interface Block Diagram



High-Speed Differential Point-to-Point Link (at 1.5 V) Interfaces

The AMB supports one FBDIMM channel consisting of two bidirectional link interfaces using highspeed differential point-to-point electrical signaling. The southbound input link is 10 lanes wide and carries commands and write data from the host memory controller or the adjacent FBDIMM in the host direction. The southbound output link forwards this same data to the next FBDIMM.

The northbound input link is 14 lanes wide and carries read return data or status information from the next FBDIMM in the chain back towards the host. The northbound output link forwards this information back towards the host and multiplexes in any read return data or status information that is generated internally.

Data and commands sent to the DDR2 SDRAMs travel southbound on 10 primary differential signal line pairs. Data received from the DDR2 SDRAMs and status information travel northbound on 14 primary differential pairs. Data and commands sent to the adjacent FBDIMM upstream are repeated and travel further southbound on 10 secondary differential pairs. Data and status information received from the adjacent FBDIMM upstream travel further northbound on 14 secondary differential pairs.

DDR2 Channel

The DDR2 channel on the advanced memory buffer supports direct connection to DDR2 SDRAM devices. The DDR2 channel supports two ranks of eight banks with 16 row/column-request, 64 data, and eight check-bit signals. There are two copies of address and command signals to support FBDIMM routing and electrical requirements. Four transfer bursts are driven on the data and check-bit lines at 800 MHz.

Propagation delays between read data/check-bit strobe lanes on a given channel can differ. Each strobe can be calibrated by hardware state machines using WRITE/READ trial and error. Hardware aligns the read data and check-bits to a single core clock. The AMB provides four copies of the command clock phase references (CLK[3:0]) and write data/check-bit strobes (DQSs) for each DDR2 SDRAM device nibble.

SMBus Slave Interface

The AMB supports an SMBus interface to allow system access to configuration registers independent of the FBDIMM link. The AMB will never be a master on the SMBus, only a slave. Serial SMBus data transfer is supported at 100 kHz. SMBus access to the AMB may be a requirement to boot and to set link strength, frequency and other parameters needed to insure robust configurations. It is also required for diagnostic support when the high speed link is down. The SMBus address straps located on the FBDIMM connector are used to set the unique ID.

Channel Latency

FBDIMM channel latency is measured from the time a read request is driven on the FBDIMM channel pins to the time when the first 16 bytes (2nd chunk) of read completion data is sampled by the memory controller.

When not using the variable read latency capability, the latency for a specific FBDIMM on a channel is always equal to the latency for any other FBDIMM on that channel. However, the latency for each FBDIMM in a specific configuration with some number of FBDIMMs installed may not be equal to the latency for each FBDIMM in a configuration with some different number of FBDIMMs installed. As more FBDIMMs are added to the channel, additional latency is required to read from each FBDIMM on the channel.

Because the channel is based on the point-to-point interconnection of buffer components between FBDIMMs, memory requests are required to travel through N - 1 buffers before reaching the Nth buffer. The result is that a four FBDIMM channel configuration will have greater idle read latency compared to a one FBDIMM channel configuration.

The variable read latency capability can be used to reduce latency for FBDIMMs closer to the host. The idle latencies listed in this section are representative of what might be achieved in typical AMB designs. Actual implementations with latencies less than the values isted will have higher application performance and vice versa.

Peak Theoretical Throughput

An FBDIMM channel transfers read completion data on the northbound data connection; 144 bits of data are transferred for every northbound data frame. This matches the 18-byte data transfer of an ECC DDR2 DRAM device in a single DDR2 SDRAM command clock. A DDR2 SDRAM device burst of eight from a single channel, or burst of four from two lockstepped channels, provides a total of 72 bytes of data (64 bytes plus 8 bytes ECC). The AMB frame rate matches the DDR2 SDRAM command clock because of the fixed 6:1 ratio of the FBDIMM channel clock to the DDR2 SDRAM command clock. Therefore, the northbound data connection will exhibit the same peak theoretical

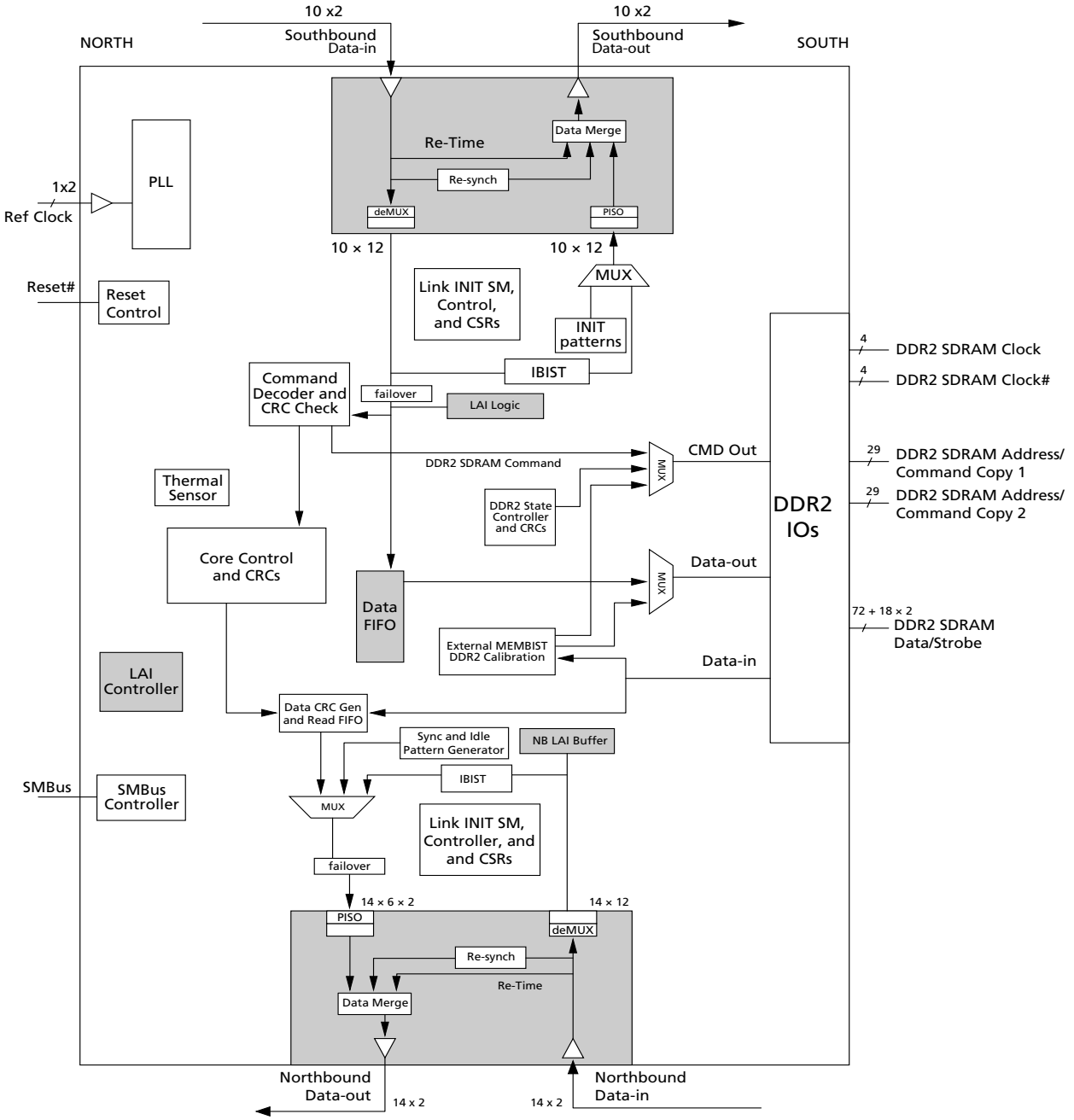
throughput as a single DDR2 SDRAM channel. For example, when using DDR2 533 SDRAMs, the peak theoretical bandwidth of the northbound data connection is 4.267 GB/sec.

Write data is transferred on the southbound command and data connection, via Command+Wdata frames. 72 bits of data are transferred for every FBDIMM Command+Wdata frame. Two Command+Wdata frames match the 18-byte data transfer of an ECC DDR2 SDRAM in a single DDR2 SDRAM command clock.

A DDR2 SDRAM burst of eight transfers from a single channel, or a burst of four from two lock-step channels, provides a total of 72 bytes of data (64 bytes plus 8 bytes ECC). When the FBDIMM frame rate matches the DDR2 SDRAM command clock, the southbound command and data connection will exhibit one half the peak theoretical throughput of a single DDR2 SDRAM channel. For example, when using DDR2 533 SDRAMs, the peak theoretical bandwidth of the southbound command and data connection is 2.133 GB/sec.

The total peak-theoretical throughput for a single FBDIMM channel is defined as the sum of the peak-theoretical throughput of the northbound data connection and the southbound command and data connection. When the FBDIMM frame rate matches the DDR2 SDRAM command clock, this is equal to 1.5 times the peak-theoretical throughput of a single DDR2 SDRAM channel. For example, when using DDR2 533 SDRAMs, the peak theoretical throughput of a DDR2 533 channel would be 4.267 GB/sec, while the peak theoretical throughput of an FBDIMM-533 channel would be 6.4 GB/sec.

Figure 4: AMB Functional Block Diagram



Hot-add

The FBDIMM channel does not provide a mechanism to automatically detect and report the addition of a new FBDIMM south of the currently active last FBDIMM. It is assumed the system will be notified through some means of the addition of one or more new FBDIMMs so that specific commands can be sent to the host controller to initialize the newly added FBDIMM(s) and perform a hot-add reset to bring them into the channel

timing domain. It should be noted that the power to the FBDIMM socket must be removed before a hot-add FBDIMM is inserted or removed. Applying or removing the power to a FBDIMM socket is a system platform function.

Hot-remove

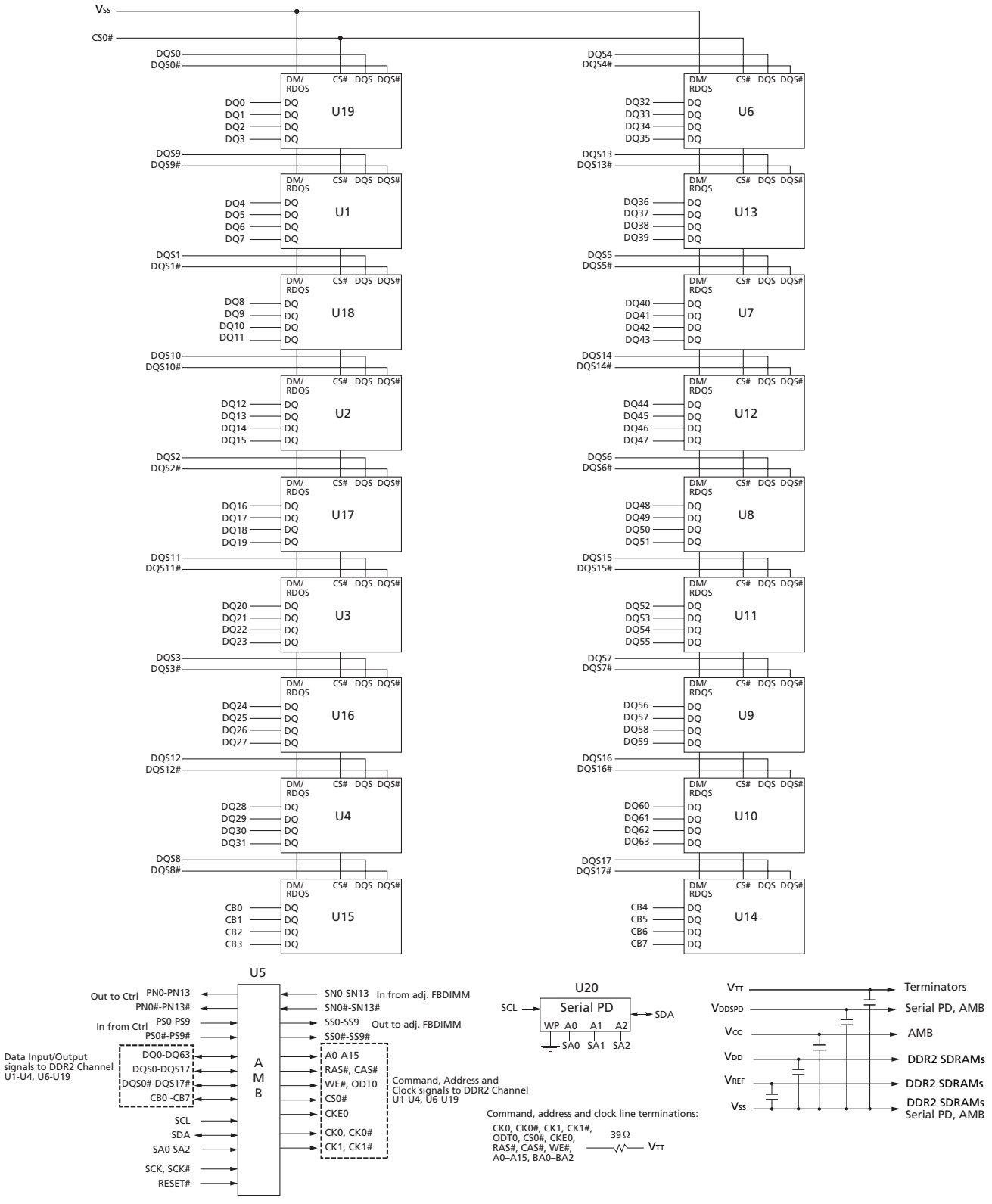
In order to accomplish removal of FBDIMMs, the host must perform a fast reset sequence targeted at the last FBDIMM that will be retained on the channel. The fast reset re-establishes the appropriate last FBDIMM so that the southbound transmission outputs of the last active FBDIMM and the southbound and northbound outputs of the FBDIMMs beyond the last active FBDIMM are disabled. Once the appropriate outputs are disabled, the system can coordinate the procedure to remove power in preparation for physical removal of the FBDIMM if needed. Note that the power to the FBDIMM socket must be removed before a hot-add FBDIMM is inserted or removed. Applying or removing the power to a FBDIMM socket is a system platform function.

Hot-replace

Hot replace of FBDIMM is accomplished through combining the hot-remove and hot-add processes.

FBDIMM Functional Block

Figure 5: FBDIMM Functional Block Diagram



Pin Assignments and Descriptions

Table 4: 240-pin FBDIMM Pin Assignment

Pin	Front	Pin	Back	Pin	Front	Pin	Back	Pin	Front	Pin	Back	Pin	Front	Pin	Back
1	VDD	121	VDD	31	PN3	151	SN3	61	PN9#	181	SN9#	91	PS9#	211	SS9#
2	VDD	122	VDD	32	PN3#	152	SN3#	62	VSS	182	VSS	92	VSS	212	VSS
3	VDD	123	VDD	33	VSS	153	VSS	63	PN10	183	SN10	93	PS5	213	SS5
4	VSS	124	VSS	34	PN4	154	SN4	64	PN10#	184	SN10#	94	PS5#	214	SS5#
5	VDD	125	VDD	35	PN4#	155	SN4#	65	VSS	185	VSS	95	VSS	215	VSS
6	VDD	126	VDD	36	VSS	156	VSS	66	PN11	186	SN11#	96	PS6	216	SS6
7	VDD	127	VDD	37	PN5	157	SN5	67	PN11#	187	SN11#	97	PS6#	217	SS6#
8	VSS	128	VSS	38	PN5#	158	SN5#	68	VSS	188	VSS	98	VSS	218	VSS
9	VCC	129	VCC	39	VSS	159	VSS	69	VSS	189	VSS	99	PS7	219	SS7
10	VCC	130	VCC	40	PN13	160	SN13	70	PS0	190	SS0	100	PS7#	220	SS7#
11	VSS	131	VSS	41	PN13#	161	SN13#	71	PS0#	191	SS0#	101	VSS	221	VSS
12	VCC	132	VCC	42	VSS	162	VSS	72	VSS	192	VSS	102	PS8	222	SS8
13	VCC	133	VCC	43	VSS	163	VSS	73	PS1	193	SS1	103	PS8#	223	SS8#
14	VSS	134	VSS	44	RFU	164	RFU[1]	74	PS1#	194	SS1#	104	VSS	224	VSS
15	VTT	135	VTT	45	RFU	165	RFU[1]	75	VSS	195	VSS	105	RFU[2]	225	RFU[2]
16	VID1	136	VID0	46	VSS	166	VSS	76	PS2	196	SS2	106	RFU[2]	226	RFU[2]
17	RESET#	137	DNU/M_TEST	47	VSS	167	VSS	77	PS2#	197	SS2#	107	VSS	227	VSS
18	VSS	138	VSS	48	PN12	168	SN12	78	VSS	198	VSS	108	VDD	228	SCK
19	RFU[2]	139	RFU[2]	49	PN12#	169	SN12#	79	PS3	199	SS3	109	VDD	229	SCK#
20	RFU[2]	140	RFU[2]	50	VSS	170	VSS	80	PS3#	200	SS3#	110	VSS	230	VSS
21	VSS	141	VSS	51	PN6	171	SN6	81	VSS	201	VSS	111	VDD	231	VDD
22	PN0	142	SN0	52	PN6#	172	SN6#	82	PS4	202	SS4	112	VDD	232	VDD
23	PN0#	143	SN0#	53	VSS	173	VSS	83	PS4#	203	SS4#	113	VDD	233	VDD
24	VSS	144	VSS	54	PN7	174	SN7	84	VSS	204	VSS	114	VSS	234	VSS
25	PN1	145	SN1	55	PN7#	175	SN7#	85	VSS	205	VSS	115	VDD	235	VDD
26	PN1#	146	SN1#	56	VSS	176	VSS	86	RFU[1]	206	RFU[1]	116	VDD	236	VDD
27	VSS	147	VSS	57	PN8	177	SN8	87	RFU[1]	207	RFU[1]	117	VTT	237	VTT
28	PN2	148	SN2	58	PN8#	178	SN8#	88	VSS	208	VSS	118	SA2	238	VDDSPD
29	PN2#	149	SN2#	59	VSS	179	VSS	89	VSS	209	VSS	119	SDA	239	SA0
30	VSS	150	VSS	60	PN9	180	SN9	90	PS9	210	SS9	120	SCL	240	SA1

Notes: 1. These pin positions are reserved for forwarded clocks to be used in future module implementations
2. These pin positions are reserved for future architecture flexibility
3. The following signals are CRC bits and thus appear out of the normal sequence: PN12/PN12#, SN12/SN12#, PN13/PN13#, SN13/SN13#, PS9/PS9#, SS9/SS9#
4. RFU = Reserved Future Use.

Figure 6: FBDIMM Pin Locations

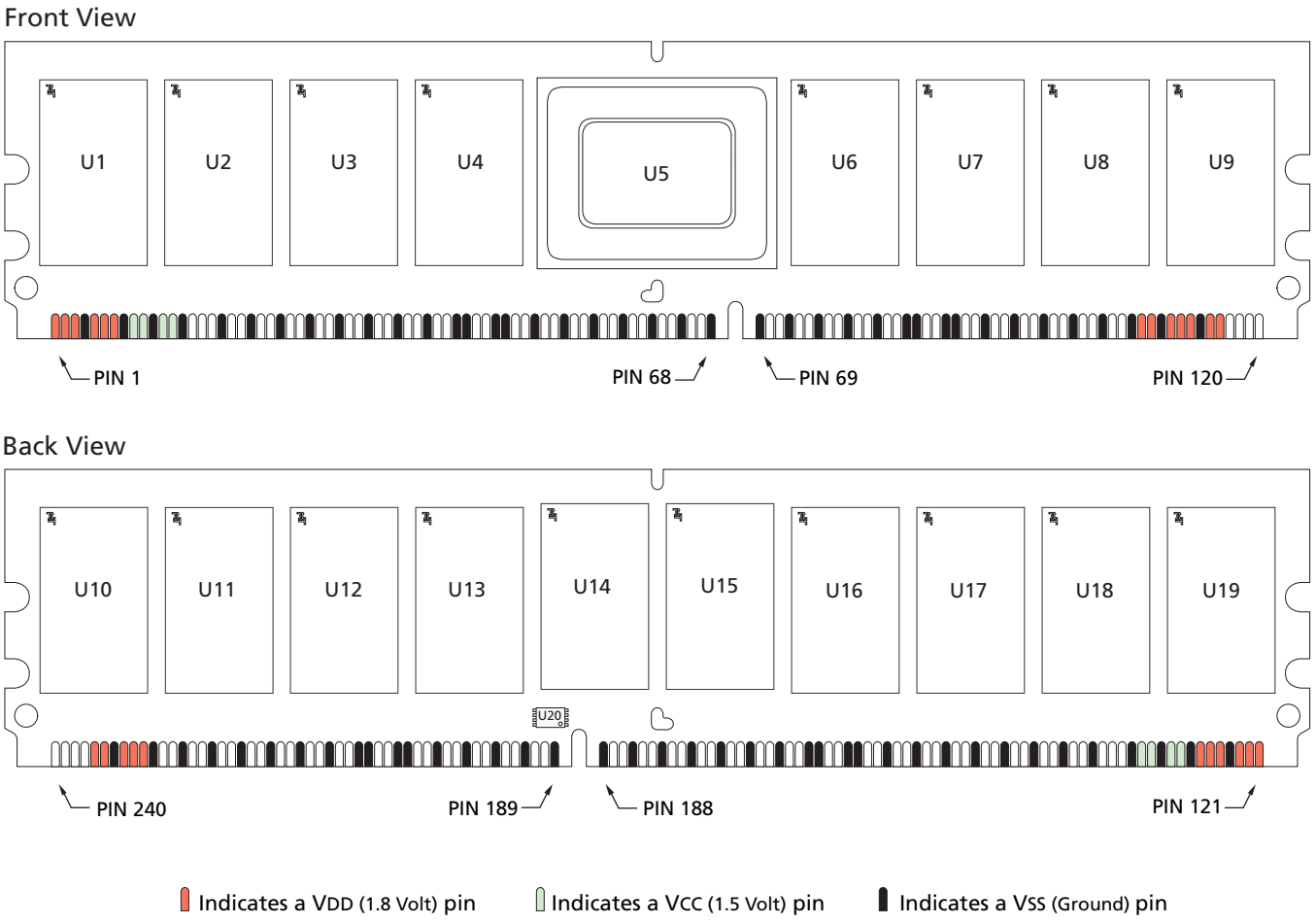


Table 5: Pin Descriptions

Pin Numbers	Symbol	Type	Description
228	SCK	Input	System clock input, positive line
229	SCK#	Input	System clock Input, negative line
22, 25, 28, 31, 34, 37, 40, 48, 51, 54, 57, 60, 63, 66	PN[13:0]	Output	Primary northbound data, positive lines
23, 26, 29, 32, 35, 38, 41, 49, 52, 55, 58, 61, 64, 67	PN#[13:0]	Output	Primary northbound data, negative lines
70, 73, 76, 79, 82, 90, 93, 96, 99, 102	PS[9:0]	Input	Primary southbound data, positive lines
71, 74, 77, 80, 83, 91, 94, 97, 100, 103	PS#[9:0]	Input	Primary southbound data, negative lines
142, 145, 148, 151, 154, 157, 160, 168, 171, 174, 177, 180, 183, 186	SN[13:0]	Output	Secondary northbound data, positive lines
143, 146, 149, 152, 155, 158, 161, 169, 172, 175, 178, 181, 184, 187	SN#[13:0]	Output	Secondary northbound data, negative lines
190, 193, 196, 199, 202, 210, 213, 216, 219, 222	SS[9:0]	Input	Secondary southbound data, positive lines
191, 194, 197, 200, 203, 211, 214, 217, 220, 223	SS#[9:0]	Input	Secondary southbound data, negative lines

Table 5: Pin Descriptions

Pin Numbers	Symbol	Type	Description
120	SCL	Input	Serial presence detect (SPD) clock input
119	SDA	I/O	SPD data input / output
118, 239, 240	SA[2:0]	I/O	SPD address Inputs, also used to select the FBDIMM number in the AMB
16, 136	VID[1:0]	NC	Voltage ID: These pins must be unconnected for DDR2-based FBDIMMs. VID[0] is VDD value: OPEN = 1.8 V, GND = 1.5 V; VID[1] is VCC value: OPEN = 1.5 V, GND = 1.2 V
17	RESET#	Supply	AMB reset signal
9, 10, 12, 13, 129, 130, 132, 133	V_{CC}	Supply	AMB core power and AMB channel interface power (1.5 Volt)
1, 2, 3, 5, 6, 7, 108, 109, 111, 112, 113, 115, 116, 121, 122, 123, 125, 126, 127, 231, 232, 233, 235, 236	V_{DD}	Supply	DRAM power and AMB DRAM I/O power (1.8 Volt)
15, 117, 135, 237	V_{TT}	Supply	DRAM address/command/clock termination power (V_{DD}/2)
238	V_{DDSPD}	Supply	SPD power
4, 8, 11, 14, 18, 21, 24, 27, 30, 33, 36, 39, 42, 43, 46, 47, 50, 53, 56, 59, 62, 65, 68, 69, 72, 75, 78, 81, 84, 85, 88, 89, 92, 95, 98, 101, 104, 107, 110, 114, 124, 128, 131, 134, 138, 141, 144, 147, 150, 153, 156, 159, 162, 163, 166, 167, 170, 173, 176, 179, 182, 185, 188, 189, 192, 195, 198, 201, 204, 205, 208, 209, 212, 215, 218, 221, 224, 227, 230, 234	V_{SS}	Supply	Ground
19, 20, 44, 45, 86, 87, 105, 106, 139, 140, 164, 165, 206, 207, 225, 226	RFU	RFU	Reserved for future use
137	DNU/ M_Test	DNU	The DNU/M_Test pin provides an external connection on R/Cs A–D for testing the margin of V_{REF} which is produced by a voltage divider on the module. It is not intended to be used in normal system operation and must not be be connected (DNU) in a system. This test pin may have other features on future card designs and will be included in this specification at that time.

Absolute Maximum Ratings

Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may adversely affect reliability.

Table 6: Absolute Maximum Ratings

Symbol	Parameter	MIN	MAX	Units
V_{IN}, V_{OUT}	Voltage on any pin relative to V_{SS}	-0.3	1.75	V
V_{CC}	Voltage on V_{CC} pin relative to V_{SS}	-0.3	1.75	V
V_{DD}	Voltage V_{DD} pin relative to V_{SS}	-0.5	2.3	V
V_{TT}	Voltage on V_{TT} pin relative to V_{SS}	-0.5	2.3	V
T_{STG}	Storage temperature	-55	100	°C
T_{CASE}	DDR2 SDRAM device operating temperature (Ambient)	0	85	°C
	AMB device operating temperature (Ambient)	0	110	°C

Input Electrical Characteristics and Operating Conditions

Table 7: Input DC Voltage and Operating Conditions

Parameter	Symbol	MIN	Nom	MAX	Units	Notes
AMB supply voltage	V_{CC}	1.46	1.50	1.54	V	
DDR2 SDRAM supply voltage	V_{DD}	1.7	1.8	1.9	V	
Termination voltage	V_{TT}	0.48 x V_{DD}	0.50 x V_{DD}	0.52 x V_{DD}	V	
EEPROM supply voltage	V_{DDSPD}	3.0	3.3	3.6	V	
SPD Input HIGH (logic 1) voltage	$V_{IH(DC)}$	2.1		V_{DDSPD}	V	1
SPD Input LOW (logic 0) voltage	$V_{IL(DC)}$			0.8	V	1
RESET Input HIGH (logic 1) voltage	$V_{IH(DC)}$	1.0			V	2
RESET Input LOW (logic 0) voltage	$V_{IL(DC)}$			0.5	V	1
Leakage Current (RESET)	I_L	-90		90	µA	2
Leakage Current (link)	I_L	-5		5	µA	3

Notes: 1. Applies for SMB and SPD bus signals.
2. Applies for AMB CMOS signal RESET#.
3. For all other AMB related DC parameters, please refer to the high-speed differential link interface specification.

Table 8: Timing Parameters

Parameter	Symbol	MIN	Typ	MAX	Units	Notes
EI assertion pass-through timing	^{t}EI Propagate			4	CK	
EI deassertion pass-through timing	^{t}EID			Bitlock	CK	2
EI assertion duration	^{t}EI	100			CK	1, 2
FBD command to DDR@ clock out that latches command			8.1		ns	3
FBD command to DDR2 WRITE			TBD		ns	
DDR2 READ to FBD (last FBDIMM)			5.0		ns	4
Resample pass-through time			1.075		ns	
Resynch pass-through time			2.075		ns	
Bitlock interval	^{t}Bitlock			119	frames	1
Framelock interval	^{t}Framelock			154	frames	1

Notes:
1. Defined in FBDIMM architecture and protocol specification.
2. Clocks defined as core closks - 2x SCK input.
3. For DDR2-667 (PC2-5300), this is measured from the beginnning of the frame at the south-bound input to the DDR2 clock output that latches the first command of a frame to the DDR2 SDRAM devices.
4. For DDR2-667 (PC2-5300), this is measured from the latest DQS input to the AMB to the start of the matching data frame at the northbound FBDIMM outputs.

IDD Specifications and Conditions

Assumptions for all Parameters:

Primary channel Drive strength at 100 percent with de-emphasis at -6.5dB, secondary channel drive strength at 60 percent with de-emphasis at -3dB when enabled.

Address and data fields are pseudo-random, which provides a 50 percent toggle rate on DDR2 SDRAM data lines and link lanes when data is being transferred.

Assuming 1 ACTIVATE command and 1 READ/WRITE command per BL = 4 transfer, BL = 4.

Ten southbound lanes and 14 northbound lanes are enabled and active.

SPD-specific assumptions:

- Number of devices on the specific FBDIMM assumed
- Termination of command, address, and control is actual value used on the FBDIMM
- ECC as per the specific FBDIMM
- SPD specifies Delta T

AMB power spec specific assumptions:

- Specific ECC FBDIMM assumed (72 bit data, 14 lanes northbound with DDR2 SDRAMs as defined in configuration options of this datasheet)
- Modeled with 27Ω termination for command, address, and clocks, and 47Ω termination for control
- AMB specification specifies current for each rail

Table 9: DDR2 IDD Specifications and Conditions – 512MB

Parameter/Condition	Symbol	-667	-53E	Units
Idle current, single or last FBDIMM: L0 state, idle (0 BW); primary channel enabled, secondary channel disabled, CKE high; command and address lines stable, DDR2 SDRAM clock active.	IDD_IDLE_0	TBD	TBD	mA
Idle current, first FBDIMM: L0 state, idle (0 BW); primary and secondary channels enabled, CKE high; command and address lines stable, DDR2 SDRAM clock active.	IDD_IDLE_1	TBD	TBD	mA
Idle current, DDR2 SDRAM power down: L0 state, idle (0 BW); primary and secondary channels enabled, CKE high; command and address lines floated, DDR2 SDRAM clock active; ODT and CKE driven LOW.	IDD_IDLE_2	TBD	TBD	mA
Active Power: L0 state; 50% DDR2 SDRAM BW, 67% READ, 33% WRITE; primary and secondary channels enabled, CKE high; DDR2 SDRAM clock active.	IDD_ACTIVE_1	TBD	TBD	mA
Active Power, data pass through: L0 state; 50% DDR2 SDRAM BW to downstream FBDIMM, 67% READ, 33% WRITE; primary and secondary channels enabled; command and address lines stable, CKE high; DDR2 SDRAM clock active.	IDD_ACTIVE_2	TBD	TBD	mA
Channel standby: Average power over 42 frames where the channel enters and exits L0s; DDR2 SDRAM devices Idle (0 BW); CKE LOW; command and address lines floated; DDR2 SDRAM lock active, ODE and CKE driven LOW.	IDD_L0s	TBD	TBD	mA
Training: Primary and secondary channels enabled; 100% toggle on all channel lanes; DDR2 SDRAM devices idle (0 BW); CKE HIGH, command and address lines stable; DDR2 SDRAM clock active.	IDD_TRAINING	TBD	TBD	mA

Table 10: DDR2 IDD Specifications and Conditions – 1GB

Parameter/Condition	Symbol	-667	-53E	Units
Idle current, single or last FBDIMM: L0 state, idle (0 BW); primary channel enabled, secondary channel disabled, CKE high; command and address lines stable, DDR2 SDRAM clock active.	IDD_IDLE_0	TBD	TBD	mA
Idle current, first FBDIMM: L0 state, idle (0 BW); primary and secondary channels enabled, CKE high; command and address lines stable, DDR2 SDRAM clock active.	IDD_IDLE_1	TBD	TBD	mA
Idle current, DDR2 SDRAM power down: L0 state, idle (0 BW); primary and secondary channels enabled, CKE high; command and address lines floated, DDR2 SDRAM clock active; ODT and CKE driven LOW.	IDD_IDLE_2	TBD	TBD	mA
Active Power: L0 state; 50% DDR2 SDRAM BW, 67% READ, 33% WRITE; primary and secondary channels enabled, CKE high; DDR2 SDRAM clock active.	IDD_ACTIVE_1	TBD	TBD	mA
Active Power, data pass through: L0 state; 50% DDR2 SDRAM BW to downstream FBDIMM, 67% READ, 33% WRITE; primary and secondary channels enabled; command and address lines stable, CKE high; DDR2 SDRAM clock active.	IDD_ACTIVE_2	TBD	TBD	mA
Channel standby: Average power over 42 frames where the channel enters and exits L0s; DDR2 SDRAM devices Idle (0 BW); CKE LOW; command and address lines floated; DDR2 SDRAM lock active, ODE and CKE driven LOW.	IDD_LOS	TBD	TBD	mA
Training: Primary and secondary channels enabled; 100% toggle on all channel lanes; DDR2 SDRAM devices idle (0 BW); CKE HIGH, command and address lines stable; DDR2 SDRAM clock active.	IDD_TRAINING	TBD	TBD	mA

Table 11: DDR2 IDD Specifications and Conditions – 2GB

Parameter/Condition	Symbol	-667	-53E	Units
Idle current, single or last FBDIMM: L0 state, idle (0 BW); primary channel enabled, secondary channel disabled, CKE high; command and address lines stable, DDR2 SDRAM clock active.	IDD_IDLE_0	TBD	TBD	mA
Idle current, first FBDIMM: L0 state, idle (0 BW); primary and secondary channels enabled, CKE high; command and address lines stable, DDR2 SDRAM clock active.	IDD_IDLE_1	TBD	TBD	mA
Idle current, DDR2 SDRAM power down: L0 state, idle (0 BW); primary and secondary channels enabled, CKE high; command and address lines floated, DDR2 SDRAM clock active; ODT and CKE driven LOW.	IDD_IDLE_2	TBD	TBD	mA
Active Power: L0 state; 50% DDR2 SDRAM BW, 67% READ, 33% WRITE; primary and secondary channels enabled, CKE high; DDR2 SDRAM clock active.	IDD_ACTIVE_1	TBD	TBD	mA
Active Power, data pass through: L0 state; 50% DDR2 SDRAM BW to downstream FBDIMM, 67% READ, 33% WRITE; primary and secondary channels enabled; command and address lines stable, CKE high; DDR2 SDRAM clock active.	IDD_ACTIVE_2	TBD	TBD	mA
Channel standby: Average power over 42 frames where the channel enters and exits L0s; DDR2 SDRAM devices Idle (0 BW); CKE LOW; command and address lines floated; DDR2 SDRAM lock active, ODE and CKE driven LOW.	IDD_LOS	TBD	TBD	mA
Training: Primary and secondary channels enabled; 100% toggle on all channel lanes; DDR2 SDRAM devices idle (0 BW); CKE HIGH, command and address lines stable; DDR2 SDRAM clock active.	IDD_TRAINING	TBD	TBD	mA

Table 12: VTT Currents

Description	Symbol	Typ	MAX	Unit
Idle current, DDR2 SDRAM device power down	ITT1	500	700	mA
Active power, 50% DDR2 SDRAM BW	ITT2	500	700	mA

Table 13: Reference Clock Input Specifications

Parameter	Symbol	Values		Unit	Notes
		MIN	MAX		
Reference clock frequency	*f*SCK	133.33	200	MHz	1, 2
Rise time, fall time	TSCK-RISE, TSCK-FALL	175	700	ps	3
Voltage high	VSCK-HIGH	660	850	mV	
Voltage low	VSCK-LOW	-150		mV	
Absolute crossing point	VCROSS-ABS	250	550	mV	4
Relative crossing point	VCROSS-REL	calculated	calculated		4, 5
Percent mismatch between rise and fall times	TSCK-RISE-FALL-MATCH	—	10	%	
Duty cycle of reference clock	TSCK-DUTYCYCLE	40	60	%	
Clock leakage current	II-CK	-10	10	µA	6, 7
Clock input capacitance	CI-CK	0.5	2	pF	7
Clock input capacitance delta	CI_CK(D)	-0.25	0.25	pF	8
Transport delay	T1		5	ns	9, 10
Phase jitter sample size	NSAMPLE	10^{16}		Periods	11
Reference clock jitter, filtered	TREF-JITTER		40	ps	12, 13
Reference clock deterministic jitter	TREF-DJ		TBD	ps	

Notes:
1. 133MHz for PC2-4200 and 166MHz for PC2-5300.
2. Measured with SSC disabled.
3. Measured differentially through the range of 0.175V to 0.525V.
4. The crossing point must meet the absolute and relative crossing point specification simultaneously.
5. VCROSS_REL_(MIN) and VCROSS_REL_(MAX) are derived using the following calculation: Min = 0.5 (V_{havg} - 0.710) + 0.250; and Max = 0.5 (V_{havg} - 0.710) + 0.550, where V_{havg} is the average of VSCK-HIGHM.
6. Measured with a single-ended input voltage of 1V.
7. Applies to reference clocks SCK and SCK#.
8. Difference between SCK and SCK# input.
9. T1 = |Tdatapath - Tclockpath| (excluding PLL loop delays). This parameter is not a direct clock output parameter but it indirectly determines the clock output parameter TREF-JITTER.
10. The net transport delay is the difference in time of flight between associated data and clock paths. The data path is defined from the reference clock source, through the TX, to data arrival at the data sampling point in the RX. The clock path is defined from the reference clock source to clock arrival at the same sampling point. See Figure 3-3. The path delays are caused by copper trace routes, on-chip routing, on-chip buffering, etc. They include the time-of-flight of interpolators or other clock adjustment mechanisms. They do *not* include the phase delays caused by finite PLL loop bandwidth because these delays are modeled by the PLL transfer functions.
11. Direct measurement of phase jitter records over 1016 periods is impractical. It is expected that the jitter will be measured over a smaller, yet statistically significant, sample size and the total jitter at 10^{16} samples extrapolated from an estimate of the sigma of the random jitter components.
12. Measured with SSC enabled on reference clock generator.
13. As measured after the phase jitter filter. This number is separate from the receiver jitter budget that is defined by the TRXTotal-MIN parameters.

Differential Transmitter and Receiver Specifications

Table 14: Differential Transmitter Output Specifications

Parameter	Symbol	Values		Unit	Comments
		MIN	MAX		
Differential peak-to-peak output voltage for large voltage swing	$V_{TX-DIFFp-p\_L}$	900	1,300	mV	EQ 1, Note1
Differential peak-to-peak output voltage for regular voltage swing	$V_{TX-DIFFp-p\_R}$	800		mV	EQ 1, Note1
Differential peak-to-peak output voltage for small voltage swing	$V_{TX-DIFFp-p\_S}$	520		mV	EQ 1, Note1
DC common code output voltage for large voltage swing	V_{TX-CM_L}		375	mV	EQ 2, Note1
DC common code output voltage for small voltage swing	V_{TX-CM_S}	135	280	mV	EQ 2, Note1, 2
De-emphasized differential output voltage ratio for -3.5 dB de-emphasis	$V_{TX-DE-3.5-Ratio}$	-3.0	-4.0	dB	1)3)4)
De-emphasized differential output voltage ratio for -6.0 dB de-emphasis	$V_{TX-DE-6.0-Ratio}$	-5.0	-7.0	dB	1)2)3)
AC peak-to-peak common mode output voltage for large swing	$V_{TX-CM-ACp-p-L}$		90	mV	EQ 7, Note1, 5
AC peak-to-peak common mode output voltage for regular swing	$V_{TX-CM-ACp-p-R}$		80	mV	EQ 7, Note1, 5
AC peak-to-peak common mode output voltage for small swing	$V_{TX-CM-ACp-p-S}$		70	mV	EQ 7, Note1, 5
Maximum single-ended voltage in EI condition DC + AC	$V_{TX-IDLE-SE}$		50	mV	6
Maximum single-ended voltage in EI condition DC + AC	$V_{TX-IDLE-SE-DC}$		20	mV	6
Maximum peak-to-peak differential voltage in EI condition	$V_{TX-IDLE-DIFFp-p}$		40	mV	
Single-ended voltage (w.r.t. Vss) on D+/D-	V_{TX-SE}	-75	750	mV	1, 7
Mimimum TX eye width, 3.2 and 4.0 Gb/s	$T_{TX-Eye-MIN}$	0.7		UI	1, 8
Mimimum TX eye width 4.8 Gb/s	$T_{TX-EYE-MIN4.8}$	TBD		UI	1, 8
Maximum TX deterministic jitter, 3.2 and 4.8 Gb/s	$T_{TX-DJ-DD}$		0.2	UI	1, 8, 9
Maximum TX deterministic jitter, 4.8 Gb/s	$T_{TX-DJ-DD-4.8}$		TBD	UI	1, 8, 9
Instantaneous pulse width	$T_{TX\ -PULSE}$	0.85		UI	10
Differential TX outout rise/fall time	$T_{TX-RISE}$ $T_{TX-FALL}$	30	90	ps	20–80% voltage, Note 1
Mismatch between rise and fall times	$T_{TX-RF-MISMATCH}$		20	ps	
Differential return loss	$RL_{TX-DIFF}$	8		dB	1 GHz–2.4 GHz, Note 11
Common mode return loss	RL_{TX-CM}	6		dB	1 GHz–2.4 GHz, Note 11
Transmitter termination impender	R_{TX}	41	55		12
D+/D- TX Impedance difference	$R_{TX-MATCH-DC}$		4	%	EQ 4, Boundaries are applied separately to high and low output voltage states
Lane-to lane skew at TX	$L_{TX-SKEW\ 1}$		100 + 3UI	ps	13, 15
Lane-to lane skew at TX	$L_{TX-SKEW\ 2}$		100 = 2UI	ps	14, 15

Table 14: Differential Transmitter Output Specifications

Parameter	Symbol	Values		Unit	Comments
		MIN	MAX		
Maximum TX Drift (resync mode)	$T_{TX-DRIFT-RESYNC}$		240	ps	16
Maximum TX Drift (resample mode only)	$T_{TX-DRIFT-RESAMPLE}$		120	ps	16
Bit Error Ratio	BER	10^{-12}			17

Notes:
1. Specified at the package pins into a timing and voltage compliance test load as shown in Figure 4-2 and in steps outlined in 4.1.2.1 of the JEDEC specification. Common-mode measurements to be performed using a 101010 pattern.
2. The transmitter designer should not artifically elevate the common mode in order to meet this specification.
3. This is the ratio of the VTX-DIFFp-p of the second and following bits after a transition divided by the VTX-DIFFp-p of the first bit after a transition.
4. De-emphasis shall be disabled in the calibration state.
5. Includes all sources of AC common mode noise
6. Single-ended voltages below that value that are simultaneously detected on D+ and D- are interpreted as the Electrical Idle condition.
7. The maximum value is specified to be at least (VTX-DIFFp-pL/4) + VTX-CML + (VTX-CM-ACp-p/2).
8. This number does not include the effects of SSC or reference clock jitter.
9. Defined as the expected maximum jitter for the given probability as measured in the system (TJ), les the unbounded jitter.
10. Puls width measure at 0V differential.
11. One of the components that contribute to the deterioration of the return loss is the ESD structure wich needs to be carefully designed
12. The termination small signal resistance; tolerance across voltages from 100 mV to 400 mV shall not exceed +/- 5 W with regard to the average of the values measured at 100 mV and 400 mV for that pin.
13. Lane to Lane skew at the Transmitter pins for an end component.
14. Lane to Lane skew at the Transmitter pins for an intermediate component (assuming zero Lane to Lane skew at the Receiver pins of the incoming PORT).
15. This is a static skew. An FBDIMM component is not allowed to change its lane to lane phase relationship after initialization.
16. Measured from the reference clock edge to the center of the output eye. This specification must be met across specified voltage and temperature ranges for a single component. Drift rate change is significantly below the tracking capability of the reciver.
17. BER per differential lane.

$$V_{TX-DIFFp-p} = 2 \times |V_{TX-D+} - V_{TX-D-}| \quad \text{(EQ 1)}$$

$$V_{TX-CM} = DC_{(avg)} \text{ of } (|V_{TX-D+} + V_{TX-D-}|/2) \quad \text{(EQ 2)}$$

$$V_{TX-CM-AC} = ((\text{Max}\,|V_{TX-D+} + V_{TX-D-}|)/2) - ((\text{Min}\,|V_{TX-D+} + V_{TX-D-}|)/2) \quad \text{(EQ 3)}$$

$$R_{TX-MATCH-DC} = 2 \times ((|R_{TX-D+} - R_{TX-D-}|)/(R_{TX-D+} + R_{TX-D-})) \quad \text{(EQ 4)}$$

Table 15: Differential Receiver Input Specifications

Parameter	Symbol	Values		Unit	Comments
		MIN	MAX		
Differential peak-to-peak input voltage for large voltage swing	$V_{RX-DIFFp-p}$	170	TBD	mV	EQ 5, Note1
Maximum single-ended voltage in EI condition	$V_{RX-IDLE-SE}$		75	mV	2, 3
Maximum single-ended voltage in EI condition (DC only)	$V_{RX-IDLE-SE-DC}$		50	mV	2, 3
Maximum peak-to-peak differential voltage in EI condition	$V_{RX-IDLE-DIFFp-p}$		65	mV	3
Single-ended voltage (w.r.t. Vss) on D+/D-	V_{RX-SE}	-300	900	mV	4
Single-pulse peak differential input voltage	$V_{RX-DIFF-PULSE}$	85		mV	4, 5
Amplitude ratio between adjacent symbols	$V_{RX-DIFF-ADJ-RATIO}$		TBD		4, 6
Maximum RX inherent timing error, 3.2 and 4.0 Gb/x	$T_{RX-TJ-MAX}$		0.4	UI	4, 7, 8
Maximum RX inherent deterministic timing eror, 3.2 and 4.8 Gb/s	$T_{RX-TJ-MAX4.8}$		TBD	UI	4, 7, 8
Single-pulse width as zero-voltage crossing	$V_{RX-DJ-DD}$		0.3	UI	4, 7, 8, 9
Single-pulse width at minimum-level crossing	$V_{RX-DJ-DD-4.8}$		TBD	UI	4, 7, 8, 9
Differential RX input rise/fall time	$T_{RX-PW-ZC}$	0.55		UI	4, 5
Common mode fo the input voltage	$T_{RX-PW-ML}$	0.2		UI	4, 5
Differential RX outout rise/fall time	$T_{RX-RISE}$ $T_{RX-FALL}$	50		ps	20–80% voltage
Common mode of input voltage	V_{RX-CM}	120	400	mV	EQ 6, Note1, 10
AC peak-to-peak common mode of input voltage	$V_{RX-CM-ACp-p}$		270	mV	EQ 7, Note1
Ratio of $V_{RX-CM-ACp-p}$ to minimum $V_{RX-DIFFp-p}$	$V_{RX-CM-EH-RATOP}$		45	%	11
Differential return loss	$RL_{RX-DIFF}$	9		dB	1 GHz–2.4 GHz, Note 12
Common mode return loss	RL_{RX-CM}	6		dB	1 GHz–2.4 GHz, Note 12
RX termination impedance	R_{RX}	41	55	Ω	13
D+/D- RX Impedance difference	$R_{RX-MATCH-DC}$		4	%	EQ 8
Lane-to lane PCB skew at RX	$L_{RX-PCB-SKEW}$		6	UI	Lane-to-lane skew at the receiver that must be tolerated. Note 14
Minimum RX drift tolerance	$T_{RX-DRIFT}$	400		ps	15
Minim data tracking 3dB bandwidth	F_{TRK}	0.2		MHz	16
Electrical idle entry detect time	$T_{EI-ENTRY-DETECT}$		60	ns	17
Electrical idle exit detect time	$T_{EI-EXIT-DETECT}$		30	ns	
Bit Error Ratio	BER		10^{-12}		18

Notes: 1. Specified at the package pins into a timing and voltage compliant test setup. Note that signal levels at the pad will be lower than at the pin.
2. Single-ended voltages below that value that are simultaneously detected on D+ and D- are interpreted as the Electrical Idle condition. Worst-case margins are determined for the case with transmitter using small voltage swing.
3. Multiple lanes need to detect the EI condition before the device can act upon the EI detection.

4. Specified at the package pins into a timing and voltage compliance test setup.
5. See Figure 3-8 and Figure 3-9. The single-pulse mask provides sufficient symbol energy for reliable RX reception. Each symbol must comply with both the single-pulse mask and the cumulative eyemask.
6. See Figure 3-10. The relative amplitude ratio limit between adjacent symbols prevents excessive intersymbol interference in the Rx. Each symbol must comply with the peak amplitude ratio with regard to both the preceding and subsequent symbols.
7. This number does not include the effects of SSC or reference clock jitter.
8. This number includes setup and hold of the RX sampling flop.
9. Defined as the dual-dirac deterministic timing error.
10. Allows for 15 mV DC offset between transmit and receive devices.
11. The received differential signal must satisfy both this ratio as well as the absolute maximum AC peaktopeak common mode specification. For example, if VRX-DIFFp-p is 200 mV, the maximum AC peak-to peak common mode is the lesser of (200 mV * 0.45 = 90 mV) and VRX-CM-AC-p-p .
12. One of the components that contribute to the deterioration of the return loss is the ESD structure which needs to be carefully designed.
13. The termination small signal resistance; tolerance across voltages from 100 mV to 400 mV shall not exceed +/- 5 W with regard to the average of the values measured at 100 mV and at 400 mV for that pin.
14. This number represents the lane-to-lane skew between TX and RX pins and does not include the transmitter output skew from the component driving the signal to the receiver. This is one component of the end-to-end channel skew in the AMB specification.
15. Measured from the reference clock edge to the center of the input eye. This specification must be met across specified voltage and temperature ranges for a single component. Drift rate of change is significantly below the tracking capability of the receiver.
16. This bandwidth number assumes the specified minimum data transition density. Maximum jitter at 0.2 MHz is 0.05 UI, see Section 4 for full jitter tolerance mask.
17. The specified time includes the time required to forward the EI entry condition.
18. BER per differential lane. Refer to Section 4 for a complete definition of Bit Error Ratio.

$$V_{RX\text{-}DIFFp\text{-}p} = 2 \times |V_{RX\text{-}D+} - V_{RX\text{-}D\text{-}}| \quad \text{(EQ 5)}$$

$$(V_{RX\text{-}CM} = DC_{(avg)} \text{ of } |V_{RX\text{-}D+} + V_{RX\text{-}D\text{-}}|/2) \quad \text{(EQ 6)}$$

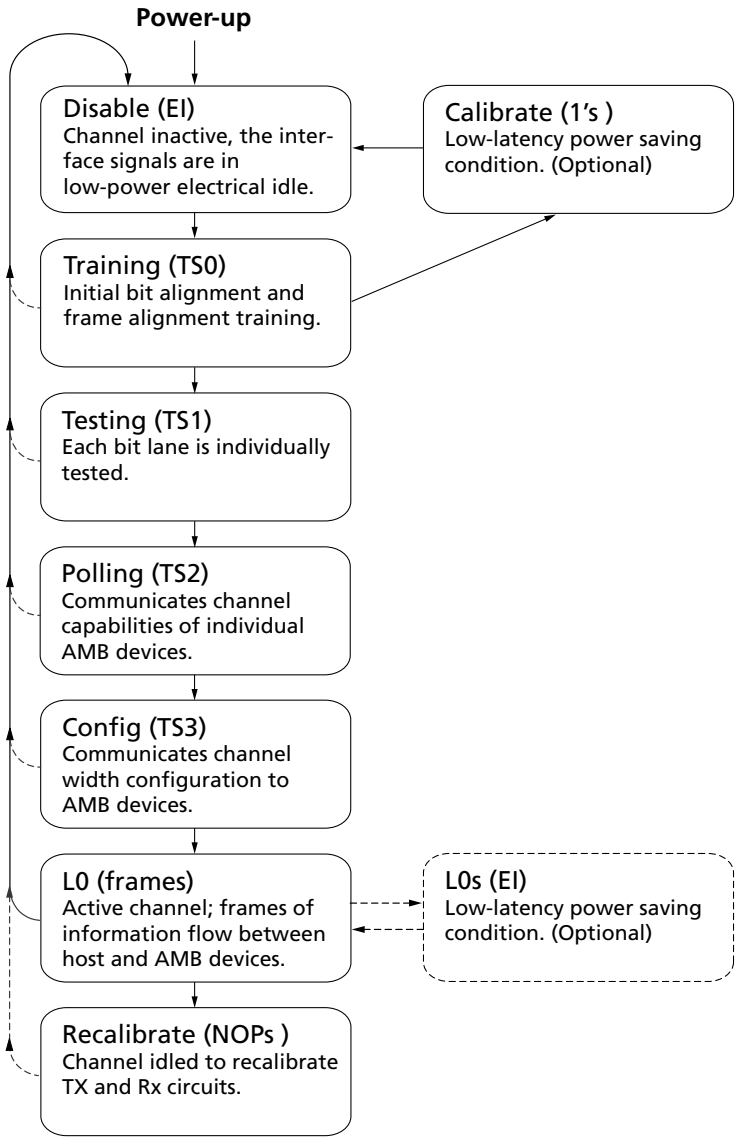
$$V_{RX\text{-}CM\text{-}AC} = ((\text{Max}\,|V_{RX\text{-}D+} + V_{RX\text{-}D\text{-}}|)/2)((\text{Min}\,|V_{RX\text{-}D+} + V_{RX\text{-}D\text{-}}|)/2) \quad \text{(EQ 7)}$$

$$R_{RX\text{-}MATCH\text{-}DC} = 2 \times ((|R_{RX\text{-}D+} - R_{RX\text{-}D\text{-}}|)/(R_{RX\text{-}D+} + R_{RX\text{-}D\text{-}})) \quad \text{(EQ 8)}$$

AMB Initialization

The FBD initialization process generally follows the top-to-bottom sequence of state transitions shown in the high level AMB Initialization Flow diagram in Figure 7, AMB Initialization Flow Diagram. The host must sequence the AMB devices through the Disable, Calibrate, (back to Disable), Training, Testing, and Polling states in order to transition the AMBs into the active channel L0 state. The value in parenthesis in each state bubble indicates the condition/activity of the links during these states.

Figure 7: AMB Initialization Flow Diagram



Each bit lane is initialized (mostly) independently to support fault tolerance. The transitions in Figure 7, AMB Initialization Flow Diagram represent the transitions of the AMB core logic state machine and are taken when the transition event is detected on the minimum required number of southbound bit lanes. The chain of FBDIMM links connecting the host to the AMBs must each be initialized to establish the timing for broadcasting

data frames in the southbound direction and for merging data frames in the northbound direction. The AMBs on the channel are generally initialized as a group but because each AMB is individually addressable many alternate initialization sequences may be employed.

Serial Presence-Detect

SPD Clock and Data Conventions

Data states on the SDA line can change only during SCL LOW. SDA state changes during SCL HIGH are reserved for indicating start and stop conditions, as shown in Figure 8, Data Validity, and Figure 9, Definition of Start and Stop.

SPD Start Condition

All commands are preceded by the start condition, which is a HIGH-to-LOW transition of SDA when SCL is HIGH. The SPD device continuously monitors the SDA and SCL lines for the start condition and will not respond to any command until this condition has been met.

SPD Stop Condition

All communications are terminated by a stop condition, which is a LOW-to-HIGH transition of SDA when SCL is HIGH. The stop condition is also used to place the SPD device into standby power mode.

SPD Acknowledge

Acknowledge is a software convention used to indicate successful data transfers. The transmitting device, either master or slave, will release the bus after transmitting eight bits. During the ninth clock cycle, the receiver will pull the SDA line LOW to acknowledge that it received the eight bits of data, as shown in Figure 10, Acknowledge Response from Receiver.

The SPD device will always respond with an acknowledge after recognition of a start condition and its slave address. If both the device and a WRITE operation have been selected, the SPD device will respond with an acknowledge after the receipt of each subsequent eight-bit word. In the read mode ,the SPD device will transmit eight bits of data, release the SDA line, and monitor the line for an acknowledge. If an acknowledge is detected and no stop condition is generated by the master, the slave will continue to transmit data. If an acknowledge is not detected, the slave will terminate further data transmissions and await the stop condition to return to standby power mode.

Figure 8: Data Validity

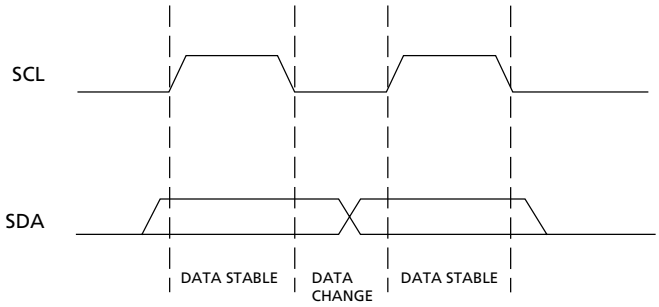


Figure 9: Definition of Start and Stop

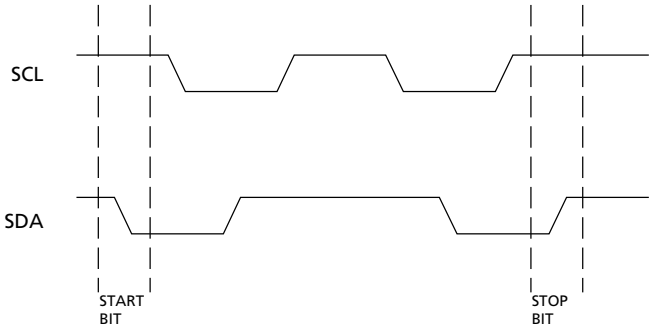


Figure 10: Acknowledge Response from Receiver

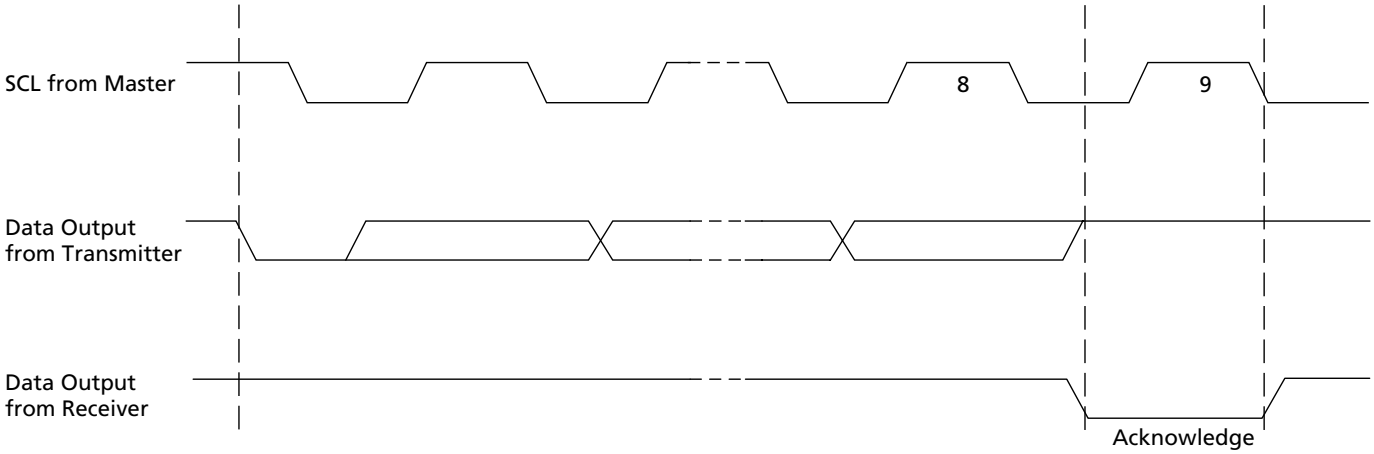


Table 16: EEPROM Device Select Code

The most significant bit (b7) is sent first

Select Code	Device Type Identifier				Chip Enable			RW
	b7	b6	b5	b4	b3	b2	b1	b0
Memory Area Select Code (two arrays)	1	0	1	0	SA2	SA1	SA0	RW
Protection Register Select Code	0	1	1	0	SA2	SA1	SA0	RW

Table 17: EEPROM Operating Modes

Mode	RW Bit	WC	Bytes	Initial Sequence
Current address read	1	VIH or VIL	1	Start, device select, RW = '1'
Random address read	0	VIH or VIL	1	Start, device select, RW = '0', Address
	1	VIH or VIL	1	Restart, device select, RW = '1'
Sequential read	1	VIH or VIL	≥ 1	Similar to current or random address read
Byte write	0	VIL	1	Start, device select, RW = '0'
Page write	0	VIL	≤ 16	Start, device select, RW = '0'

Figure 11: SPD EEPROM Timing Diagram

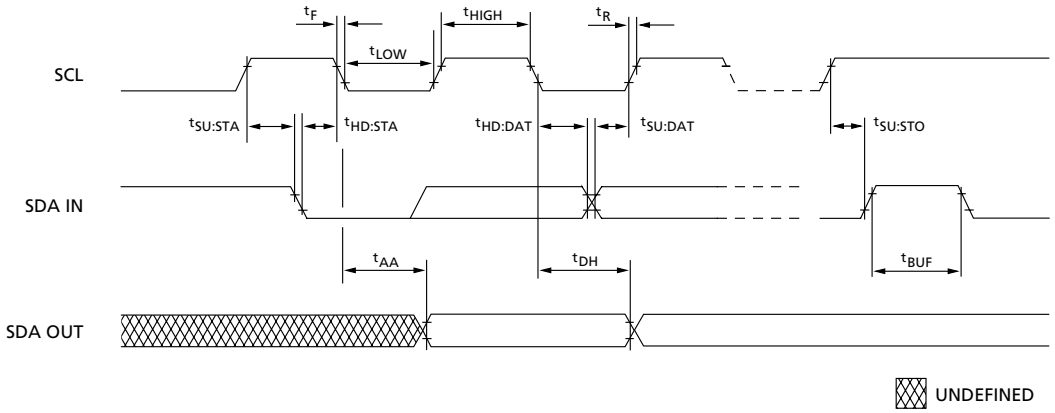


Table 18: Serial Presence-Detect EEPROM DC Operating Conditions
All voltages referenced to V_{SS}; V_{DDSPD} = +1.7V to +3.6V

Parameter/Condition	Symbol	MIN	MAX	Units
Supply voltage	V_{DDSPD}	1.7	3.6	V
Input high voltage: logic 1; all inputs	V_{IH}	V_{DDSPD} x 0.7	V_{DDSPD} + 0.5	V
Input low voltage: logic 0; all inputs	V_{IL}	-0.6	V_{DDSPD} x 0.3	V
Output low voltage: I_{OUT} = 3mA	V_{OL}	–	0.4	V
Input leakage current: V_{IN} = GND to V_{DD}	I_{LI}	0.10	3	µA
Output leakage current: V_{OUT} = GND to V_{DD}	I_{LO}	0.05	3	µA
Standby current:	I_{SB}	1.6	4	µA
Power supply current, READ: SCL clock frequency = 100 KHz	ICC_R	0.4	1	mA
Power supply current, WRITE: SCL clock frequency = 100 KHz	ICC_W	2	3	mA

Table 19: Serial Presence-Detect EEPROM AC Operating Conditions
All voltages referenced to V_{SS}; V_{DDSPD} = +1.7V to +3.6V

Parameter/Condition	Symbol	MIN	MAX	Units	Notes
SCL LOW to SDA data-out valid	^tAA	0.2	0.9	µs	1
Time the bus must be free before a new transition can start	^tBUF	1.3		µs	
Data-out hold time	^tDH	200		ns	
SDA and SCL fall time	^tF		300	ns	2
Data-in hold time	$^tHD:DAT$	0		µs	
Start condition hold time	$^tHD:STA$	0.6		µs	
Clock HIGH period	^tHIGH	0.6		µs	
Noise suppression time constant at SCL, SDA inputs	^tI		50	ns	
Clock LOW period	^tLOW	1.3		µs	
SDA and SCL rise time	^tR		0.3	µs	2
SCL clock frequency	^fSCL		400	KHz	
Data-in setup time	$^tSU:DAT$	100		ns	
Start condition setup time	$^tSU:STA$	0.6		µs	3
Stop condition setup time	$^tSU:STO$	0.6		µs	
WRITE cycle time	^tWRC		10	ms	4

Notes:
1. To avoid spurious start and stop conditions, a minimum delay is placed between SCL = 1 and the falling or rising edge of SDA.
2. This parameter is sampled.
3. For a restart condition, or following a WRITE cycle.
4. The SPD EEPROM WRITE cycle time (^tWRC) is the time from a valid stop condition of a write sequence to the end of the EEPROM internal ERASE/PROGRAM cycle. During the WRITE cycle, the EEPROM bus interface circuit is disabled, SDA remains HIGH due to pull-up resistor, and the EEPROM does not respond to its slave address.

Table 20: Serial Presence-Detect Matrix

"1"/"0": Serial Data, "driven to HIGH"/"driven to LOW"

Byte	Description	Entry	MT18HTF6472F	MT18HTF12872F	MT18HTF25672F
0	CRC Range / SPD Bytes Total / Bytes Used	Bytes 0 - 116/ 256 Bytes/ 176 Bytes	92	92	92
1	SPD revision	Initial Release 1.0	10	10	10
2	Key byte / DRAM device type	DDR2 FBDIMM	09	09	09
3	Voltage levels of this assembly	DRAM|AMB	12	12	12
4	SDRAM addressing: Device Rows | Columns | Banks	256Mb, 512Mb, 1Gb	28	48	49
5	Module physical attributes: Height | Thickness	1.18 in., 0.315 - 0.354in.	24	24	24
6	Module type	FBDIMM	07	07	07
7	Module organization: Module Ranks | SDRAM Device Width (I/Os)	Single Rank, x4	08	08	08
8	Fine timebase dividend and divisor	5ps	51	51	51
9	Medium timebase dividend	1/4=0.25ns	01	01	01
10	Medium timebase divisor	1/4=0.25ns	04	04	04
11	SDRAM minimum cycle time (^{t}CKmin)	-53E -667	0F 0C	0F 0C	0F 0C
12	SDRAM maximum cycle time (^{t}CKmax)	-53E, -667	20	20	20
13	SDRAM CAS latencies supported: -53E CAS 4, 3 | -667 CAS 5, 4, 3	-53E -667	23 33	23 33	23 33
14	SDRAM minimum cas latency time (^{t}CAS)	15ns	3C	3C	3C
15	SDRAM write recovery times supported	Range, Min	22	22	22
16	SDRAM write recovery time (^{t}WR)	-53E, -667	3C	3C	3C
17	SDRAM write latencies supported	Range, Min	52	52	52
18	SDRAM additive latencies supported	Range, Min	50	50	50
19	SDRAM minimum RAS to CAS delay (^{t}RCD)	-53E, -667	3C	3C	3C
20	SDRAM minimum row active to row active delay (^{t}RRD)	-53E, -667	1E	1E	1E
21	SDRAM minimum row precharge time (^{t}RP)	-53E, -667	3C	3C	3C
22	SDRAM upper nibbles for ^{t}RAS and ^{t}RC		00	00	00
23	SDRAM minimum active to precharge time (^{t}RAS)	-53E, -667	B4	B4	B4
24	SDRAM minimu auto-refresh to active/auto-refresh time (^{t}RC)	-53E, -667	DC	DC	DC
25	SDRAM minimum auto-refresh to active/auto-refresh command period (^{t}RFC - MSB)	256Mb 512Mb 1Gb	2C A4 FE	2C A4 FE	2C A4 FE
26	SDRAM minimum auto-refresh to active/auto-refresh command period (^{t}RFC - LSB)	256Mb 512Mb 1Gb	01 01 01	01 01 01	01 01 01
27	SDRAM internal write to read command delay (^{t}WTR)	-53E, -667	1E	1E	1E

Table 20: Serial Presence-Detect Matrix (Continued)

"1"/"0": Serial Data, "driven to HIGH"/"driven to LOW"

Byte	Description	Entry	MT18HTF6472F	MT18HTF12872F	MT18HTF25672F
28	SDRAM internal read to precharge command delay (^{t}RTP)	-53E, -667	1E	1E	1E
29	SDRAM burst lengths supported	4, 8	03	03	03
30	SDRAM drivers / Terminations Supported: 03 = 75 and 100 Ohm, 07 = 50, 75 and 100 Ohm	-53E -667	03 07	03 07	03 07
31	Drivers Supported	Weak Drivers	01	01	01
32	SDRAM refresh rate (^{t}REFI)	7.8 µs	02	02	02
33	Bits 7:4: TCASEMAX Delta (DRAM case temperature difference between maximum case temperature and baseline maximum case temperature), the baseline maximum case temperature is 85°C. Bits 3:0: DT4R4W Delta (Case temperature rise difference between IDD4R/page open burst READ and IDD4W/page open burst WRITE operations).	TBD	TBD	TBD	TBD
34	Thermal resistance of DRAM device package from top (case) to ambient (Psi T-A DRAM) at still air condition based on JESD51-2 standard.	TBD	TBD	TBD	TBD
35	DT0/TCASE mode bits: Bits 7:2: Case temperature rise from ambient due to IDD0/activate precharge operation minus 2.8°C offset temperature. Bit 1: Double refresh mode bit. Bit 0: High Temperature self-refresh rate support indication	TBD	TBD	TBD	TBD
36	DT2N/DT2Q: Case temperature rise from ambient due to IDD2N/ precharge standby operation for UDIMM and due to IDD2Q/ precharge quiet standby operation for RDIMM.	TBD	TBD	TBD	TBD
37	DT2P: Case temperature rise from ambient due to IDD2P/ precharge power-down operation.	TBD	TBD	TBD	TBD
38	DT3N: Case temperature rise from ambient due to IDD3N/active standby operation.	TBD	TBD	TBD	TBD
39	DT4R/mode bit: Bits 7:1: Case temperature rise from ambient due to IDD4R/page open burst read operation. Bit 0: Mode bit to specify if DT4W is greater or less than DT4R.	TBD	TBD	TBD	TBD
40	DT5B: Case temperature rise from ambient due to IDD5B/burst refresh operation.	TBD	TBD	TBD	TBD
41	DT7: Case temperature rise from ambient due to IDD7/bank interleave read mode operation.	TBD	TBD	TBD	TBD
42-80	FBDIMM Reserved Btyes	00	00	00	00
81-116	AMB personality bytes: Post-initialization	TBD	TBD	TBD	TBD
117-118	Module ID: Module manufacturer's JEDEC ID code	Micron	802C	802C	802C
119	Module ID: Module manufacturing location	01–12	01–0C	01–0C	01–0C
120-121	Module ID: Module manufacturing date		Variable Data	Variable Data	Variable Data
122-125	Module ID: Module serial number		Variable Data	Variable Data	Variable Data
126-127	Checksum for bytes 0 -116	TBD	TBD	TBD	TBD

Table 20: Serial Presence-Detect Matrix (Continued)

"1"/"0": Serial Data, "driven to HIGH"/"driven to LOW"

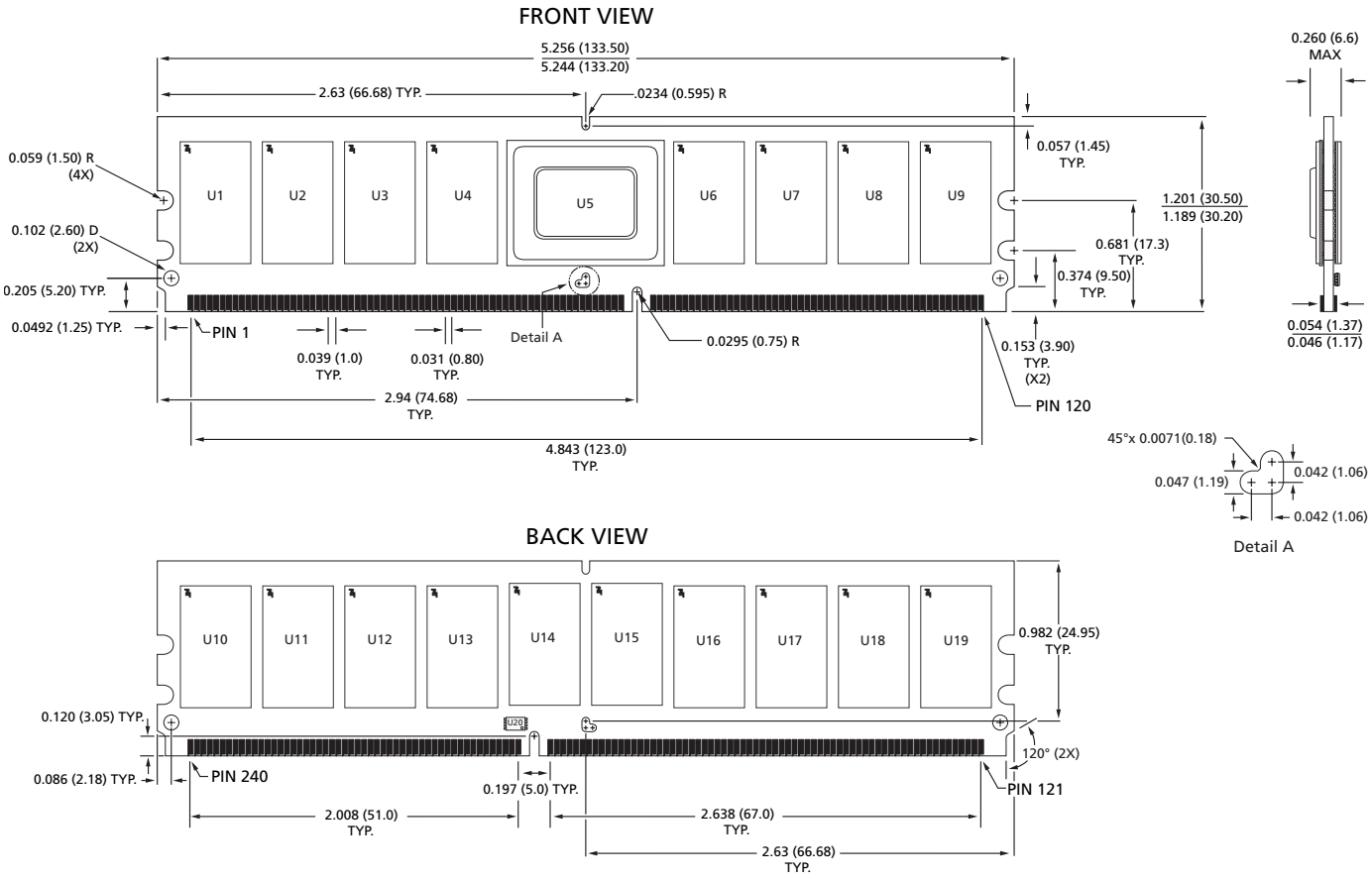
Byte	Description	Entry	MT18HTF6472F	MT18HTF12872F	MT18HTF25672F
128-145	Module part number		Variable Data	Variable Data	Variable Data
146-147	Module revision code		Variable Data	Variable Data	Variable Data
148-149	DRAM manufacturer's JEDEC ID code	Micron	002C	002C	002C
150-175	Manufacturer-specific data (RSVD)		FF	FF	FF
176-255	Open for customer use		FF	FF	FF

Module Dimensions

All dimensions are in inches (millimeters). Module shown without heat spreader dimensions.

The dimensional diagram is for reference only. Refer to the MO document for complete design dimensions.

Figure 12: 240-pin DDR2 FBDIMM Module Dimensions



Data Sheet Designation

Preliminary: Initial characterization limits, subject to change upon full characterization of production devices.

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