DDR2 SDRAM

MT47H64M4 – 16 Meg x 4 x 4 banks
MT47H32M8 – 8 Meg x 8 x 4 banks
MT47H16M16 – 4 Meg x 16 x 4 banks

For the latest data sheet, refer to Micron's Web site: http://www.micron.com/ddr2

Features

- RoHS compliant
- V_{DD} = +1.8V ±0.1V, V_{DDQ} = +1.8V ±0.1V
- JEDEC standard 1.8V I/O (SSTL_18-compatible)
- Differential data strobe (DQS, DQS#) option
- 4-bit prefetch architecture
- Duplicate output strobe (RDQS) option for x8
- DLL to align DQ and DQS transitions with CK
- 4 internal banks for concurrent operation
- Programmable CAS latency (CL)
- Posted CAS additive latency (AL)
- WRITE latency = READ latency - 1 ^{t}CK
- Programmable burst lengths: 4 or 8
- Adjustable data-output drive strength
- 64ms, 8,192-cycle refresh
- On-die termination (ODT)
- Industrial temperature (IT) option
- Supports JEDEC clock jitter specification

Options — Marking

- Configuration
  - 64 Meg x 4 (16 Meg x 4 x 4 banks) — 64M4
  - 32 Meg x 8 (8 Meg x 8 x 4 banks) — 32M8
  - 16 Meg x 16 (4 Meg x 16 x 4 banks) — 16M16
- FBGA package (lead-free)
  - x4, x8 60-ball FBGA (8mm x 12mm) (:B) — BP
  - x16 84-ball FBGA (8mm x 14)mm (:B) — BG
- Timing – cycle time
  - 5.0ns @ CL = 3 (DDR2-400) — -5E
  - 3.75ns @ CL = 4 (DDR2-533) — -37E
  - 3.0ns @ CL = 5 (DDR2-667) — -3
  - 3.0ns @ CL = 4 (DDR2-667) — -3E
  - 2.5ns @ CL = 5 (DDR2-800) — -25E
- Operating temperature
  - Commercial (0°C ≤ T_C ≤ 85°C) — None
  - Industrial (-40°C ≤ T_C ≤ 95°C; -40°C ≤ T_A ≤ 85°C) — IT
- Revision — :B

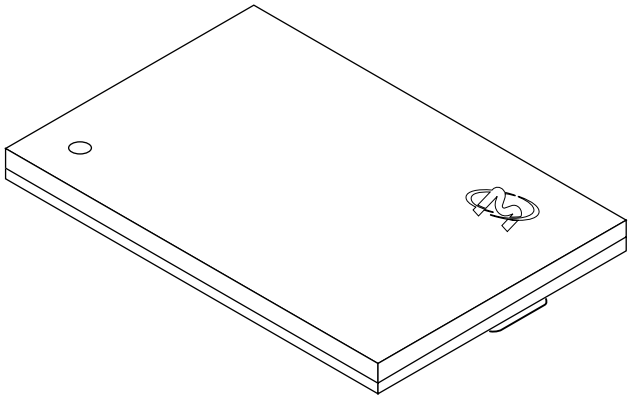


Table 1: Configuration Addressing

Architecture	64 Meg x 4	32 Meg x 8	16 Meg x 16
Configuration	16 Meg x 4 x 4 banks	8 Meg x 8 x 4 banks	4 Meg x 16 x 4 banks
Refresh Count	8K	8K	8K
Row Addr.	8K (A0–A12)	8K (A0–A12)	8K (A0–A12)
Bank Addr.	4 (BA0–BA1)	4 (BA0–BA1)	4 (BA0–BA1)
Column Addr.	2K (A0–A9, A11)	1K (A0–A9)	512 (A0–A8)

Table 2: Key Timing Parameters

Speed Grade	Data Rate (MHz)			^{t}RCD (ns)	^{t}RP (ns)	^{t}RC (ns)
	CL = 3	CL = 4	CL = 5			
-5E	400	400	N/A	15	15	55
-37E	400	533	N/A	15	15	55
-3	400	533	667	15	15	55
-3E	N/A	667	667	12	12	54
-25E	N/A	533	800	12.5	12.5	55

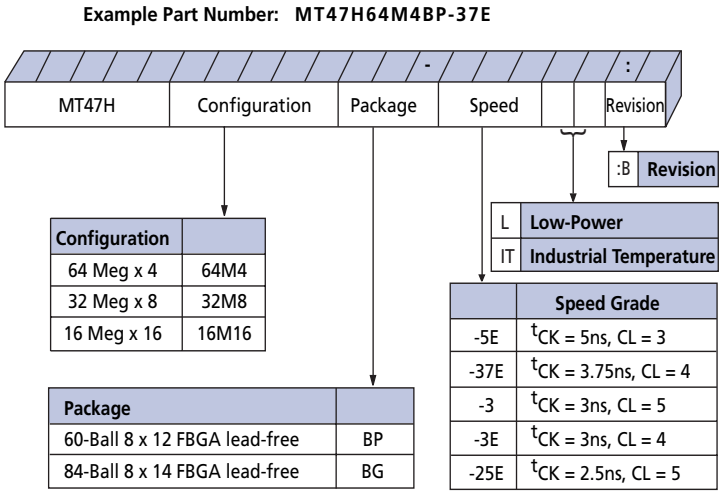
Table of Contents

List of Figures

List of Tables

Part Numbers

Figure 1: 256Mb DDR2 Part Numbers



Note: Not all speeds and configurations are available. Contact Micron sales for current revision.

FBGA Part Marking Decoder

Due to space limitations, FBGA-packaged components have an abbreviated part marking that is different from the part number. Micron's FBGA Part Marking Decoder is available at www.micron.com/decoder.

General Description

The 256Mb DDR2 SDRAM is a high-speed CMOS, dynamic random-access memory containing 268,435,456 bits. It is internally configured as a 4-bank DRAM. The functional block diagrams of the all device configurations are shown in the "Functional Description" section. Ball assignments and signal descriptions are shown in the "Ballouts and Ball Descriptions" section.

The 256Mb DDR2 SDRAM uses a double-data-rate architecture to achieve high-speed operation. The double data rate architecture is essentially a 4*n*-prefetch architecture, with an interface designed to transfer two data words per clock cycle at the I/O balls. A single read or write access for the 256Mb DDR2 SDRAM effectively consists of a single 4*n*-bit-wide, one-clock-cycle data transfer at the internal DRAM core and four corresponding *n*-bit-wide, one-half-clock-cycle data transfers at the I/O balls.

A bidirectional data strobe (DQS, DQS#) is transmitted externally, along with data, for use in data capture at the receiver. DQS is a strobe transmitted by the DDR2 SDRAM during READs and by the memory controller during WRITEs. DQS is edge-aligned with data for READs and center-aligned with data for WRITEs. The x16 offering has two data strobes, one for the lower byte (LDQS, LDQS#) and one for the upper byte (UDQS, UDQS#).

The 256Mb DDR2 SDRAM operates from a differential clock (CK and CK#); the crossing of CK going HIGH and CK# going LOW will be referred to as the positive edge of CK. Commands (address and control signals) are registered at every positive edge of CK. Input data is registered on both edges of DQS, and output data is referenced to both edges of DQS, as well as to both edges of CK.

Read and write accesses to the DDR2 SDRAM are burst-oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an ACTIVE command, which is then followed by a READ or WRITE command. The address bits registered coincident with the ACTIVE command are used to select the bank and row to be accessed. The address bits registered coincident with the READ or WRITE command are used to select the bank and the starting column location for the burst access.

The DDR2 SDRAM provides for programmable read or write burst lengths of four or eight locations. DDR2 SDRAM supports interrupting a burst read of eight with another read, or a burst write of eight with another write. An auto precharge function may be enabled to provide a self-timed row precharge that is initiated at the end of the burst access.

As with standard DDR SDRAMs, the pipelined, multibank architecture of DDR2 SDRAMs allows for concurrent operation, thereby providing high, effective bandwidth by hiding row precharge and activation time.

A self refresh mode is provided, along with a power-saving power-down mode.

All inputs are compatible with the JEDEC standard for SSTL_18. All full drive-strength outputs are SSTL_18-compatible.

Industrial Temperature

The industrial temperature (IT) device has two simultaneous requirements: ambient temperature surrounding the device cannot exceed -40°C or +85°C, and the case temperature cannot exceed -40°C or 95°C. JEDEC specifications require the refresh rate to double when T_C exceeds 85°C; this also requires use of the high-temperature self refresh option. Additionally, ODT resistance and the input/output impedance must be derated when the T_C is < 0°C or > 85°C.

General Notes

- The functionality and the timing specifications discussed in this data sheet are for the DLL-enabled mode of operation.
- Throughout the data sheet, the various figures and text refer to DQs as “DQ.” The DQ term is to be interpreted as any and all DQ collectively, unless specifically stated otherwise. Additionally, the x16 is divided into 2 bytes, the lower byte and upper byte. For the lower byte (DQ0–DQ7), DM refers to LDM and DQS refers to LDQS. For the upper byte (DQ8–DQ15), DM refers to UDM and DQS refers to UDQS.
- Complete functionality is described throughout the document and any page or diagram may have been simplified to convey a topic and may not be inclusive of all requirements.
- Any specific requirement takes precedence over a general statement.

Ballouts and Ball Descriptions

Figure 2: 84-Ball FBGA Assignment (x16), 8mm x 14mm (Top View)

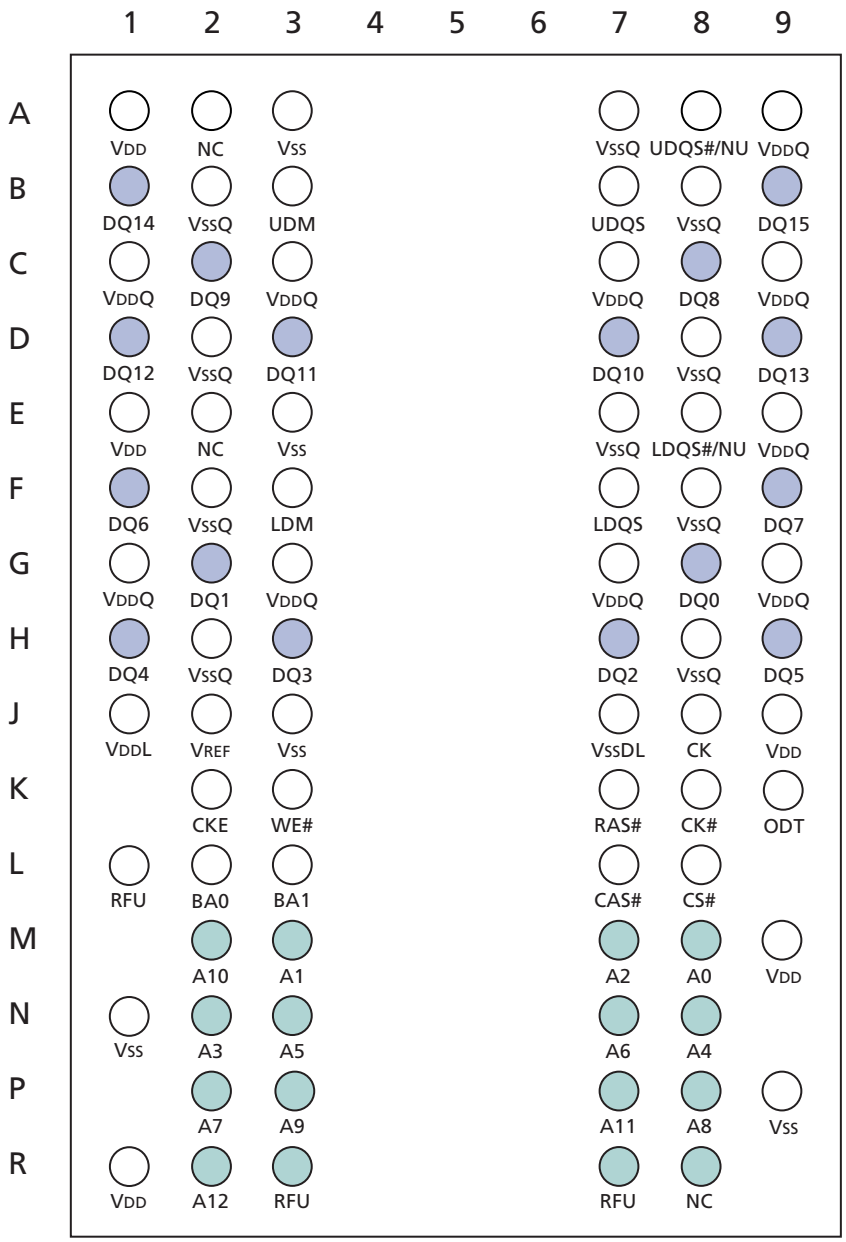


Figure 3: 60-Ball FBGA Assignment (x4, x8), 8mm x 12mm (Top View)

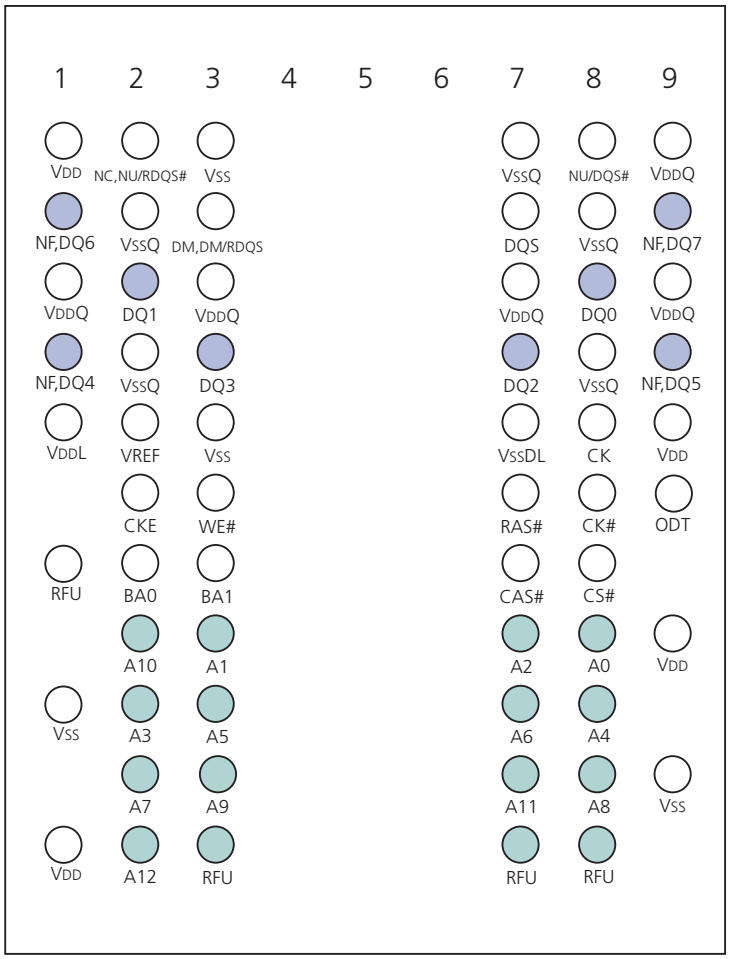


Table 3: 84-/60-Ball FBGA Descriptions 64 Meg x 4, 32 Meg x 8, 16 Meg x 16

x16 FBGA Ball Number	x4, x8 FBGA Ball Number	Symbol	Type	Description
K9	F9	ODT	Input	On-Die termination: ODT (registered HIGH) enables termination resistance internal to the DDR2 SDRAM. When enabled, ODT is only applied to each of the following balls: DQ0–DQ15, LDM, UDM, LDQS, LDQS#, UDQS, and UDQS# for the x16; DQ0–DQ7, DQS, DQS#, RDQS, RDQS#, and DM for the x8; DQ0–DQ3, DQS, DQS#, and DM for the x4. The ODT input will be ignored if disabled via the LOAD MODE command.
J8, K8	E8, F8	CK, CK#	Input	Clock: CK and CK# are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK and negative edge of CK#. Output data (DQs and DQS/DQS#) is referenced to the crossings of CK and CK#.
K2	F2	CKE	Input	Clock enable: CKE (registered HIGH) activates and CKE (registered LOW) deactivates clocking circuitry on the DDR2 SDRAM. The specific circuitry that is enabled/disabled is dependent on the DDR2 SDRAM configuration and operating mode. CKE LOW provides precharge power-down mode and SELF REFRESH operation (all banks idle), or active power-down (row active in any bank). CKE is synchronous for power-down entry, Power-down exit, output disable, and for self refresh entry. CKE is asynchronous for self refresh exit. Input buffers (excluding CK, CK#, CKE, and ODT) are disabled during power-down. Input buffers (excluding CKE) are disabled during self refresh. CKE is an SSTL_18 input but will detect a LVCMOS LOW level once V_{DD} is applied during first power-up. After V_{REF} has become stable during the power on and initialization sequence, it must be maintained for proper operation of the CKE receiver. For proper SELF-REFRESH operation, V_{REF} must be maintained.
L8	G8	CS#	Input	Chip select: CS# enables (registered LOW) and disables (registered HIGH) the command decoder. All commands are masked when CS# is registered HIGH. CS# provides for external bank selection on systems with multiple ranks. CS# is considered part of the command code.
K7, L7, K3	F7, G7, F3	RAS#, CAS#, WE#	Input	Command inputs: RAS#, CAS#, and WE# (along with CS#) define the command being entered.
F3, B3	B3	LDM, UDM	Input	Input data mask: DM is an input mask signal for write data. Input data is masked when DM is concurrently sampled HIGH during a WRITE access. DM is sampled on both edges of DQS. Although DM balls are input-only, the DM loading is designed to match that of DQ and DQS balls. LDM is DM for lower byte DQ0–DQ7 and UDM is DM for upper byte DQ8–DQ15.
L2, L3	G2, G3	BA0, BA1	Input	Bank address inputs: BA0 and BA1 define to which bank an ACTIVE, READ, WRITE, or PRECHARGE command is being applied. BA0 and BA1 define which mode register including MR, EMR, EMR(2), and EMR(3) is loaded during the LOAD MODE command.

Table 3: 84-/60-Ball FBGA Descriptions 64 Meg x 4, 32 Meg x 8, 16 Meg x 16

x16 FBGA Ball Number	x4, x8 FBGA Ball Number	Symbol	Type	Description
M8, M3, M7, N2, N8, N3, N7, P2, P8, P3, M2, P7, R2	H8, H3, H7, J2, J8, J3, J7, K2, K8, K3, H2, K7, L2	A0–A12	Input	Address inputs: Provide the row address for ACTIVE commands, and the column address and auto precharge bit (A10) for READ/WRITE commands, to select one location out of the memory array in the respective bank. A10 sampled during a PRECHARGE command determines whether the PRECHARGE applies to one bank (A10 LOW, bank selected by BA0, BA1) or all banks (A10 HIGH). The address inputs also provide the op-code during a LOAD MODE command.
G8, G2, H7, H3, H1, H9, F1, F9, C8, C2, D7, D3, D1, D9, B1, B9	–	DQ0–DQ15	I/O	Data input/output: Bidirectional data bus for 16 Meg x 16.
–	C8, C2, D7, D3, D1, D9, B1, B9	DQ0–DQ7	I/O	Data input/output: Bidirectional data bus for 32 Meg x 8.
–	C8, C2, D7, D3	DQ0–DQ3	I/O	Data input/output: Bidirectional data bus for 64 Meg x 4.
B7, A8	–	UDQS, UDQS#	I/O	Data strobe for upper byte: Output with read data, input with write data for source synchronous operation. Edge-aligned with read data, center-aligned with write data. UDQS# is only used when differential data strobe mode is enabled via the LOAD MODE command.
F7, E8	–	LDQS, LDQS#	I/O	Data strobe for lower byte: Output with read data, input with write data for source synchronous operation. Edge-aligned with read data, center-aligned with write data. LDQS# is only used when differential data strobe mode is enabled via the LOAD MODE command.
–	B7, A8	DQS, DQS#	I/O	data strobe: output with read data, input with write data for source synchronous operation. edge-aligned with read data, center aligned with write data. dqs# is only used when differential data strobe mode is enabled via the load mode command.
–	B3, A2	RDQS, RDQS#	Output	Redundant data strobe for 32 Meg x 8 only. RDQS is enabled/ disabled via the LOAD MODE command to the extended mode register (EMR). When RDQS is enabled, RDQS is output with read data only and is ignored during write data. When RDQS is disabled, ball B3 becomes data mask (see DM ball). RDQS# is only used when RDQS is enabled *and* differential data strobe mode is enabled.
A1, E1, J9, M9, R1	A1, E9, H9, L1	V_{DD}	Supply	Power supply: 1.8V ±0.1V.
J1	E1	V_{DDL}	Supply	DLL Power supply: 1.8V ±0.1V.
A9, C1, C3, C7, C9, E9, G1, G3, G7, G9	A9, C1, C3, C7, C9	V_{DDQ}	Supply	DQ Power supply: 1.8V ±0.1V. Isolated on the device for improved noise immunity.
J2	E2	V_{REF}	Supply	SSTL_18 reference voltage.
A3, E3, J3, N1, P9	A3, E3, J1, K9	V_{SS}	Supply	Ground.
J7	E7	V_{SSDL}	Supply	DLL ground. Isolated on the device from V_{SS} and V_{SSQ}.
A7, B2, B8, D2, D8, E7, F2, F8, H2, H8,	A7, B2, B8, D2, D8	V_{SSQ}	Supply	DQ ground. Isolated on the device for improved noise immunity.

Table 3: 84-/60-Ball FBGA Descriptions 64 Meg x 4, 32 Meg x 8, 16 Meg x 16

x16 FBGA Ball Number	x4, x8 FBGA Ball Number	Symbol	Type	Description
A2, E2	A2, B1, B9, D1, D9	NC	–	No connect: These balls should be left unconnected.
	D1, D9, B1, B9	NF	–	No function: These balls are used as DQ4–DQ7 on the 32 Meg x 8, but are NF (no function) on the 16 Meg x 16 configuration.
A8, E8	A2, A8	NU	–	Not used: If EMR[E10] = 0, A8 and E8 are UDQS# and LDQS#. If EMR[E10] = 1, then A8 and E8 are Not Used.
L1, R3, R7, R8	G1, L3, L7, L8	RFU	–	Reserved for future use: Bank address bit BA2(L1) is reserved for 1Gb, 2Gb, and 4Gb densities. Row address bits A13(R8), A14(R3), and A15(R7) are reserved for higher densities.

Functional Description

The 256Mb DDR2 SDRAM is a high-speed CMOS dynamic random-access memory containing bits. The 256Mb DDR2 SDRAM is internally configured as a 4-bank DRAM.

The 256Mb DDR2 SDRAM uses a double data rate architecture to achieve high-speed operation. The DDR2 architecture is essentially a 4*n*-prefetch architecture, with an interface designed to transfer two data words per clock cycle at the I/O balls. A single read or write access for the 256Mb DDR2 SDRAM consists of a single 4*n*-bit-wide, one-clock-cycle data transfer at the internal DRAM core and four corresponding *n*-bit- wide, one-half-clock-cycle data transfers at the I/O balls.

Prior to normal operation, the DDR2 SDRAM must be initialized. The following sections provide detailed information covering device initialization, register definition, command descriptions, and device operation.

Figure 4: Functional Block Diagram (64 Meg x 4)

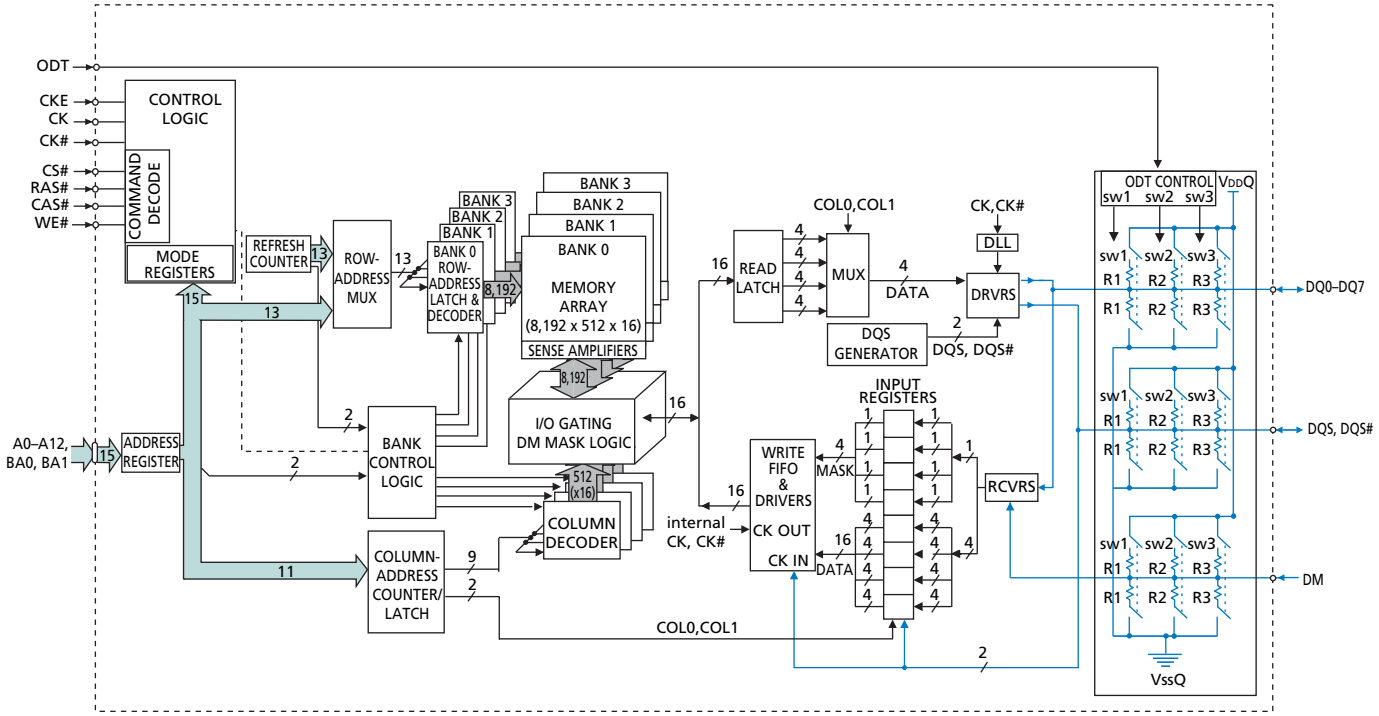


Figure 5: Functional Block Diagram (32 Meg x 8)

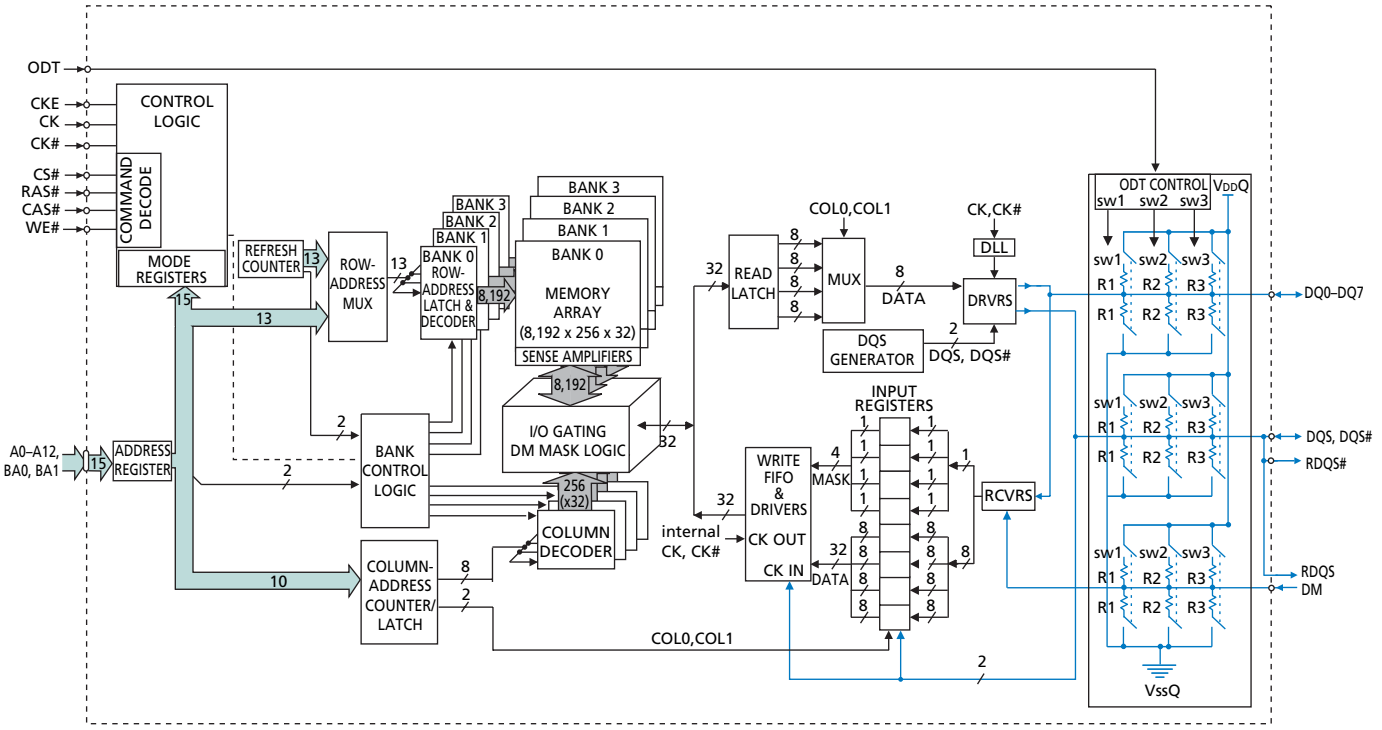
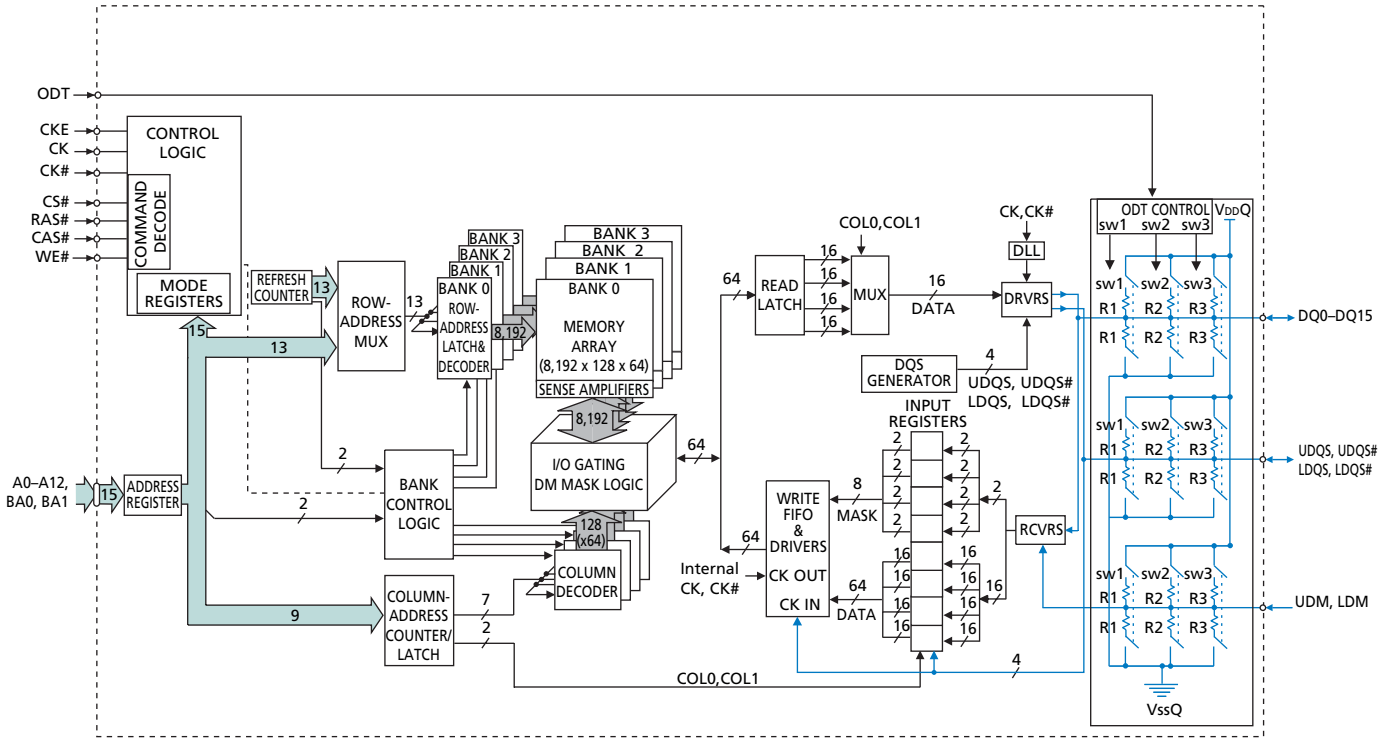


Figure 6: Functional Block Diagram (16 Meg x 16)



Initialization

DDR2 SDRAMs must be powered up and initialized in a predefined manner. Operational procedures other than those specified may result in undefined operation. The following sequence is required for power up and initialization and is shown in Figure 7 on page 18.

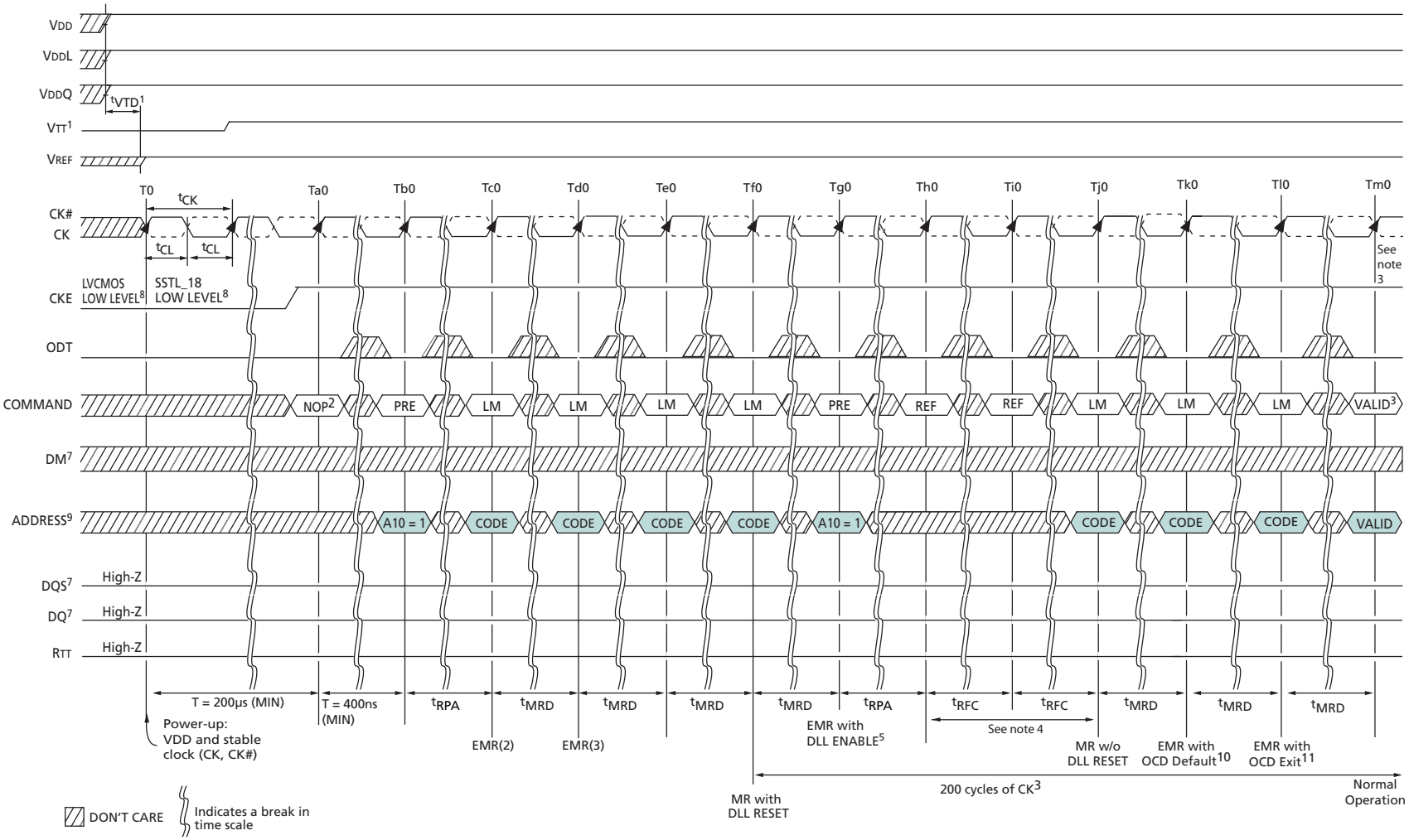
1. Applying power; if CKE is maintained below 0.2 x VDDQ, outputs remain disabled. To guarantee RTT (ODT resistance) is off, VREF must be valid and a low level must be applied to the ODT ball (all other inputs may be undefined, I/Os and outputs must be less than VDDQ during voltage ramp time to avoid DDR2 SDRAM device latch-up). At least one of the following two sets of conditions (A or B) must be met to obtain a stable supply state (stable supply defined as VDD, VDDL, VDDQ, VREF, and VTT are between their minimum and maximum values as stated in Table 20):
   A. (single power source) The VDD voltage ramp from 300mV to VDD (MIN) must take no longer than 200ms; during the VDD voltage ramp, |VDD - VDDQ| ≤ 0.3V. Once supply voltage ramping is complete (when VDDQ crosses VDD (MIN)), Table 20 specifications apply.
      - VDD, VDDL, and VDDQ are driven from a single power converter output
      - VTT is limited to 0.95V MAX
      - VREF tracks VDDQ/2; VREF must be within ±0.3V with respect to VDDQ/2 during supply ramp time
      - VDDQ ≥ VREF at all times
   B. (multiple power sources) VDD ≥ VDDL ≥ VDDQ must be maintained during supply voltage ramping, for both AC and DC levels, until supply voltage ramping completes (VDDQ crosses VDD [MIN]). Once supply voltage ramping is complete, Table 20 specifications apply.
      - Apply VDD and VDDL before or at the same time as VDDQ; VDD/VDDL voltage ramp time must be ≤ 200ms from when VDD ramps from 300mV to VDD (MIN)
      - Apply VDDQ before or at the same time as VTT; the VDDQ voltage ramp time from when VDD (MIN) is achieved to when VDDQ (MIN) is achieved must be ≤ 500ms; while VDD is ramping, current can be supplied from VDD through the device to VDDQ
      - VREF must track VDDQ/2, VREF must be within ±0.3V with respect to VDDQ/2 during supply ramp time; VDDQ ≥ VREF must be met at all times
      - Apply VTT; The VTT voltage ramp time from when VDDQ (MIN) is achieved to when VTT (MIN) is achieved must be no greater than 500ms
2. For a minimum of 200µs after stable power and clock (CK, CK#), apply NOP or DESELECT commands and take CKE HIGH.
3. Wait a minimum of 400ns, then issue a PRECHARGE ALL command.
4. Issue an LOAD MODE command to the EMR(2). (To issue an EMR(2) command, provide LOW to BA0, provide HIGH to BA1.)
5. Issue a LOAD MODE command to the EMR(3). (To issue an EMR(3) command, provide HIGH to BA0 and BA1.)
6. Issue an LOAD MODE command to the EMR to enable DLL. To issue a DLL ENABLE command, provide LOW to BA1 and A0, provide HIGH to BA0. Bits E7, E8, and E9 can be set to "0" or "1"; Micron recommends setting them to "0."
7. Issue a LOAD MODE command for DLL RESET. 200 cycles of clock input is required to lock the DLL. (To issue a DLL RESET, provide HIGH to A8 and provide LOW to BA1, and BA0.) CKE must be HIGH the entire time.
8. Issue PRECHARGE ALL command.
9. Issue two or more REFRESH commands, followed by a dummy WRITE.

10. Issue a LOAD MODE command with LOW to A8 to initialize device operation (i.e., to program operating parameters without resetting the DLL).
11. Issue a LOAD MODE command to the EMR to enable OCD default by setting bits E7, E8, and E9 to "1," and then setting all other desired parameters.
12. Issue a LOAD MODE command to the EMR to enable OCD exit by setting bits E7, E8, and E9 to "0," and then setting all other desired parameters.

The DDR2 SDRAM is now initialized and ready for normal operation 200 clocks after DLL RESET (in step 7).

Figure 7: DDR2 Power-Up and Initialization

Notes appear on page 19



pdf: 09005aef811 7c187, source: 09005aef80b12a05
256MbDDR2_2.fm - Rev. J 11/05 EN

Notes: 1. Applying power; if CKE is maintained below 0.2 x $V_{DD}Q$, outputs remain disabled. To guarantee R_{TT} (ODT resistance) is off, V_{REF} must be valid and a low level must be applied to the ODT ball (all other inputs may be undefined, I/Os and outputs must be less than $V_{DD}Q$ during voltage ramp time to avoid DDR2 SDRAM device latch-up). At least one of the following two sets of conditions (A or B) must be met to obtain a stable supply state (stable supply defined as V_{DD}, $V_{DD}L$, $V_{DD}Q$, V_{REF}, and V_{TT} are between their minimum and maximum values as stated in Table 20):

   A. (single power source) The V_{DD} voltage ramp from 300mV to V_{DD} (MIN) must take no longer than 200ms; during the V_{DD} voltage ramp, $|V_{DD} - V_{DD}Q| \leq 0.3V$. Once supply voltage ramping is complete (when $V_{DD}Q$ crosses V_{DD} (MIN)), Table 20 specifications apply.
      - V_{DD}, $V_{DD}L$, and $V_{DD}Q$ are driven from a single power converter output
      - V_{TT} is limited to 0.95V MAX
      - V_{REF} tracks $V_{DD}Q/2$; V_{REF} must be within ±0.3V with respect to $V_{DD}Q/2$ during supply ramp time
      - $V_{DD}Q \geq V_{REF}$ at all times

   B. (multiple power sources) $V_{DD} \geq V_{DD}L \geq V_{DD}Q$ must be maintained during supply voltage ramping, for both AC and DC levels, until supply voltage ramping completes ($V_{DD}Q$ crosses V_{DD} [MIN]). Once supply voltage ramping is complete, Table 20 specifications apply.
      - Apply V_{DD} and $V_{DD}L$ before or at the same time as $V_{DD}Q$; $V_{DD}/V_{DD}L$ voltage ramp time must be ≤ 200ms from when V_{DD} ramps from 300mV to V_{DD} (MIN)
      - Apply $V_{DD}Q$ before or at the same time as V_{TT}; the $V_{DD}Q$ voltage ramp time from when V_{DD} (MIN) is achieved to when $V_{DD}Q$ (MIN) is achieved must be ≤ 500ms; while V_{DD} is ramping, current can be supplied from V_{DD} through the device to $V_{DD}Q$
      - V_{REF} must track $V_{DD}Q/2$, V_{REF} must be within ±0.3V with respect to $V_{DD}Q/2$ during supply ramp time; $V_{DD}Q \geq V_{REF}$ must be met at all times
      - Apply V_{TT}; The V_{TT} voltage ramp time from when $V_{DD}Q$ (MIN) is achieved to when V_{TT} (MIN) is achieved must be no greater than 500ms

2. For a minimum of 200µs after stable power and clock (CK, CK#), apply NOP or DESELECT commands and take CKE HIGH.
3. Wait a minimum of 400ns, then issue a PRECHARGE ALL command.
4. Issue an LOAD MODE command to the EMR(2). (To issue an EMR(2) command, provide LOW to BA0, provide HIGH to BA1.)
5. Issue a LOAD MODE command to the EMR(3). (To issue an EMR(3) command, provide HIGH to BA0 and BA1.)
6. Issue an LOAD MODE command to the EMR to enable DLL. To issue a DLL ENABLE command, provide LOW to BA1 and A0, provide HIGH to BA0. Bits E7, E8, and E9 can be set to "0" or "1"; Micron recommends setting them to "0."
7. Issue a LOAD MODE command for DLL RESET. 200 cycles of clock input is required to lock the DLL. (To issue a DLL RESET, provide HIGH to A8 and provide LOW to BA1, and BA0.) CKE must be HIGH the entire time.
8. Issue PRECHARGE ALL command.
9. Issue two or more REFRESH commands, followed by a dummy WRITE.
10. Issue a LOAD MODE command with LOW to A8 to initialize device operation (i.e., to program operating parameters without resetting the DLL).
11. Issue a LOAD MODE command to the EMR to enable OCD default by setting bits E7, E8, and E9 to "1," and then setting all other desired parameters.
12. Issue a LOAD MODE command to the EMR to enable OCD exit by setting bits E7, E8, and E9 to "0," and then setting all other desired parameters.

Mode Register (MR)

The mode register is used to define the specific mode of operation of the DDR2 SDRAM. This definition includes the selection of a burst length, burst type, CL, operating mode, DLL RESET, write recovery, and power-down mode, as shown in Figure 8. Contents of the mode register can be altered by re-executing the LOAD MODE (LM) command. If the user chooses to modify only a subset of the MR variables, all variables (M0–M14) must be programmed when the command is issued.

The mode register is programmed via the LM command (bits BA1–BA0 = 0, 0) and other bits (M12–M0) will retain the stored information until it is programmed again or the device loses power (except for bit M8, which is self-clearing). Reprogramming the mode register will not alter the contents of the memory array, provided it is performed correctly.

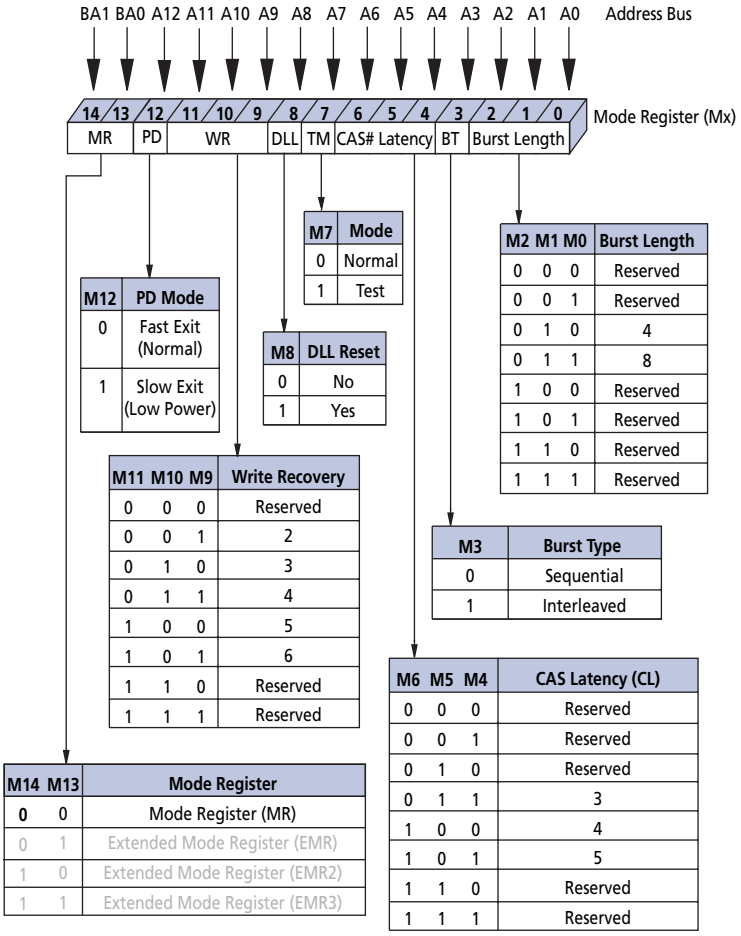
The LM command can only be issued (or reissued) when all banks are in the precharged state (idle state) and no bursts are in progress. The controller must wait the specified time ^{t}MRD before initiating any subsequent operations such as an ACTIVE command. Violating either of these requirements will result in unspecified operation.

Burst Length

Burst length is defined by bits M0–M3, as shown in Figure 8. Read and write accesses to the DDR2 SDRAM are burst-oriented, with the burst length being programmable to either four or eight. The burst length determines the maximum number of column locations that can be accessed for a given READ or WRITE command.

When a READ or WRITE command is issued, a block of columns equal to the burst length is effectively selected. All accesses for that burst take place within this block, meaning that the burst will wrap within the block if a boundary is reached. The block is uniquely selected by A2–A*i* when BL = 4 and by A3–A*i* when BL = 8 (where A*i* is the most significant column address bit for a given configuration). The remaining (least significant) address bit(s) is (are) used to select the starting location within the block. The programmed burst length applies to both READ and WRITE bursts.

Figure 8: Mode Register (MR) Definition



Burst Type

Accesses within a given burst may be programmed to be either sequential or interleaved. The burst type is selected via bit M3, as shown in Figure 8. The ordering of accesses within a burst is determined by the burst length, the burst type, and the starting column address, as shown in Table 4. DDR2 SDRAM supports 4-bit burst mode and 8-bit burst mode only. For 8-bit burst mode, full interleave address ordering is supported; however, sequential address ordering is nibble-based.

Table 4: Burst Definition

Burst Length	Starting Column Address (A2, A1, A0)	Order of Accesses Within a Burst	
		Burst Type = Sequential	Burst Type = Interleaved
4	0 0	0,1,2,3	0,1,2,3
	0 1	1,2,3,0	1,0,3,2
	1 0	2,3,0,1	2,3,0,1
	1 1	3,0,1,2	3,2,1,0
8	0 0 0	0,1,2,3,4,5,6,7	0,1,2,3,4,5,6,7
	0 0 1	1,2,3,0,5,6,7,4	1,0,3,2,5,4,7,6
	0 1 0	2,3,0,1,6,7,4,5	2,3,0,1,6,7,4,5
	0 1 1	3,0,1,2,7,4,5,6	3,2,1,0,7,6,5,4
	1 0 0	4,5,6,7,0,1,2,3	4,5,6,7,0,1,2,3
	1 0 1	5,6,7,4,1,2,3,0	5,4,7,6,1,0,3,2
	1 1 0	6,7,4,5,2,3,0,1	6,7,4,5,2,3,0,1
	1 1 1	7,4,5,6,3,0,1,2	7,6,5,4,3,2,1,0

Operating Mode

The normal operating mode is selected by issuing a command with bit M7 set to "0," and all other bits set to the desired values, as shown in Figure 8 on page 21. When bit M7 is "1," no other bits of the mode register are programmed. Programming bit M7 to "1" places the DDR2 SDRAM into a test mode that is only used by the manufacturer and should *not* be used. No operation or functionality is guaranteed if M7 bit is '1.'

DLL RESET

DLL RESET is defined by bit M8, as shown in Figure 8 on page 21. Programming bit M8 to "1" will activate the DLL RESET function. Bit M8 is self-clearing, meaning it returns back to a value of "0" after the DLL RESET function has been issued.

Anytime the DLL RESET function is used, 200 clock cycles must occur before a READ command can be issued to allow time for the internal clock to be synchronized with the external clock. Failing to wait for synchronization to occur may result in a violation of the ^{t}AC or ^{t}DQSCK parameters.

Write Recovery

Write recovery (WR) time is defined by bits M9–M11, as shown in Figure 8 on page 21. The WR register is used by the DDR2 SDRAM during WRITE with auto precharge operation. During WRITE with auto precharge operation, the DDR2 SDRAM delays the internal auto precharge operation by WR clocks (programmed in bits M9–M11) from the last data burst. An example of WRITE with auto precharge is shown in Figure 61 on page 23.

WR values of 2, 3, 4, 5, or 6 clocks may be used for programming bits M9–M11. The user is required to program the value of WR, which is calculated by dividing ^{t}WR (in ns) by ^{t}CK (in ns) and rounding up a noninteger value to the next integer; WR [cycles] = ^{t}WR [ns] / ^{t}CK [ns]. Reserved states should not be used as unknown operation or incompatibility with future versions may result.

Power-Down Mode

Active power-down (PD) mode is defined by bit M12, as shown in Figure 8 on page 21. PD mode allows the user to determine the active power-down mode, which determines performance versus power savings. PD mode bit M12 does not apply to prechargePD mode.

When bit M12 = 0, standard active PD mode or "fast-exit" active PD mode is enabled. The ^{t}XARD parameter is used for fast-exit active PD exit timing. The DLL is expected to be enabled and running during this mode.

When bit M12 = 1, a lower-power active PD mode or "slow-exit" active PD mode is enabled. The ^{t}XARDS parameter is used for slow-exit active PD exit timing. The DLL can be enabled, but "frozen" during active PD mode since the exit-to-READ command timing is relaxed. The power difference expected between PD normal and PD low-power mode is defined in the IDD table.

CAS Latency (CL)

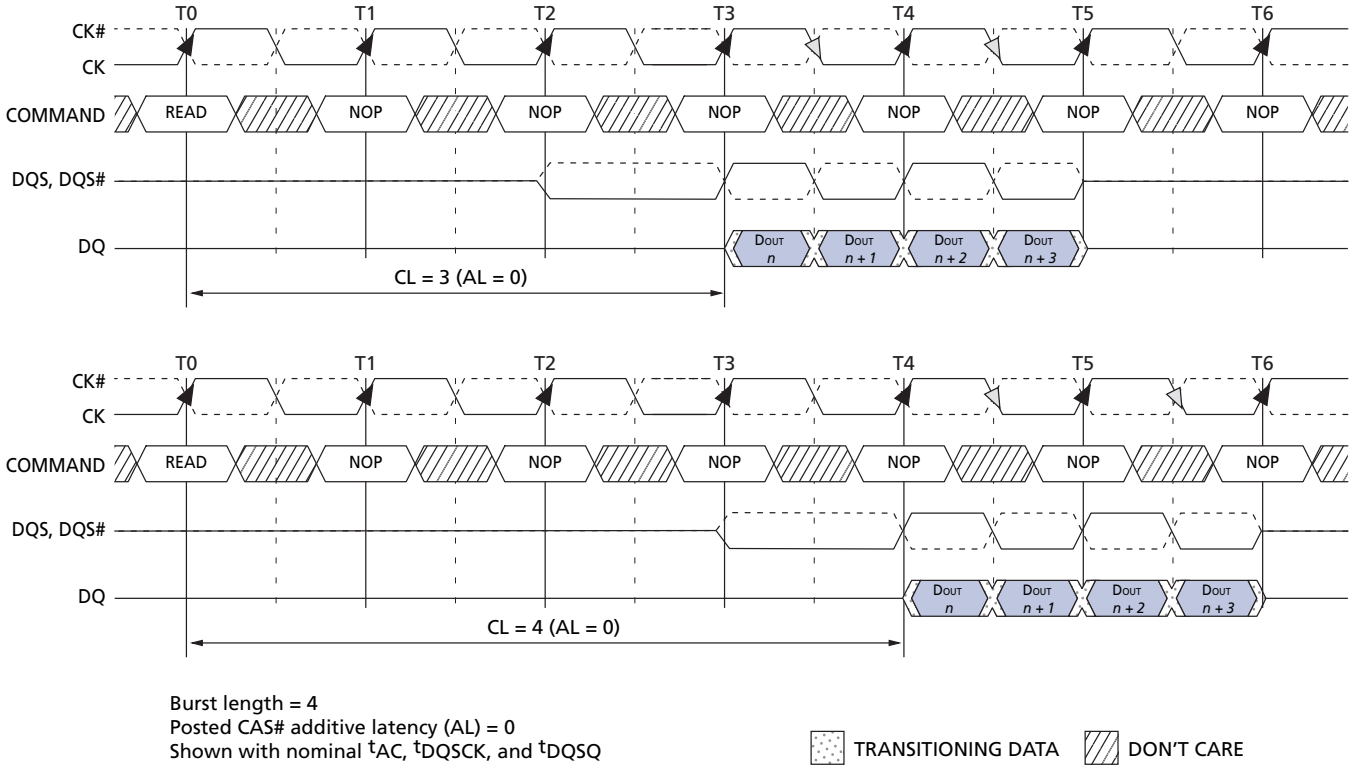
The CAS latency (CL) is defined by bits M4–M6, as shown in Figure 8 on page 21. CL is the delay, in clock cycles, between the registration of a READ command and the availability of the first bit of output data. The CL can be set to 3, 4, or 5 clocks, depending speed grade option being used. CL of 6 clocks is a JEDEC-optional feature and may be enabled in future speed grades.

DDR2 SDRAM does not support any half-clock latencies. Reserved states should not be used as unknown operation or incompatibility with future versions may result.

DDR2 SDRAM also supports a feature called posted CAS additive latency (AL). This feature allows the READ command to be issued prior to ^{t}RCD (MIN) by delaying the internal command to the DDR2 SDRAM by AL clocks. The AL feature is described in more detail in the "Extended Mode Register (EMR)" on page 24 and "Operating Mode" on page 22.

Examples of CL = 3 and CL = 4 are shown in Figure 9; both assume AL = 0. If a READ command is registered at clock edge *n*, and the CL is *m* clocks, the data will be available nominally coincident with clock edge *n* + *m* (this assumes AL = 0).

Figure 9: CAS Latency (CL)

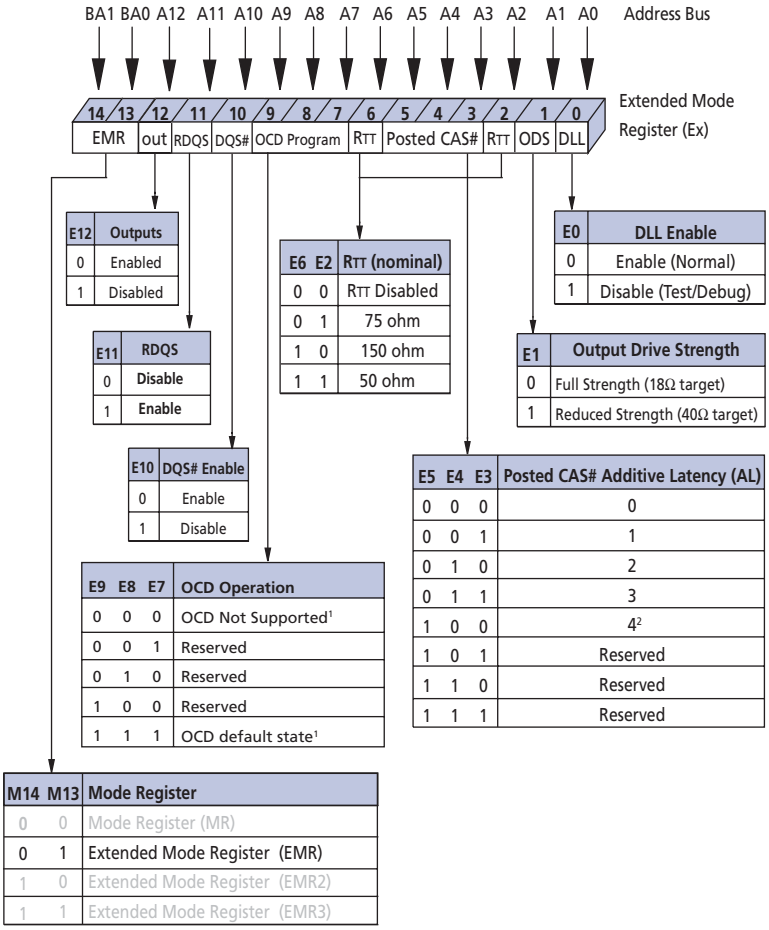


Extended Mode Register (EMR)

The extended mode register controls functions beyond those controlled by the mode register; these additional functions are DLL enable/disable, output drive strength, on-die termination (ODT) (RTT), posted AL, off-chip driver impedance calibration (OCD), DQS# enable/disable, RDQS/RDQS# enable/disable, and output disable/enable. These functions are controlled via the bits shown in Figure 10. The EMR is programmed via the LOAD MODE (LM) command and will retain the stored information until it is programmed again or the device loses power. Reprogramming the EMR will not alter the contents of the memory array, provided it is performed correctly.

The EMR must be loaded when all banks are idle and no bursts are in progress, and the controller must wait the specified time tMRD before initiating any subsequent operation. Violating either of these requirements could result in unspecified operation.

Figure 10: Extended Mode Register Definition



Notes: 1. During initialization, all three bits must be set to '1' for OCD Default State, then must be set to '0' before initialization is finished, as detailed in the initialization procedure.
2. Not supported when ^{t}CK > 667 MHz.

DLL Enable/Disable

The DLL may be enabled or disabled by programming bit E0 during the LM command, as shown in Figure 10 on page 25. The DLL must be enabled for normal operation. DLL enable is required during power-up initialization and upon returning to normal operation after having disabled the DLL for the purpose of debugging or evaluation. Enabling the DLL should always be followed by resetting the DLL using an LM command.

The DLL is automatically disabled when entering SELF REFRESH operation and is automatically re-enabled and reset upon exit of SELF REFRESH operation.

Any time the DLL is enabled (and subsequently reset), 200 clock cycles must occur before a READ command can be issued, to allow time for the internal clock to synchronize with the external clock. Failing to wait for synchronization to occur may result in a violation of the ^{t}AC or ^{t}DQSCK parameters.

Output Drive Strength

The output drive strength is defined by bit E1, as shown in Figure 10 on page 25. The normal drive strength for all outputs are specified to be SSTL_18. Programming bit E1 = 0 selects normal (full strength) drive strength for all outputs. Selecting a reduced drive strength option (E1 = 1) will reduce all outputs to approximately 60 percent of the SSTL_18 drive strength. This option is intended for the support of lighter load and/or point-to-point environments.

DQS# Enable/Disable

The DQS# ball is enabled by bit E10. When E10 = 0, DQS# is the complement of the differential data strobe pair DQS/DQS#. When disabled (E10 = 1), DQS is used in a single-ended mode and the DQS# ball is disabled. When disabled, DQS# should be left floating. This function is also used to enable/disable RDQS#. If RDQS is enabled (E11 = 1) and DQS# is enabled (E10 = 0), then both DQS# and RDQS# will be enabled.

RDQS Enable/Disable

The RDQS ball is enabled by bit E11, as shown in Figure 10 on page 25. This feature is only applicable to the x8 configuration. When enabled (E11 = 1), RDQS is identical in function and timing to data strobe DQS during a READ. During a WRITE operation, RDQS is ignored by the DDR2 SDRAM.

Output Enable/Disable

The OUTPUT ENABLE function is defined by bit E12, as shown in Figure 10 on page 25. When enabled (E12 = 0), all outputs (DQs, DQS, DQS#, RDQS, RDQS#) function normally. When disabled (E12 = 1), all DDR2 SDRAM outputs (DQs, DQS, DQS#, RDQS, RDQS#) are disabled, thus removing output buffer current. The output disable feature is intended to be used during IDD characterization of read current.

On-Die Termination (ODT)

ODT effective resistance, RTT (EFF), is defined by bits E2 and E6 of the EMR, as shown in Figure 10 on page 25. The ODT feature is designed to improve signal integrity of the memory channel by allowing the DDR2 SDRAM controller to independently turn on/off ODT for any or all devices. RTT effective resistance values of 50Ω, 75Ω, and 150Ω are selectable and apply to each DQ, DQS/DQS#, RDQS/RDQS#, UDQS/UDQS#, LDQS/LDQS#, DM, and UDM/LDM signals. Bits (E6, E2) determine what ODT resistance is enabled by turning on/off "sw1," "sw2," or "sw3." The ODT effective resistance value is selected by enabling switch "sw1," which enables all R1 values that are 150Ω each, enabling an effective resistance of 75Ω (RTT2(EFF) = R2/2). Similarly, if "sw2" is enabled, all R2 values that are 300Ω each, enable an effective ODT resistance of 150Ω (RTT2(EFF) = R2/2). Switch "sw3" enables R1 values of 100Ω, enabling effective resistance of 50Ω. Reserved states should not be used, as unknown operation or incompatibility with future versions may result.

The ODT control ball is used to determine when RTT(EFF) is turned on and off, assuming ODT has been enabled via bits E2 and E6 of the EMR. The ODT feature and ODT input ball are only used during active, active power-down (both fast-exit and slow-exit modes), and precharge power-down modes of operation. ODT must be turned off prior to entering self refresh. During power-up and initialization of the DDR2 SDRAM, ODT should be disabled until issueing the EMR command to enable the ODT feature, at which point the

ODT ball will determine the RTT(EFF) value. Any time the EMR enables the ODT function, ODT may not be driven HIGH until eight clocks after the EMR has been enabled. See "ODT Timing" section for ODT timing diagrams.

Off-Chip Driver (OCD) Impedance Calibration

The Off-Chip Driver function is no longer supported and must be set to the default state. See "Initialization" on page 16 for proper setting of OCD defaults.

Posted CAS Additive Latency (AL)

Posted CAS additive latency (AL) is supported to make the command and data bus efficient for sustainable bandwidths in DDR2 SDRAM. Bits E3–E5 define the value of AL, as shown in Figure 10 on page 25. Bits E3–E5 allow the user to program the DDR2 SDRAM with an inverse AL of 0, 1, 2, 3, or 4 clocks. Reserved states should not be used as unknown operation or incompatibility with future versions may result.

In this operation, the DDR2 SDRAM allows a READ or WRITE command to be issued prior to ^{t}RCD (MIN) with the requirement that AL ≤ ^{t}RCD (MIN). A typical application using this feature would set AL = ^{t}RCD (MIN) - 1 x ^{t}CK. The READ or WRITE command is held for the time of the AL before it is issued internally to the DDR2 SDRAM device. RL is controlled by the sum of AL and CL; RL = AL + CL. Write latency (WL) is equal to RL minus one clock; WL = AL + CL - 1 x ^{t}CK. An example of RL is shown in Figure 11. An example of a WL is shown in Figure 12 on page 27.

Figure 11: READ Latency

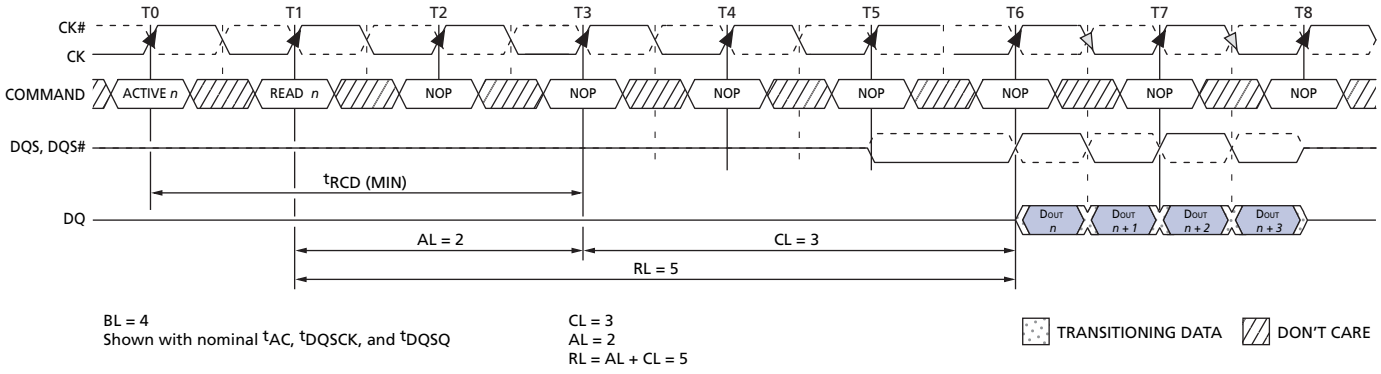
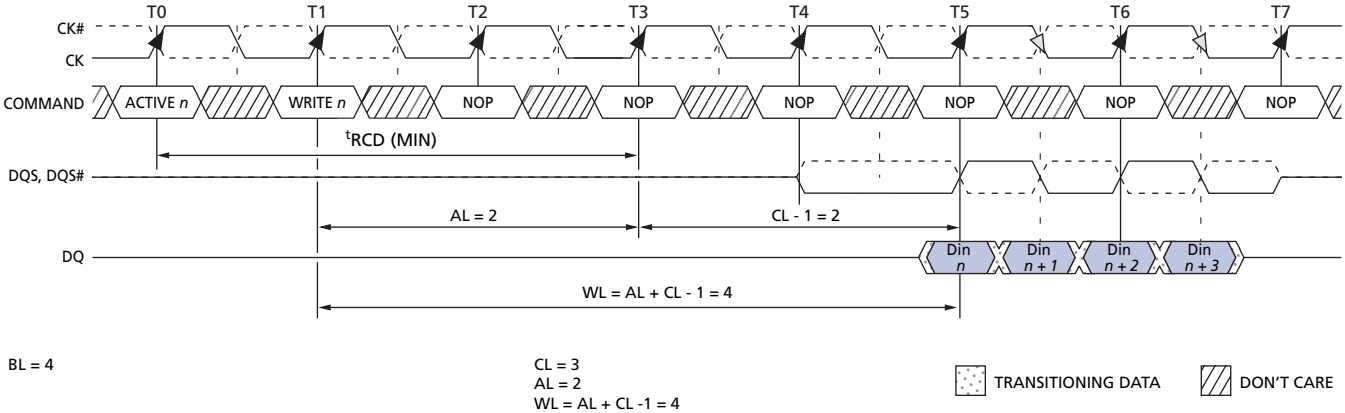


Figure 12: WRITE Latency



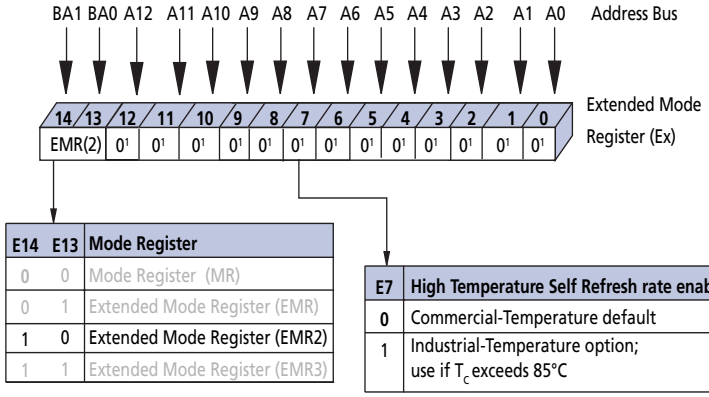
Extended Mode Register 2

The extended mode register 2 (EMR2) controls functions beyond those controlled by the mode register. Currently all bits in EMR2 are reserved for the commercial offering, as shown in Figure 13. The EMR2 is programmed via the LM command and will retain the stored information until it is programmed again or the device loses power. Reprogramming the EMR will not alter the contents of the memory array, provided it is performed correctly.

Bit E7 (A7) must be programmed to provide a faster refresh rate on IT devices if the TCASE exceeds 85°C.

EMR2 must be loaded when all banks are idle and no bursts are in progress, and the controller must wait the specified time ^{t}MRD before initiating any subsequent operation. Violating either of these requirements could result in unspecified operation.

Figure 13: Extended Mode Register 2 (EMR2) Definition



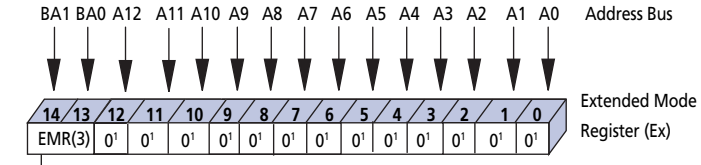
Notes: 1. E12 (A12)–E8 and E6(A6)–E0 (A0) are reserved for future use and must all be programmed to "0."

Extended Mode Register 3

The extended mode register 3 (EMR3) controls functions beyond those controlled by the mode register. Currently, all bits in EMR3 are reserved, as shown in Figure 14. The EMR3 is programmed via the LM command and will retain the stored information until it is programmed again or the device loses power. Reprogramming the EMR will not alter the contents of the memory array, provided it is performed correctly.

EMR3 must be loaded when all banks are idle and no bursts are in progress, and the controller must wait the specified time ^{t}MRD before initiating any subsequent operation. Violating either of these requirements could result in unspecified operation.

Figure 14: Extended Mode Register 3 (EMR3) Definition



E14	E13	Mode Register
0	0	Mode Register (MR)
0	1	Extended Mode Register (EMR)
1	0	Extended Mode Register (EMR2)
1	1	Extended Mode Register (EMR3)

Notes: 1. E12 (A12)–E8 and E6(A6)–E0 (A0) are reserved for future use and must all be programmed to "0."

Command Truth Tables

The following tables provide a quick reference of DDR2 SDRAM available commands, including CKE power-down modes, and bank-to-bank commands.

Table 5: Truth Table – DDR2 Commands

Notes: 1, 5, and 6 apply to all

Function	CKE		CS#	RAS#	CAS#	WE#	BA1 BA0	A12 A11	A10	A9–A0	Notes
	Previous Cycle	Current Cycle									
LOAD MODE	H	H	L	L	L	L	BA	OP Code			2
REFRESH	H	H	L	L	L	H	X	X	X	X	
SELF REFRESH Entry	H	L	L	L	L	H	X	X	X	X	
SELF REFRESH Exit	L	H	H	X	X	X	X	X	X	X	7
			L	H	H	H					
Single bank precharge	H	H	L	L	H	L	BA	X	L	X	2
All banks PRECHARGE	H	H	L	L	H	L	X	X	H	X	
Bank activate	H	H	L	L	H	H	BA	Row Address			
WRITE	H	H	L	H	L	L	BA	Column Address	L	Column Address	2, 3
WRITE with auto precharge	H	H	L	H	L	L	BA	Column Address	H	Column Address	2, 3
READ	H	H	L	H	L	H	BA	Column Address	L	Column Address	2, 3
READ with auto precharge	H	H	L	H	L	H	BA	Column Address	H	Column Address	2, 3
NO OPERATION	H	X	L	H	H	H	X	X	X	X	
Device DESELECT	H	X	H	X	X	X	X	X	X	X	
POWER-DOWN entry	H	L	H	X	X	X	X	X	X	X	4
			L	H	H	H					
POWER-DOWN exit	L	H	H	X	X	X	X	X	X	X	4
			L	H	H	H					

Notes:
1. All DDR2 SDRAM commands are defined by states of CS#, RAS#, CAS#, WE#, and CKE at the rising edge of the clock.
2. Bank addresses (BA) BA0–BA12 determine which bank is to be operated upon. BA during a LM command selects which mode register is programmed.
3. Burst reads or writes at BL = 4 cannot be terminated or interrupted. See Figure 43 and Figure 57 for other restrictions and details.
4. The power-down mode does not perform any REFRESH operations. The duration of power-down is therefore limited by the refresh requirements outlined in the AC parametric section.
5. The state of ODT does not affect the states described in this table. The ODT function is not available during self refresh. See "On-Die Termination (ODT)" on page 12 for details.
6. "X" means "H or L" (but a defined logic level).
7. Self refresh exit is asynchronous.

Table 6: Truth Table – Current State Bank *n* - Command to Bank *n*

Notes: 1–6; notes appear below and on next page

Current State	CS#	RAS#	CAS#	WE#	Command/Action	Notes
Any	H	X	X	X	DESELECT (NOP/continue previous operation)	
	L	H	H	H	NO OPERATION (NOP/continue previous operation)	
Idle	L	L	H	H	ACTIVE (select and activate row)	
	L	L	L	H	REFRESH	7
	L	L	L	L	LOAD MODE	7
Row Active	L	H	L	H	READ (select column and start READ burst)	9
	L	H	L	L	WRITE (select column and start WRITE burst)	9
	L	L	H	L	PRECHARGE (deactivate row in bank or banks)	8
Read (Auto-Precharge Disabled	L	H	L	H	READ (select column and start new READ burst)	9
	L	H	L	L	WRITE (select column and start WRITE burst)	9, 10
	L	L	H	L	PRECHARGE (start PRECHARGE)	8
Write (Auto-Precharge Disabled)	L	H	L	H	READ (select column and start READ burst)	9
	L	H	L	L	WRITE (select column and start new WRITE burst)	9
	L	L	H	L	PRECHARGE (start PRECHARGE)	8

Notes:
1. This table applies when CKE*n* - 1 was HIGH and CKE*n* is HIGH and after ^{t}XSNR has been met (if the previous state was self refresh).
2. This table is bank-specific, except where noted (i.e., the current state is for a specific bank and the commands shown are those allowed to be issued to that bank when in that state). Exceptions are covered in the notes below.
3. Current state definitions:
   - **Idle**: The bank has been precharged, ^{t}RP has been met, and any READ burst is complete.
   - **Row active**: A row in the bank has been activated, and ^{t}RCD has been met. No data bursts/accesses and no register accesses are in progress.
   - **Read**: A READ burst has been initiated, with auto precharge disabled, and has not yet terminated.
   - **Write**: A WRITE burst has been initiated, with auto precharge disabled, and has not yet terminated.
4. The following states must not be interrupted by a command issued to the same bank. Issue DESELECT or NOP commands, or allowable commands to the other bank, on any clock edge occurring during these states. Allowable commands to the other bank are determined by its current state and this table, and according to Table 7.
   - **Precharging**: Starts with registration of a PRECHARGE command and ends when ^{t}RP is met. Once ^{t}RP is met, the bank will be in the idle state.
   - **Row activating**: Starts with registration of an ACTIVE command and ends when ^{t}RCD is met. Once ^{t}RCD is met, the bank will be in the "row active" state.
   - **Read with auto precharge enabled**: Starts with registration of a READ command with auto precharge enabled and ends when ^{t}RP has been met. Once ^{t}RP is met, the bank will be in the idle state.
   - **Write with auto precharge enabled**: Starts with registration of a WRITE command with auto precharge enabled and ends when ^{t}RP has been met. Once ^{t}RP is met, the bank will be in the idle state.
5. The following states must not be interrupted by any executable command; DESELECT or NOP commands must be applied on each positive clock edge during these states.
   - **Refreshing**: Starts with registration of a REFRESH command and ends when ^{t}RFC is met. Once ^{t}RFC is met, the DDR2 SDRAM will be in the all banks idle state.

- **Accessing mode register**: Starts with registration of an LM command and ends when ^{t}MRD has been met. Once ^{t}MRD is met, the DDR2 SDRAM will be in the all banks idle state.
- **Precharging all**: Starts with registration of a PRECHARGE ALL command and ends when ^{t}RP is met. Once ^{t}RP is met, all banks will be in the idle state.

6. All states and sequences not shown are illegal or reserved.
7. Not bank-specific; requires that all banks are idle, and bursts are not in progress.
8. May or may not be bank-specific; if multiple banks are to be precharged, each must be in a valid state for precharging.
9. READs or WRITEs listed in the Command/Action column include READs or WRITEs with auto precharge enabled and READs or WRITEs with auto precharge disabled.
10. A WRITE command may be applied after the completion of the READ burst.

Table 7: Truth Table – Current State Bank *n* - Command to Bank *m*
Notes: 1–6; notes appear below and on next page

Current State	CS#	RAS#	CAS#	WE#	Command/Action	Notes
Any	H	X	X	X	DESELECT (NOP/continue previous operation)	
	L	H	H	H	NO OPERATION (NOP/continue previous operation)	
Idle	X	X	X	X	Any Command Otherwise Allowed to Bank m	
Row Activating, Active, or Precharging	L	L	H	H	ACTIVE (select and activate row)	
	L	H	L	H	READ (select column and start READ burst)	7
	L	H	L	L	WRITE (select column and start WRITE burst)	7
	L	L	H	L	PRECHARGE	
Read (auto precharge disabled	L	L	H	H	ACTIVE (select and activate row)	
	L	H	L	H	READ (select column and start new READ burst)	7
	L	H	L	L	WRITE (select column and start WRITE burst)	7, 9
	L	L	H	L	PRECHARGE	
Write (auto precharge disabled.)	L	L	H	H	ACTIVE (select and activate row)	
	L	H	L	H	READ (select column and start READ burst)	7, 8
	L	H	L	L	WRITE (select column and start new WRITE burst)	7
	L	L	H	L	PRECHARGE	
Read (with auto-precharge)	L	L	H	H	ACTIVE (select and activate row)	
	L	H	L	H	READ (select column and start new READ burst)	7, 3
	L	H	L	L	WRITE (select column and start WRITE burst)	7, 9, 3
	L	L	H	L	PRECHARGE	
Write (with auto-precharge)	L	L	H	H	ACTIVE (select and activate row)	
	L	H	L	H	READ (select column and start READ burst)	7, 3
	L	H	L	L	WRITE (select column and start new WRITE burst)	7, 3
	L	L	H	L	PRECHARGE	

Notes: 1. This table applies when CKE*n* - 1 was HIGH and CKE*n* is HIGH (see Truth Table 2) and after ^{t}XSNR has been met (if the previous state was self refresh).

2. This table describes alternate bank operation, except where noted (i.e., the current state is for bank *n* and the commands shown are those allowed to be issued to bank *m*, assuming that bank *m* is in such a state that the given command is allowable). Exceptions are covered in the notes below.

3. Current state definitions:
   - **Idle**: The bank has been precharged, and ^{t}RP has been met, and any READ burst is complete.
   - **Row active**: A row in the bank has been activated and ^{t}RCD has been met. No data bursts/accesses and no register accesses are in progress.
   - **Read**: A READ burst has been initiated with auto precharge disabled, and has not yet terminated.
   - **Write**: A WRITE burst has been initiated, with auto precharge disabled, and has not yet terminated.
   - **Read with auto precharge enabled/write with auto precharge enabled**: The read with auto precharge enabled or write with auto precharge enabled states can each be broken into two parts: the access period and the precharge period. For read with auto precharge, the precharge period is defined as if the same burst was executed with auto precharge disabled and then followed with the earliest possible PRECHARGE command that still accesses all of the data in the burst. For write with auto precharge, the precharge period begins when ^{t}WR ends, with ^{t}WR measured as if auto precharge was disabled. The access period starts with registration of the command and ends where the precharge period (or ^{t}RP) begins. This device supports concurrent auto precharge such that when a read with auto precharge is enabled or a write with auto pre-

charge is enabled any command to other banks is allowed, as long as that command does not interrupt the read or write data transfer already in process. In either case, all other related limitations apply (e.g., contention between read data and write data must be avoided).

The minimum delay from a READ or WRITE command with auto precharge enabled to a command to a different bank is summarized in Table 8:

Table 8: Minimum Delay with Auto Precharge Enabled

From Command (Bank *n*)	To Command (Bank *m*)	Minimum Delay (With Concurrent Auto Precharge)	Units
WRITE with auto precharge	READ or READ w/auto precharge	(CL - 1) + (BL / 2) + ^{t}WTR	^{t}CK
	WRITE or WRITE w/auto precharge	(BL / 2)	^{t}CK
	PRECHARGE or ACTIVE	1	^{t}CK
READ with auto precharge	READ or READ w/auto precharge	(BL / 2)	^{t}CK
	WRITE or WRITE w/auto precharge	(BL / 2) + 2	^{t}CK
	PRECHARGE or ACTIVE	1	^{t}CK

4. REFRESH and LM commands may only be issued when all banks are idle.
5. Not used.
6. All states and sequences not shown are illegal or reserved.
7. READs or WRITEs listed in the Command/Action column include READs or WRITEs with auto precharge enabled and READs or WRITEs with auto precharge disabled.
8. Requires appropriate DM.
9. A WRITE command may be applied after the completion of the READ burst.
10. The number of clock cycles required to meet ^{t}WTR is either 2 or ^{t}WTR/^{t}CK, whichever is greater.

DESELECT, NOP, and LOAD MODE Commands

DESELECT

The DESELECT function (CS# HIGH) prevents new commands from being executed by the DDR2 SDRAM. The DDR2 SDRAM is effectively deselected. Operations already in progress are not affected.

NO OPERATION (NOP)

The NO OPERATION (NOP) command is used to instruct the selected DDR2 SDRAM to perform a NOP (CS# is LOW; RAS#, CAS#, and WE are HIGH). This prevents unwanted commands from being registered during idle or wait states. Operations already in progress are not affected.

LOAD MODE (LM)

The mode registers are loaded via inputs BA1–BA0 and A12–A0 for x4 and x8, and A12–A0 for x16 configurations. BA1–BA0 determine which mode register will be programmed. See "Mode Register (MR)" on page 7. The LM command can only be issued when all banks are idle, and a subsequent executable command cannot be issued until ^{t}MRD is met.

Bank/Row Activation

ACTIVE Command

The ACTIVE command is used to open (or activate) a row in a particular bank for a subsequent access. The value on the BA1–BA0 inputs selects the bank, and the address provided on inputs (A12–A0 for x4 and x8, and A12–A0 for x16) selects the row. This row remains active (or open) for accesses until a PRECHARGE command is issued to that bank. A PRECHARGE command must be issued before opening a different row in the same bank.

ACTIVE Operation

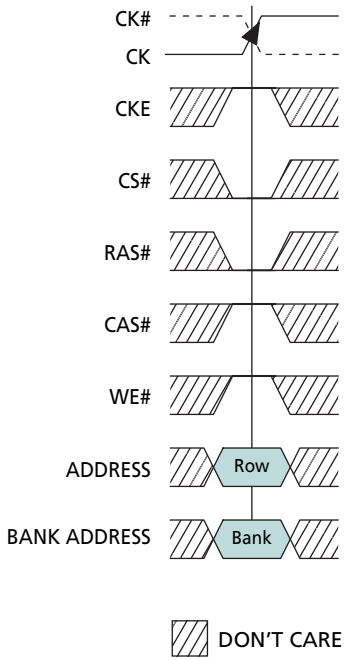
Before any READ or WRITE commands can be issued to a bank within the DDR2 SDRAM, a row in that bank must be opened (activated), even when additive latency is used. This is accomplished via the ACTIVE command, which selects both the bank and the row to be activated, as shown in Figure 15 on page 36.

After a row is opened with an ACTIVE command, a READ or WRITE command may be issued to that row, subject to the ^{t}RCD specification. ^{t}RCD (MIN) should be divided by the clock period and rounded up to the next whole number to determine the earliest clock edge after the ACTIVE command on which a READ or WRITE command can be entered. The same procedure is used to convert other specification limits from time units to clock cycles. For example, a ^{t}RCD (MIN) specification of 20ns with a 266 MHz clock (^{t}CK = 3.75ns) results in 5.3 clocks, rounded up to 6. This is reflected in Figure 17 on page 38, which covers any case where 5 < ^{t}RCD (MIN) / ^{t}CK ≤ 6. Figure 17 also shows the case for ^{t}RRD where 2 < ^{t}RRD (MIN) / ^{t}CK ≤ 3.

A subsequent ACTIVE command to a different row in the same bank can only be issued after the previous active row has been closed (precharged). The minimum time interval between successive ACTIVE commands to the same bank is defined by ^{t}RC.

A subsequent ACTIVE command to another bank can be issued while the first bank is being accessed, which results in a reduction of total row-access overhead. The minimum time interval between successive ACTIVE commands to different banks is defined by ^{t}RRD.

Figure 15: ACTIVE Command



READs

READ Command

The READ command is used to initiate a burst read access to an active row. The value on the BA1–BA0 inputs selects the bank, and the address provided on inputs A0–*i* (where i = A9 for x16, A9 for x8, or A9, A11 for x4) selects the starting column location. The value on input A10 determines whether or not auto precharge is used. If auto precharge is selected, the row being accessed will be precharged at the end of the READ burst; if auto precharge is not selected, the row will remain open for subsequent accesses.

READ Operation

READ bursts are initiated with a READ command, as shown in Figure 16 on page 38. The starting column and bank addresses are provided with the READ command and auto precharge is either enabled or disabled for that burst access. If auto precharge is enabled, the row being accessed is automatically precharged at the completion of the burst. If auto precharge is disabled, the row will be left open after the completion of the burst.

During READ bursts, the valid data-out element from the starting column address will be available READ latency (RL) clocks later. RL is defined as the sum of AL and CL; RL = AL + CL. The value for AL and CL are programmable via the MR and EMR commands, respectively. Each subsequent data-out element will be valid nominally at the next positive or negative clock edge (i.e., at the next crossing of CK and CK#). Figure 18 on page 39 shows examples of RL based on different AL and CL settings.

DQS/DQS# is driven by the DDR2 SDRAM along with output data. The initial LOW state on DQS and HIGH state on DQS# is known as the read preamble (^{t}RPRE). The LOW state on DQS and HIGH state on DQS# coincident with the last data-out element is known as the read postamble (^{t}RPST).

Upon completion of a burst, assuming no other commands have been initiated, the DQ will go High-Z. A detailed explanation of ^{t}DQSQ (valid data-out skew), ^{t}QH (data-out window hold), the valid data window are depicted in Figure 27 on page 46 and Figure 28 on page 47. A detailed explanation of ^{t}DQSCK (DQS transition skew to CK) and ^{t}AC (data-out transition skew to CK) is shown in Figure 29 on page 48.

Data from any READ burst may be concatenated with data from a subsequent READ command to provide a continuous flow of data. The first data element from the new burst follows the last element of a completed burst. The new READ command should be issued *x* cycles after the first READ command, where *x* equals BL / 2 cycles. This is shown in Figure 19 on page 40.

Figure 16: READ Command

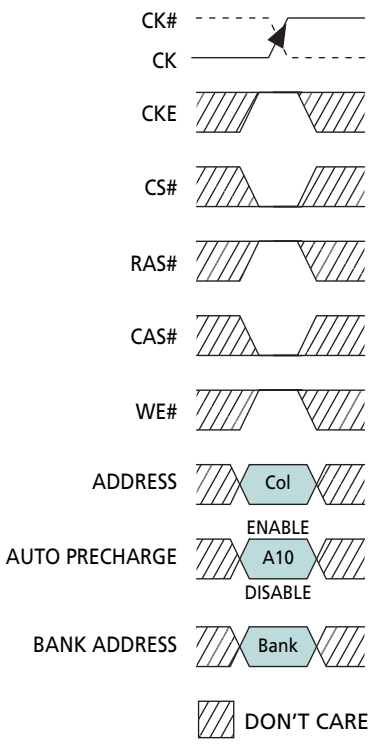


Figure 17: Example: Meeting ^{t}RRD (MIN) and ^{t}RCD (MIN)

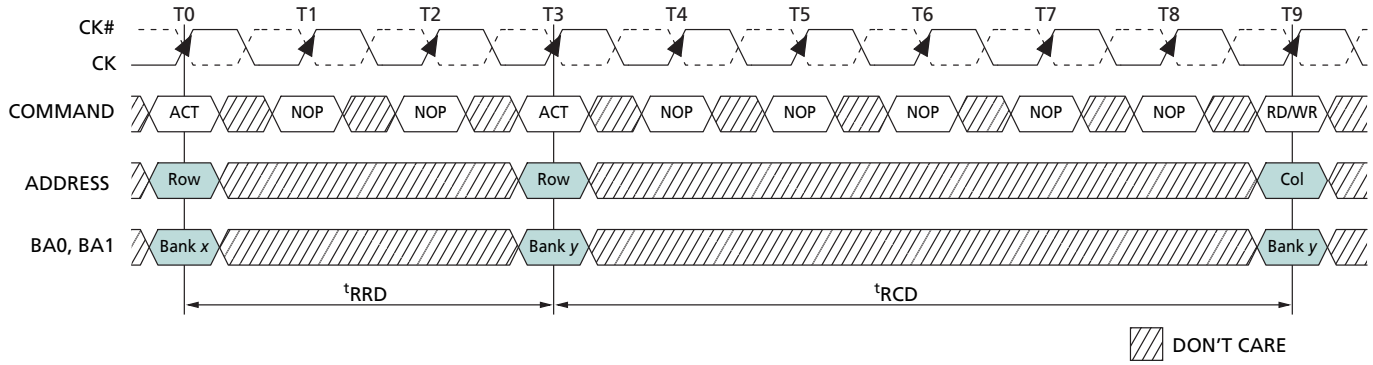
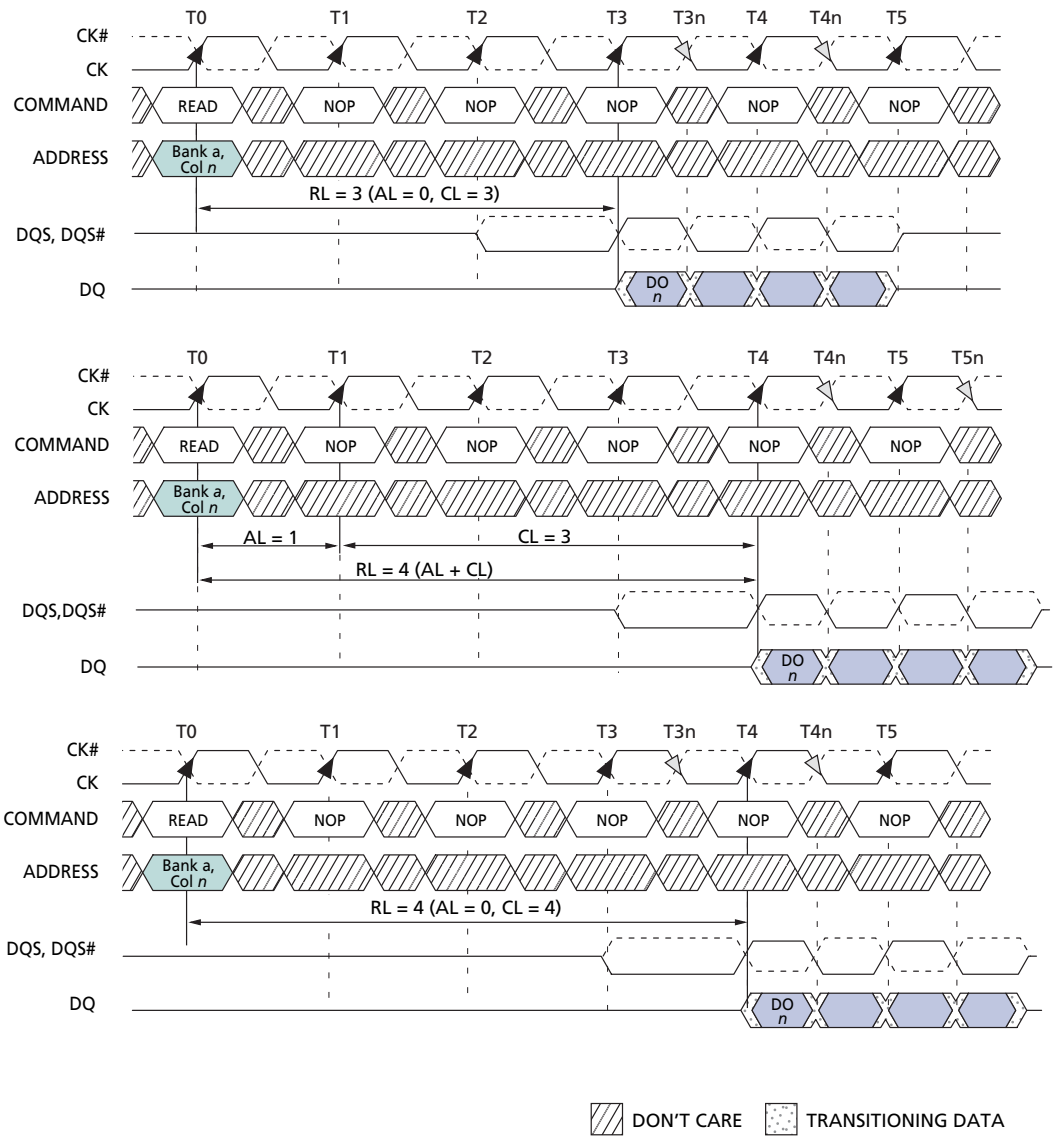
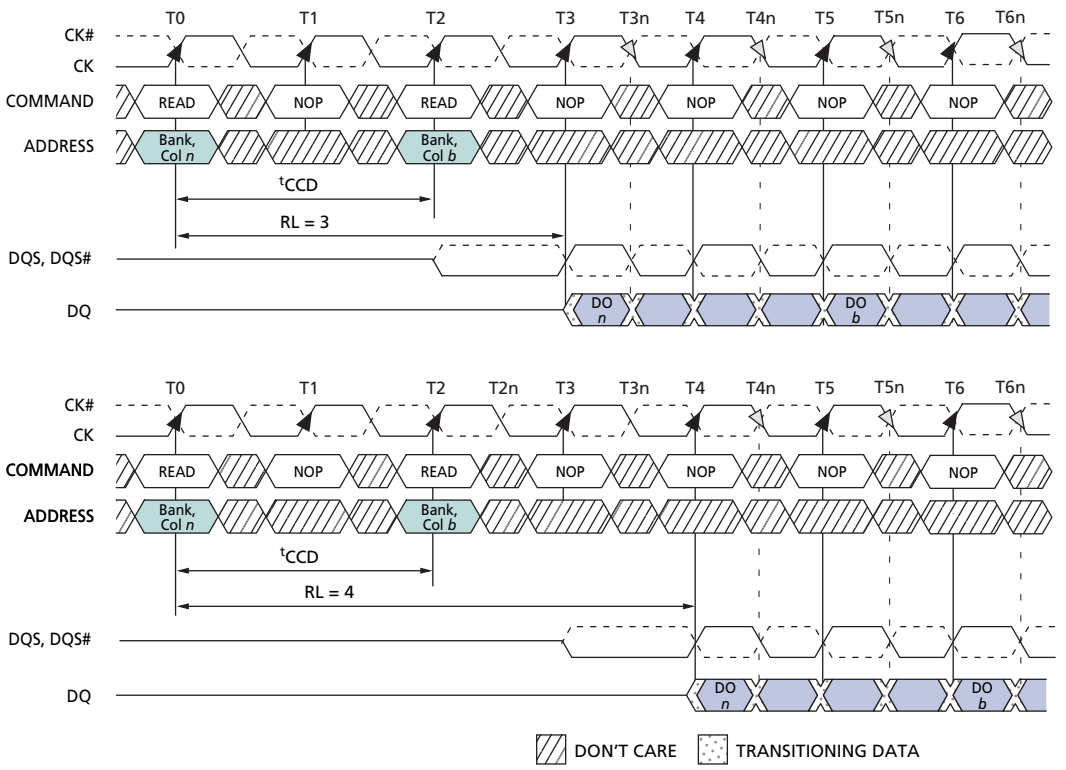


Figure 18: READ Latency



Notes: 1. DO *n* = data-out from column *n*.
2. BL = 4.
3. Three subsequent elements of data-out appear in the programmed order following DO *n*.
4. Shown with nominal ^{t}AC, ^{t}DQSCK, and ^{t}DQSQ.

Figure 19: Consecutive READ Bursts

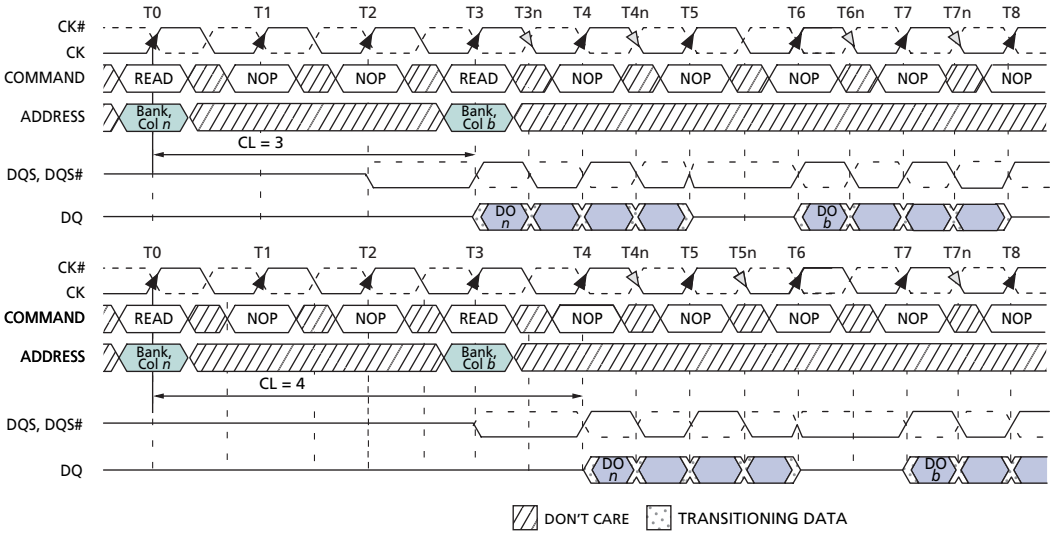


Notes: 1. DO *n* (or *b*) = data-out from column *n* (or column *b*).
2. BL = 4.
3. Three subsequent elements of data-out appear in the programmed order following DO *n*.
4. Three subsequent elements of data-out appear in the programmed order following DO *b*.
5. Shown with nominal ^{t}AC, ^{t}DQSCK, and ^{t}DQSQ.
6. Example applies only when READ commands are issued to same device.

Nonconsecutive read data is illustrated in Figure 20 on page 41. Full-speed random read accesses within a page (or pages) can be performed. DDR2 SDRAM supports the use of concurrent auto precharge timing, which is shown in Table 9 on page 42.

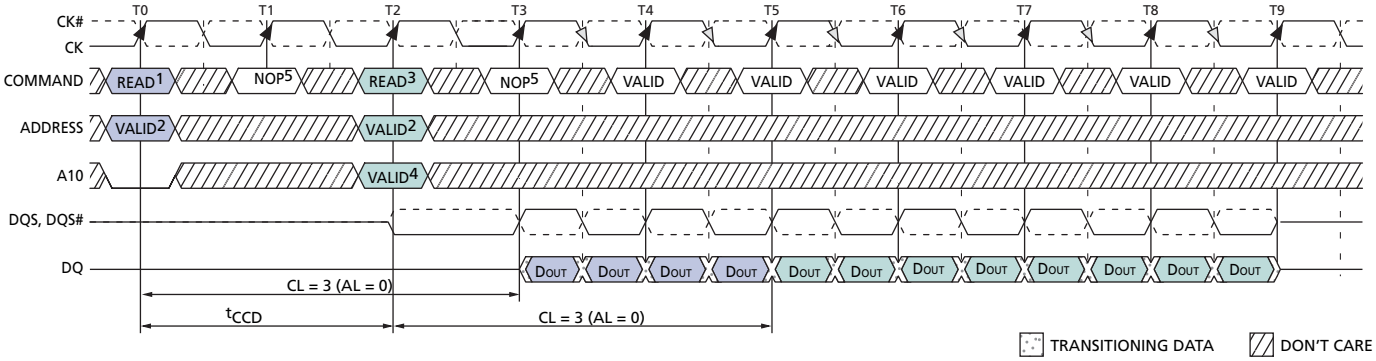
DDR2 SDRAM does not allow interrupting or truncating of any READ burst using BL = 4 operations. Once the BL = 4 READ command is registered, it must be allowed to complete the entire READ burst. However, a READ (with auto precharge disabled) using BL = 8 operation may be interrupted and truncated *only* by another READ burst as long as the interruption occurs on a 4-bit boundary due to the 4*n* prefetch architecture of DDR2 SDRAM. READ burst BL = 8 operations may not be interrupted or truncated with any command except another READ command, as shown in Figure 21 on page 41.

Figure 20: Nonconsecutive READ Bursts



Notes: 1. DO *n* (or *b*) = data-out from column *n* (or column *b*).
2. BL = 4.
3. Three subsequent elements of data-out appear in the programmed order following DO *n*.
4. Three subsequent elements of data-out appear in the programmed order following DO *b*.
5. Shown with nominal ^{t}AC, ^{t}DQSCK, and ^{t}DQSQ.
6. Example applies when READ commands are issued to different devices or nonconsecutive READs.

Figure 21: READ Interrupted by READ



Notes: 1. BL = 8 required; auto precharge must be disabled (A10 = LOW).
2. READ command can be issued to any valid bank and row address (READ command at T0 and T2 can be either same bank or different bank).
3. Interrupting READ command must be issued exactly 2 x ^{t}CK from previous READ.
4. Auto precharge can be either enabled (A10 = HIGH) or disabled (A10 = LOW) by the interrupting READ command.
5. NOP or COMMAND INHIBIT commands are valid. PRECHARGE command cannot be issued to banks used for READs at T0 and T2.
6. Example shown uses AL = 0; CL = 3, BL = 8, shown with nominal ^{t}AC, ^{t}DQSCK, and ^{t}DQSQ.

Table 9: READ Using Concurrent Auto Precharge

From Command (Bank *n*)	To Command (Bank *m*)	Minimum Delay (with Concurrent Auto Precharge)	Units
READ with auto precharge	READ or READ w/auto precharge	BL/2	^{t}CK
	WRITE or WRITE w/auto precharge	(BL/2) + 2	^{t}CK
	PRECHARGE or ACTIVE	1	^{t}CK

Data from any READ burst must be completed before a subsequent WRITE burst is allowed. An example of a READ burst followed by a WRITE burst is shown in Figure 24 on page 43. The ^{t}DQSS (MIN) case is shown; the ^{t}DQSS (MAX) case has a longer bus idle time. (^{t}DQSS [MIN] and ^{t}DQSS [MAX] are defined in Figure 31 on page 51.)

A READ burst may be followed by a PRECHARGE command to the same bank, provided that auto precharge was not activated. The minimum READ to PRECHARGE command spacing to the same bank is AL + BL/2 clocks and must also satisfy a minimum analog time from the rising clock edge that initiates the last 4-bit prefetch of a READ to PRECHARGE command. This read-to-precharge time is called ^{t}RTP. For BL = 4 this is the time from the actual READ (AL after the READ command) to PRECHARGE command. For BL = 8 this is the firm from AL + 2CK after the READ to PRECHARGE command. Following the PRECHARGE command, a subsequent command to the same bank cannot be issued until ^{t}RP is met. Not that part of the row precharge time is hidden during the access of the last data elements. Examples of READ to PRECHARGE are shown in Figure 22 on page 43 for BL = 4 and Figure 23 on page 43 for BL = 8. The delay from READ command to PRECHARGE command to the same bank is AL + BL/2 + MAX(^{t}RTP/^{t}CK or 2CK) - 2CK.

If A10 is HIGH when a READ command is issued, the READ with auto precharge function is engaged. The DDR2 SDRAM starts an auto precharge operation on the rising edge which is AL + (BL/2) cycles later than the READ with auto precharge command if ^{t}RAS (MIN) and ^{t}RTP are satisfied. If ^{t}RAS (MIN) is not satisfied at the edge, the start point of auto precharge operation will be delayed until ^{t}RAS (MIN) is satisfied. If ^{t}RTP (MIN) is not satisfied at the edge, the start point of the auto precharge operation will be delayed until ^{t}RTP (MIN) is satisfied. In case the internal precharge is pushed out by ^{t}RTP, ^{t}RP starts at the point where the internal precharge happens (not at the next rising clock edge after this event). For BL = 4 the minimum time from READ with auto precharge to the next activate command becomes AL + (^{t}RTP + ^{t}RP)*, shown in Figure 22 on page 43; for BL = 8 the time from READ with auto precharge to the next activate is AL + 2 clocks + (^{t}RTP + ^{t}RP)*, shown in Figure 23 on page 43). The * indicates each parameter term is divided by ^{t}CK and rounded up to the next integer. In any event, internal precharge does not start earlier than two clocks after the last 4-bit prefetch.

Figure 22: READ-To-PRECHARGE, BL = 4

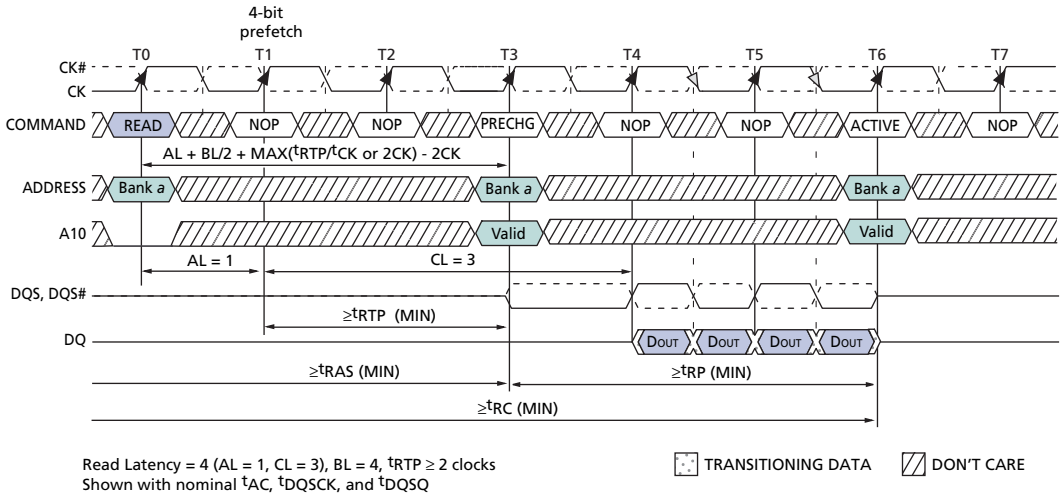


Figure 23: READ-To-PRECHARGE, BL = 8

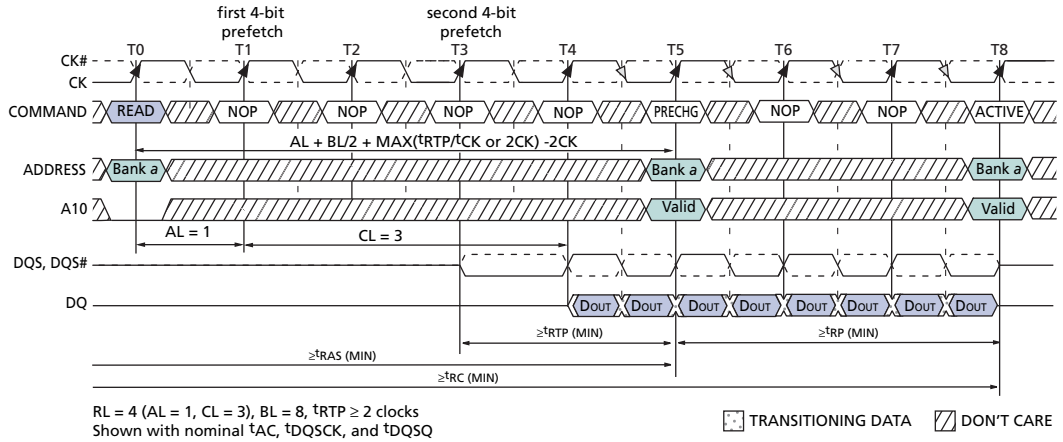


Figure 24: READ-To-WRITE

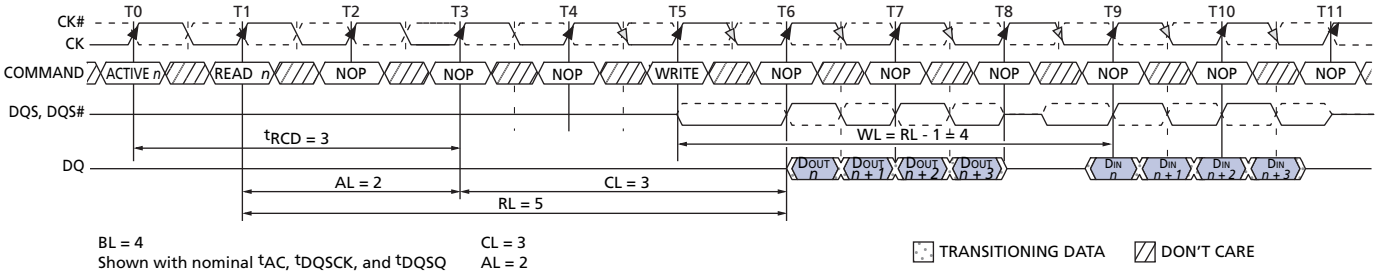
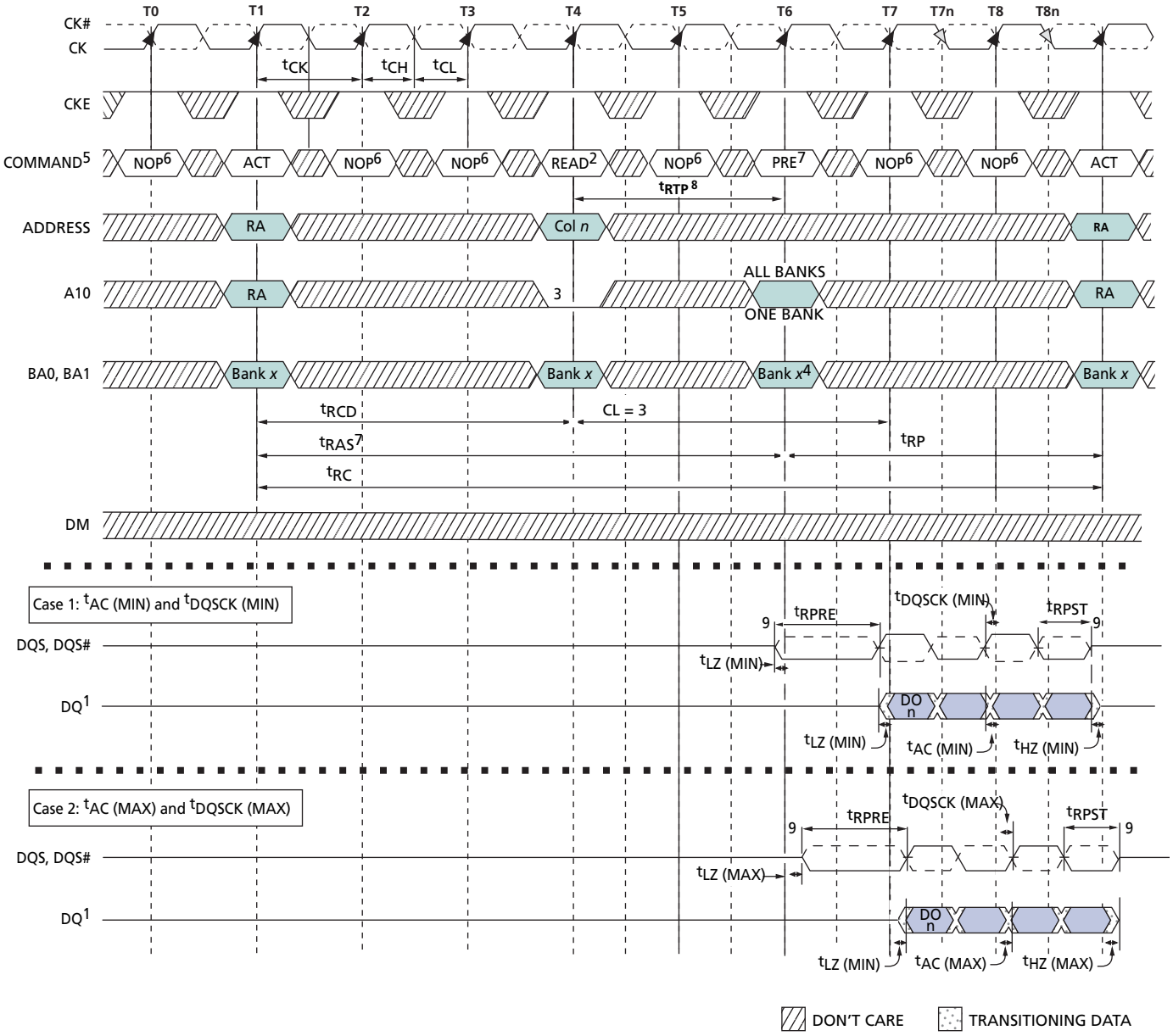
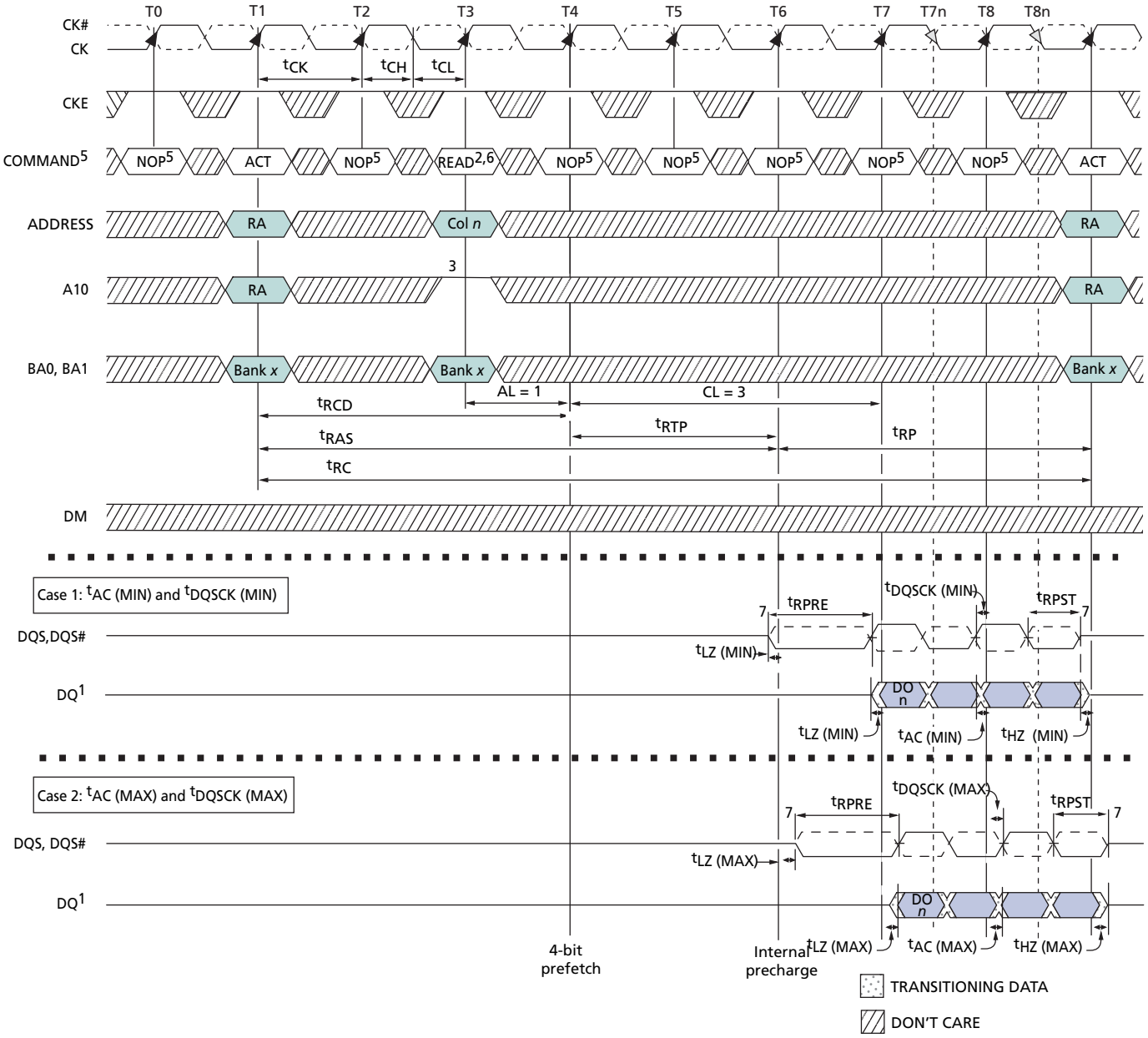


Figure 25: Bank Read – Without Auto Precharge



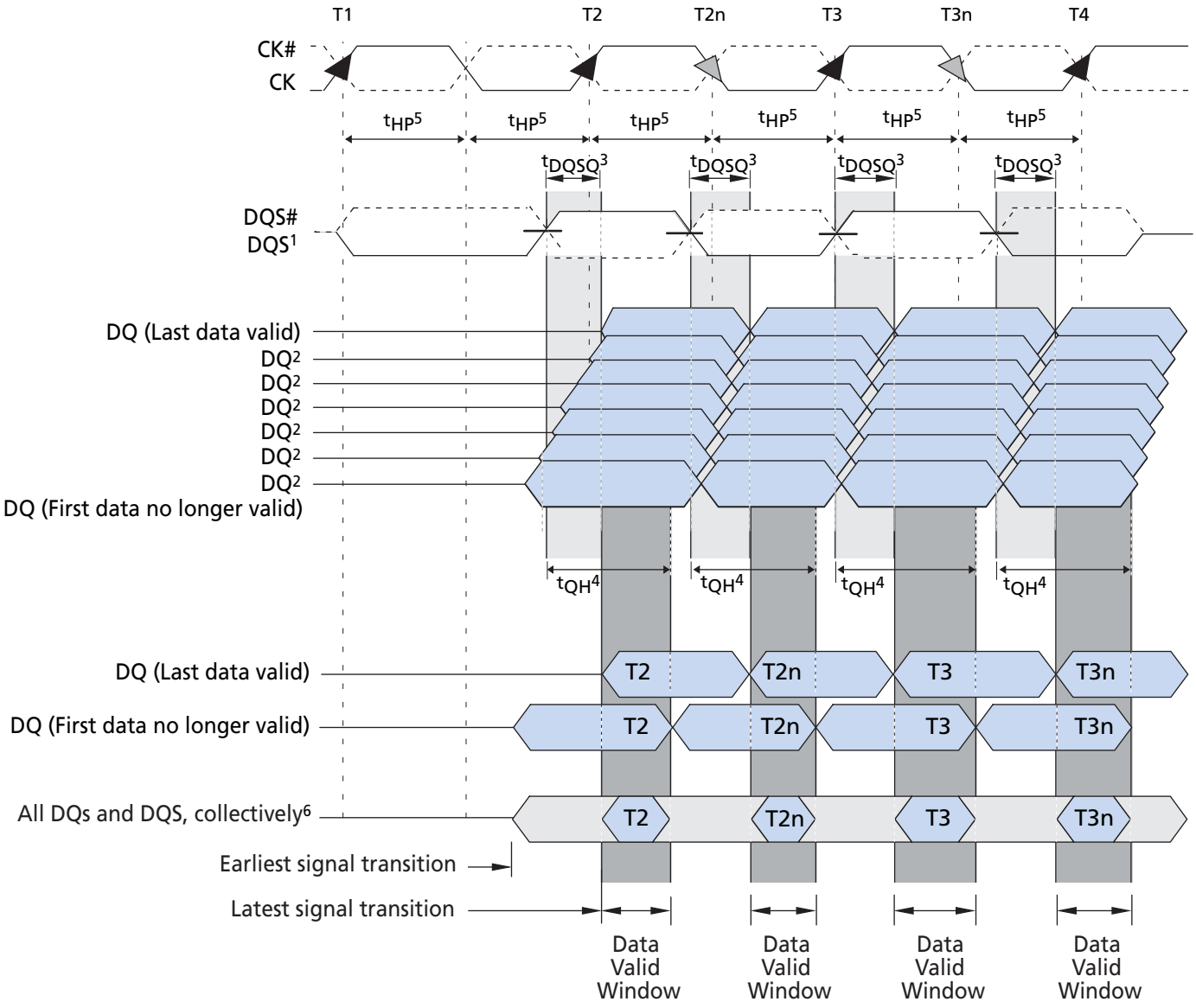
Notes:
1. DO *n* = data-out from column *n*; subsequent elements are applied in the programmed order.
2. BL = 4 and AL = 0 in the case shown.
3. Disable auto precharge.
4. "Don't Care" if A10 is HIGH at T5.
5. PRE = PRECHARGE, ACT = ACTIVE, RA = row address, BA = bank address.
6. NOP commands are shown for ease of illustration; other commands may be valid at these times.
7. The PRECHARGE command can only be applied at T6 if ^{t}RAS (MIN) is met.
8. READ-To-PRECHARGE = AL + BL/2 + (^{t}RTP - 2 clocks).
9. I/0 balls, when entering or exiting HIGH-Z are not referenced to a specific voltage level, but to when the device begins to drive or no longer drives, respectively.

Figure 26: Bank Read – With Auto Precharge



Notes:
1. DO *n* = data-out from column *n*; subsequent elements are applied in the programmed order.
2. BL = 4, RL = 4 (AL = 1, CL = 3) in the case shown.
3. Enable auto precharge.
4. ACT = ACTIVE, RA = row address, BA = bank address.
5. NOP commands are shown for ease of illustration; other commands may be valid at these times.
6. The DDR2 SDRAM internally delays auto precharge until both ^{t}RAS (MIN) and ^{t}RTP (MIN) have been satisfied.
7. I/0 balls, when entering or exiting HIGH-Z are not referenced to a specific voltage level, but to when the device begins to drive or no longer drives, respectively.

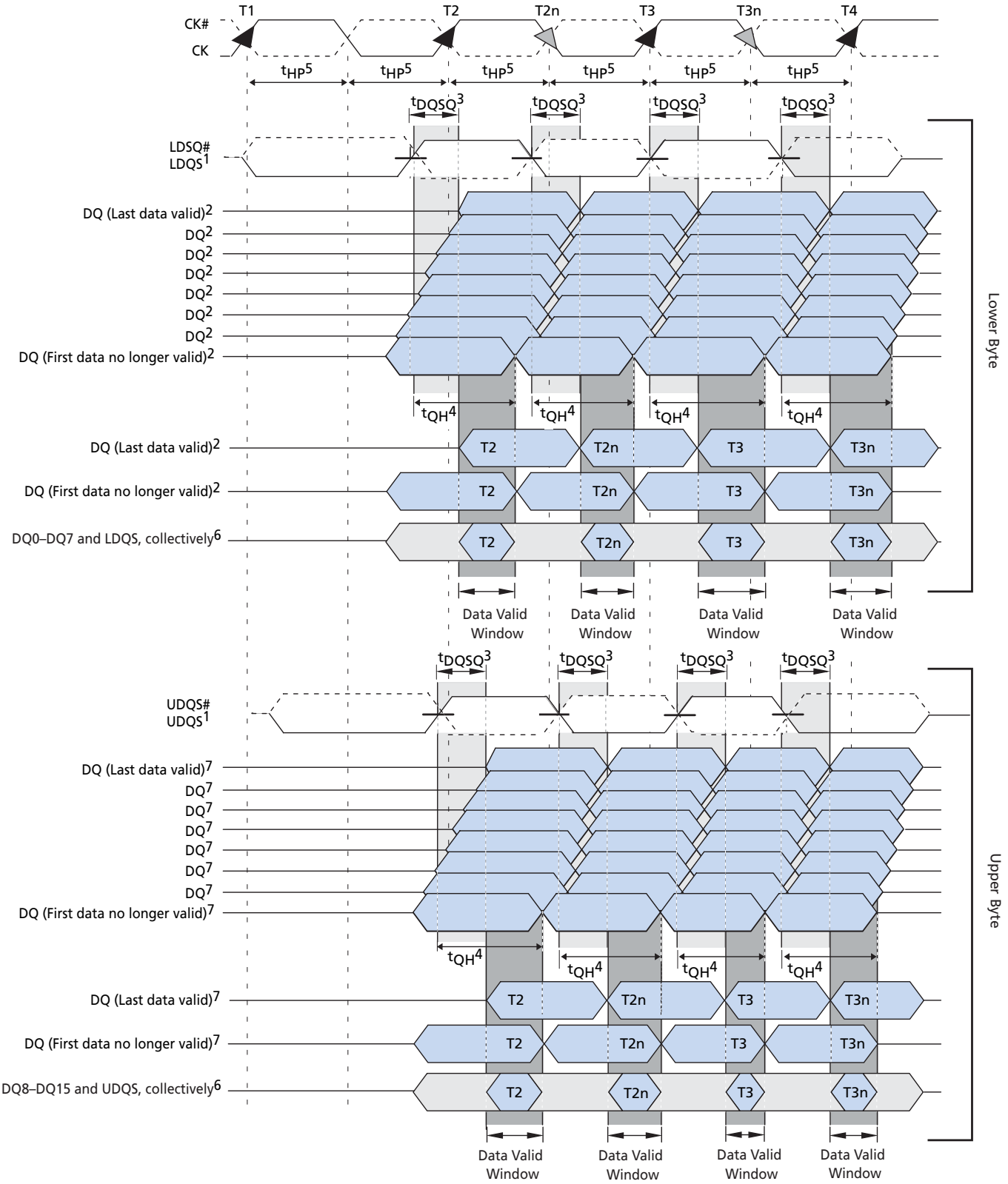
Figure 27: x4, x8 Data Output Timing – ^{t}DQSQ, ^{t}QH, and Data Valid Window



Notes:
1. DQ transitioning after DQS transition define ^{t}DQSQ window. DQS transitions at T2 and at T2n are "early DQS," at T3 are "nominal DQS," and at T3n are "late DQS."
2. For a x4, only two DQ apply.
3. ^{t}DQSQ is derived at each DQS clock edge, is not cumulative over time, begins with DQS transitions, and ends with the last valid transition of DQ.
4. ^{t}QH is derived from ^{t}HP: ^{t}QH = ^{t}HP - ^{t}QHS.
5. ^{t}HP is the lesser of ^{t}CL or ^{t}CH clock transitions collectively when a bank is active.
6. The data valid window is derived for each DQS transition and is defined as ^{t}QH - ^{t}DQSQ.

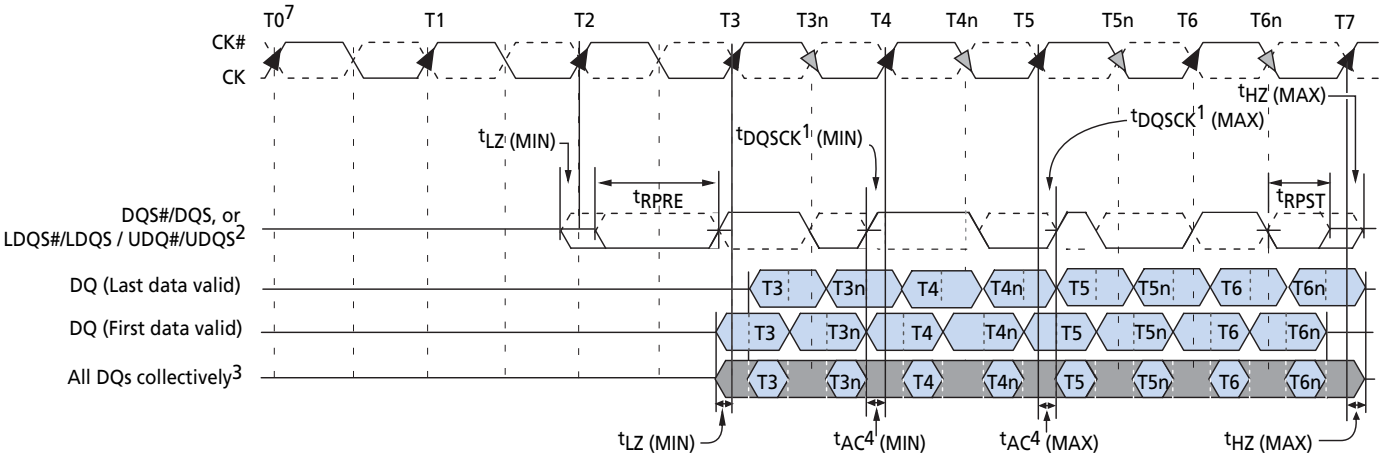
Figure 28: x16 Data Output Timing – ^{t}DQSQ, ^{t}QH, and Data Valid Window

Figure notes appear on page 48



Notes: 1. DQ transitioning after DQS transitions define the tDQSQ window. LDQS defines the lower byte, and UDQS defines the upper byte.
2. DQ0, DQ1, DQ2, DQ3, DQ4, DQ5, DQ6, or DQ7.
3. tDQSQ is derived at each DQS clock edge, is not cumulative over time, begins with DQS transitions, and ends with the last valid transition of DQ.
4. tQH is derived from tHP: tQH = tHP - tQHS.
5. tHP is the lesser of tCL or tCH clock transitions collectively when a bank is active.
6. The data valid window is derived for each DQS transition and is tQH - tDQSQ.
7. DQ8, DQ9, DQ10, D11, DQ12, DQ13, DQ14, or DQ15.

Figure 29: Data Output Timing – tAC and tDQSCK



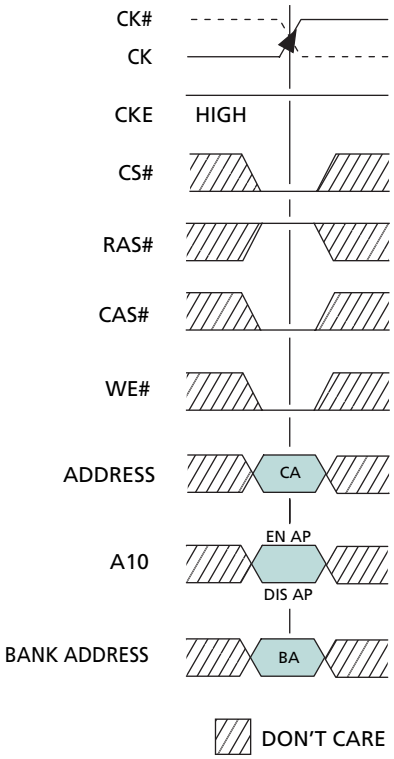
Notes: 1. tDQSCK is the DQS output window relative to CK and is the "long-term" component of DQS skew.
2. DQ transitioning after DQS transitions define tDQSQ window.
3. All DQ must transition by tDQSQ after DQS transitions, regardless of tAC.
4. tAC is the DQ output window relative to CK and is the "long term" component of DQ skew.
5. tLZ (MIN) and tAC (MIN) are the first valid signal transitions.
6. tHZ (MAX) and tAC (MAX) are the latest valid signal transitions.
7. READ command with CL = 3, AL = 0 issued at T0.
8. I/O balls, when entering or exiting HIGH-Z, are not referenced to a specific voltage level, but to when the device begins to drive or no longer drives, respectively.

WRITEs

WRITE Command

The WRITE command is used to initiate a burst write access to an active row. The value on the BA1–BA0 inputs selects the bank, and the address provided on inputs A0–*i* (where *i* = A9 for x8 and x16; or A9, A11 for x4) selects the starting column location. The value on input A10 determines whether or not auto precharge is used. If auto precharge is selected, the row being accessed will be precharged at the end of the WRITE burst; if auto precharge is not selected, the row will remain open for subsequent accesses.

Figure 30: WRITE Command



Note: CA = column address; BA = bank address; EN AP = enable auto precharge; and DIS AP = disable auto precharge.

Input data appearing on the DQ is written to the memory array subject to the DM input logic level appearing coincident with the data. If a given DM signal is registered LOW, the corresponding data will be written to memory; if the DM signal is registered HIGH, the corresponding data inputs will be ignored, and a WRITE will not be executed to that byte/column location (Figure 40 on page 58).

WRITE Operation

WRITE bursts are initiated with a WRITE command, as shown in Figure 30. DDR2 SDRAM uses WL equal to RL minus one clock cycle [WL = RL - 1CK = AL + (CL - 1CK)]. The starting column and bank addresses are provided with the WRITE command, and auto precharge is either enabled or disabled for that access. If auto precharge is enabled, the row being accessed is precharged at the completion of the burst. For the generic WRITE commands used in the following illustrations, auto precharge is disabled.

During WRITE bursts, the first valid data-in element will be registered on the first rising edge of DQS following the WRITE command, and subsequent data elements will be registered on successive edges of DQS. The LOW state on DQS between the WRITE command and the first rising edge is known as the write preamble; the LOW state on DQS following the last data-in element is known as the write postamble.

The time between the WRITE command and the first rising DQS edge is WL ±^{t}DQSS. Subsequent DQS positive rising edges are timed, relative to the associated clock edge, as ±^{t}DQSS. ^{t}DQSS is specified with a relatively wide range (25 percent of one clock cycle). All of the WRITE diagrams show the nominal case, and where the two extreme cases (^{t}DQSS [MIN] and ^{t}DQSS [MAX]) might not be intuitive, they have also been included. Figure 31 on page 51 shows the nominal case and the extremes of ^{t}DQSS for BL = 4. Upon completion of a burst, assuming no other commands have been initiated, the DQ will remain High-Z and any additional input data will be ignored.

Data for any WRITE burst may be concatenated with a subsequent WRITE command to provide continuous flow of input data. The first data element from the new burst is applied after the last element of a completed burst. The new WRITE command should be issued *x* cycles after the first WRITE command, where *x* equals BL/2.

Figure 32 on page 52 shows concatenated bursts of BL = 4. An example of nonconsecutive WRITEs is shown in Figure 33. Full-speed random write accesses within a page or pages can be performed as shown in Figure 34 on page 53. DDR2 SDRAM supports concurrent auto precharge options, as shown in Table 10.

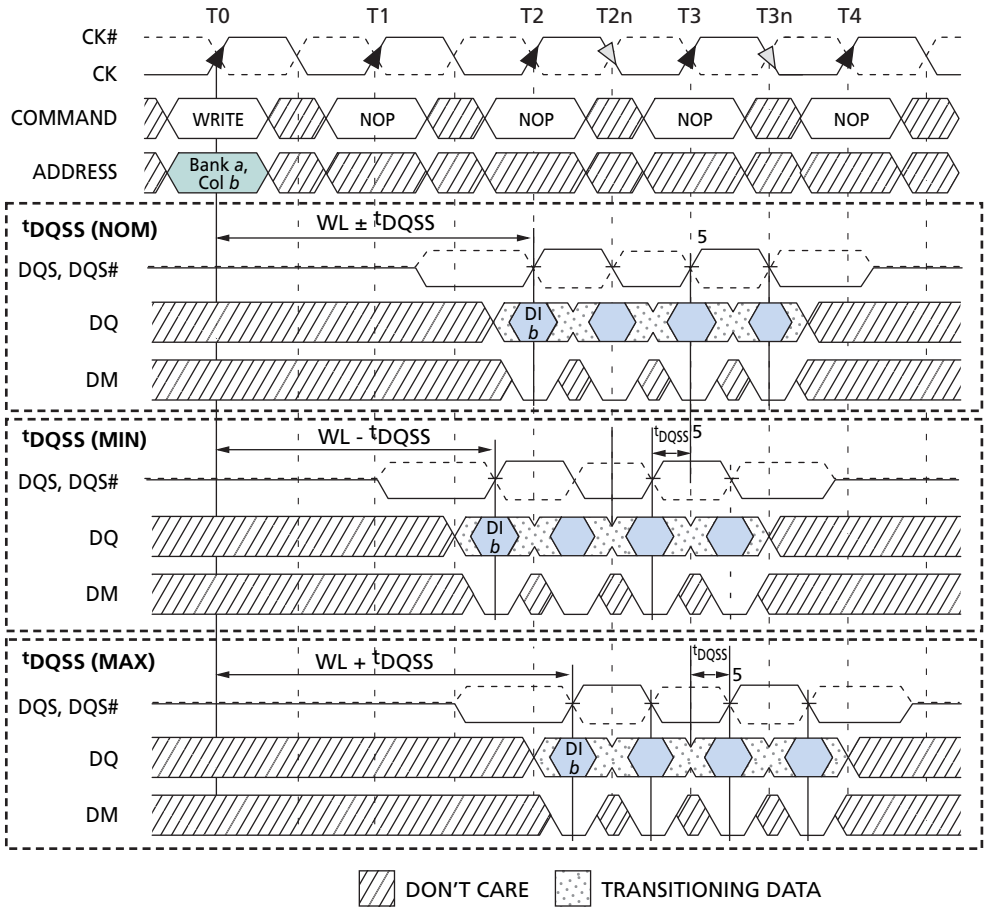
DDR2 SDRAM does not allow interrupting or truncating any WRITE burst using BL = 4 operation. Once the BL = 4 WRITE command is registered, it must be allowed to complete the entire WRITE burst cycle. However, a WRITE (with auto precharge disabled) using BL = 8 operation might be interrupted and truncated ONLY by another WRITE burst as long as the interruption occurs on a 4-bit boundary, due to the 4*n* prefetch architecture of DDR2 SDRAM. WRITE burst BL = 8 operations may *not* be interrupted or truncated with any command except another WRITE command, as shown in Figure 35.

Data for any WRITE burst may be followed by a subsequent READ command. To follow a WRITE, ^{t}WTR should be met as shown in Figure 36 on page 54. The number of clock cycles required to meet tWTR is either 2 or ^{t}WTR/^{t}CK, whichever is greater. Data for any WRITE burst may be followed by a subsequent PRECHARGE command. ^{t}WR must be met, as shown in Figure 30 on page 49. ^{t}WR starts at the end of the data burst, regardless of the data mask condition.

Table 10: WRITE Using Concurrent Auto Precharge

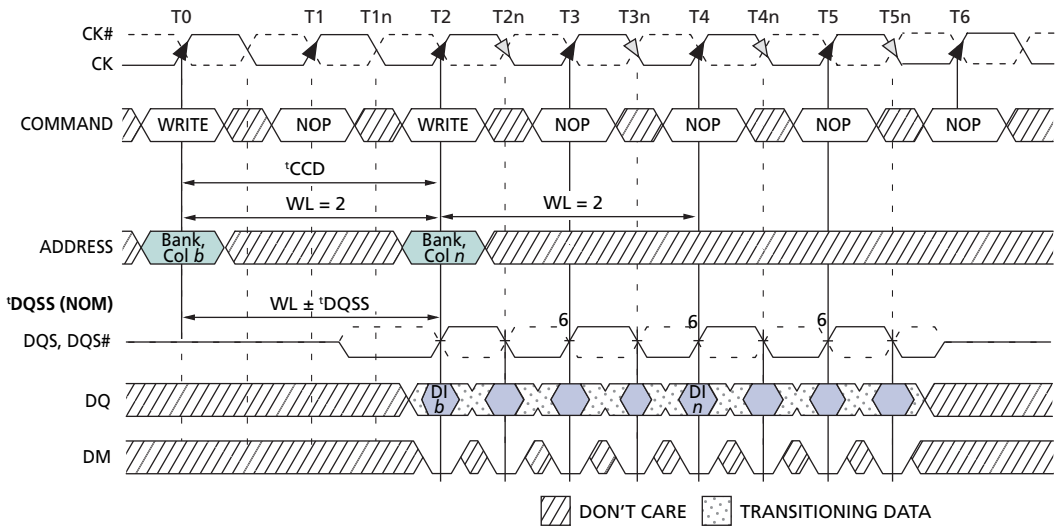
From Command (Bank *n*)	To Command (Bank *m*)	Minimum Delay (With Concurrent Auto Precharge)	Units
WRITE with Auto Precharge	READ or READ w/AP	(CL-1) + (BL/2) + ^{t}WTR	^{t}CK
	WRITE or WRITE w/AP	(BL/2)	^{t}CK
	PRECHARGE or ACTIVE	1	^{t}CK

Figure 31: WRITE Burst



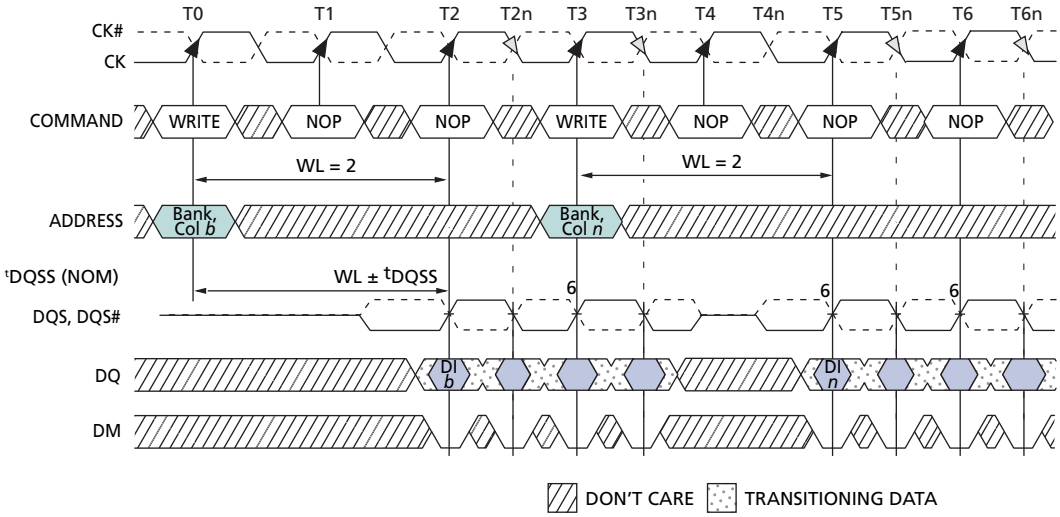
Notes:
1. DI *b* = data-in for column *b*.
2. Three subsequent elements of data-in are applied in the programmed order following DI *b*.
3. Shown with BL = 4, AL = 0, CL = 3; thus, WL = 2.
4. A10 is LOW with the WRITE command (auto precharge is disabled).
5. Subsequent rising DQS signals must align to the clock within ^{t}DQSS.

Figure 32: Consecutive WRITE to WRITE



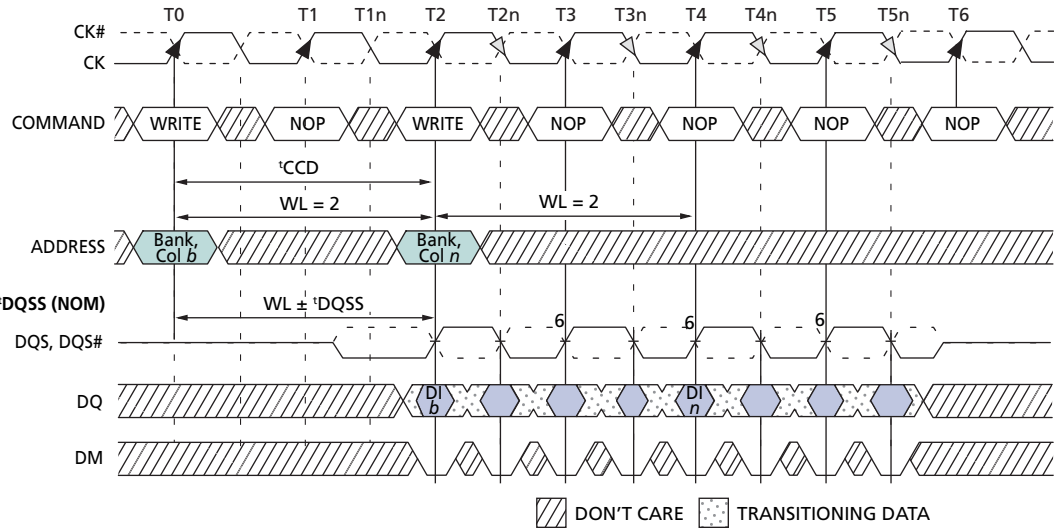
Notes: 1. DI *b*, etc. = data-in for column *b*, etc.
2. Three subsequent elements of data-in are applied in the programmed order following DI *b*.
3. Three subsequent elements of data-in are applied in the programmed order following DI *n*.
4. Shown with BL = 4, AL = 0, CL = 3; thus, WL = 2.
5. Each WRITE command may be to any bank.
6. Subsequent rising DQS signals must align to the clock within ^{t}DQSS.

Figure 33: Nonconsecutive WRITE to WRITE



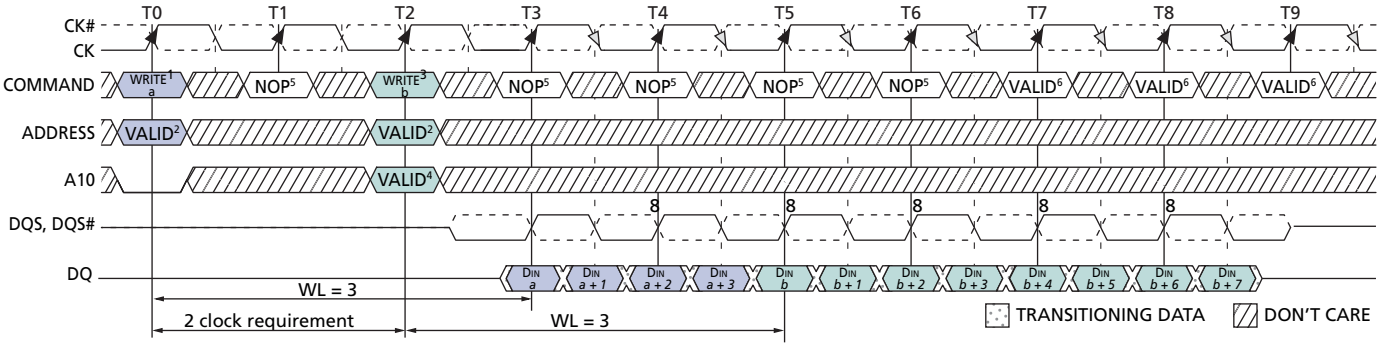
Notes: 1. DI *b*, etc. = data-in for column *b*, etc.
2. Three subsequent elements of data-in are applied in the programmed order following DI *b*.
3. Three subsequent elements of data-in are applied in the programmed order following DI *n*.
4. Shown with BL = 4, AL = 0, CL = 3; thus, WL = 2.
5. Each WRITE command may be to any bank.
6. Subsequent rising DQS signals must align to the clock within ^{t}DQSS.

Figure 34: Random WRITE Cycles



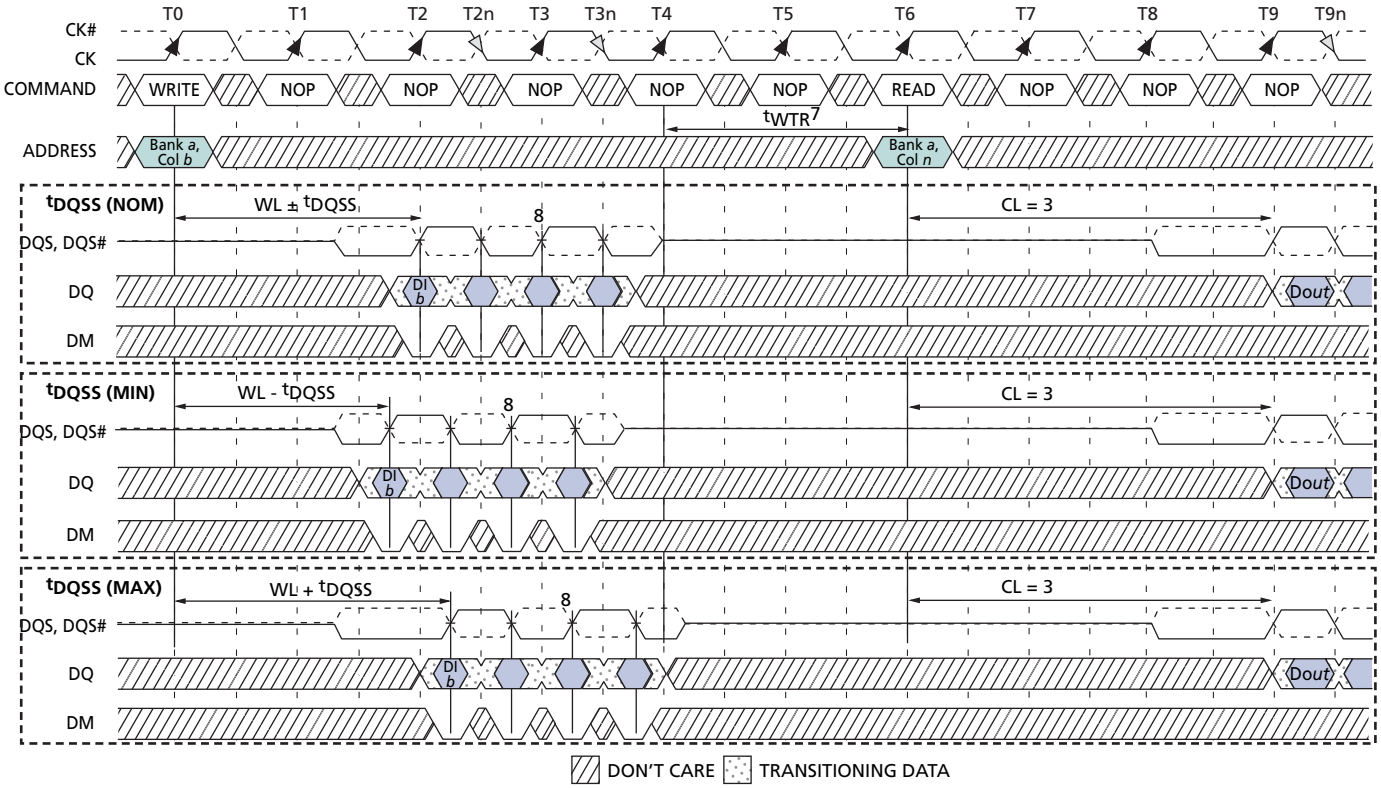
Notes:
1. DI *b*, etc. = data-in for column *b*, etc.
2. Three subsequent elements of data-in are applied in the programmed order following DI *b*.
3. Three subsequent elements of data-in are applied in the programmed order following DI *n*.
4. Shown with BL = 4, AL = 0, CL = 3; thus, WL = 2.
5. Each WRITE command may be to any bank.
6. Subsequent rising DQS signals must align to the clock within ^{t}DQSS.

Figure 35: WRITE Interrupted by WRITE



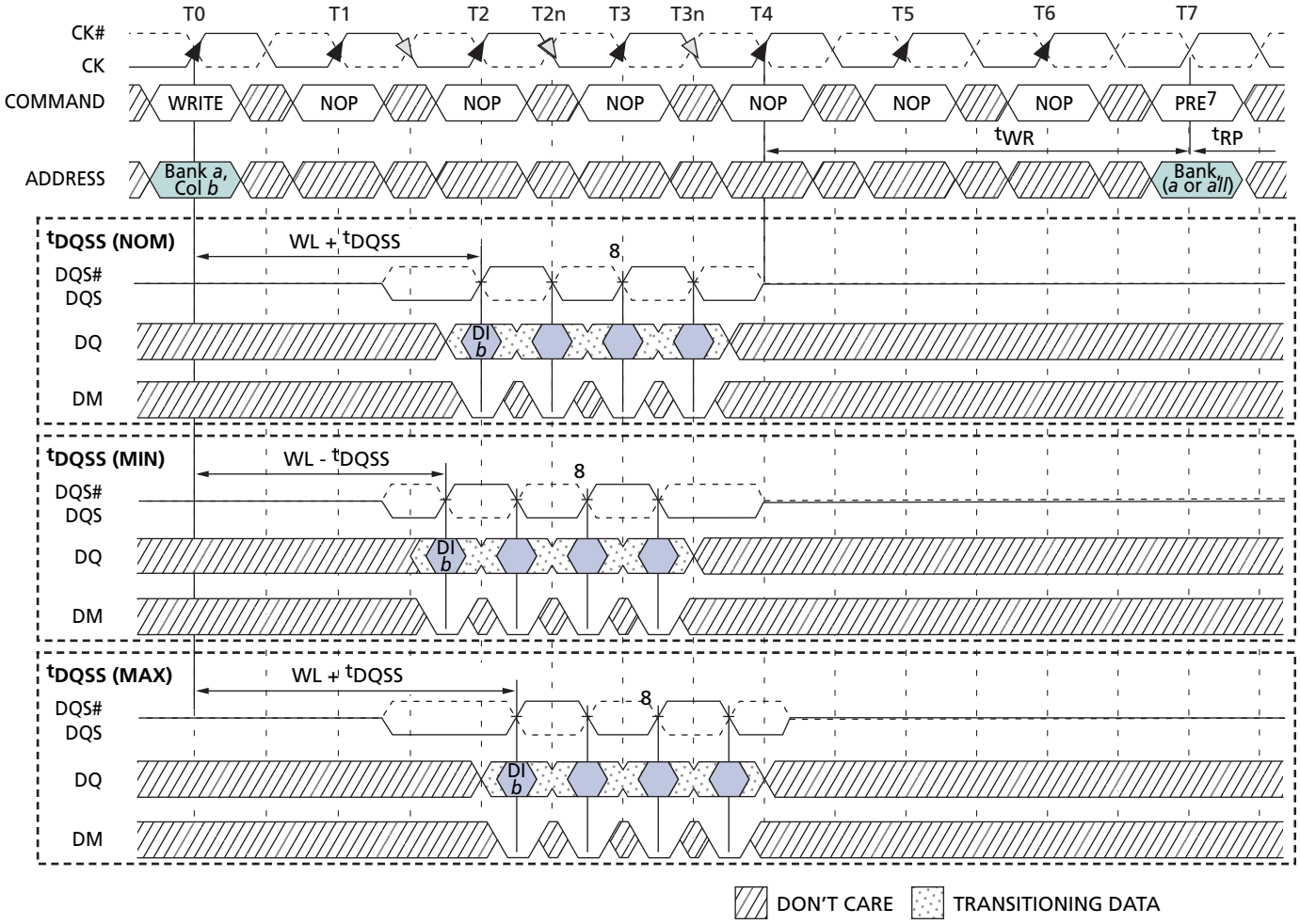
Notes:
1. BL = 8 required and auto precharge must be disabled (A10 = LOW).
2. WRITE command can be issued to any valid bank and row address (WRITE command at T0 and T2 can be either same bank or different bank).
3. Interrupting WRITE command must be issued exactly 2 x ^{t}CK from previous WRITE.
4. Auto precharge can be either enabled (A10 = HIGH) or disabled (A10 = LOW) by the interrupting WRITE command.
5. NOP or COMMAND INHIBIT commands are valid. PRECHARGE command cannot be issued to banks used for WRITEs at T0 and T2.
6. Earliest WRITE-to-PRECHARGE timing for WRITE at T0 is WL + BL/2 + ^{t}WR where ^{t}WR starts with T7 and not T5 (since BL = 8 from MR and not the truncated length).
7. Example shown uses AL = 0; CL = 4, BL = 8.
8. Subsequent rising DQS signals must align to the clock within ^{t}DQSS.

Figure 36: WRITE-To-READ



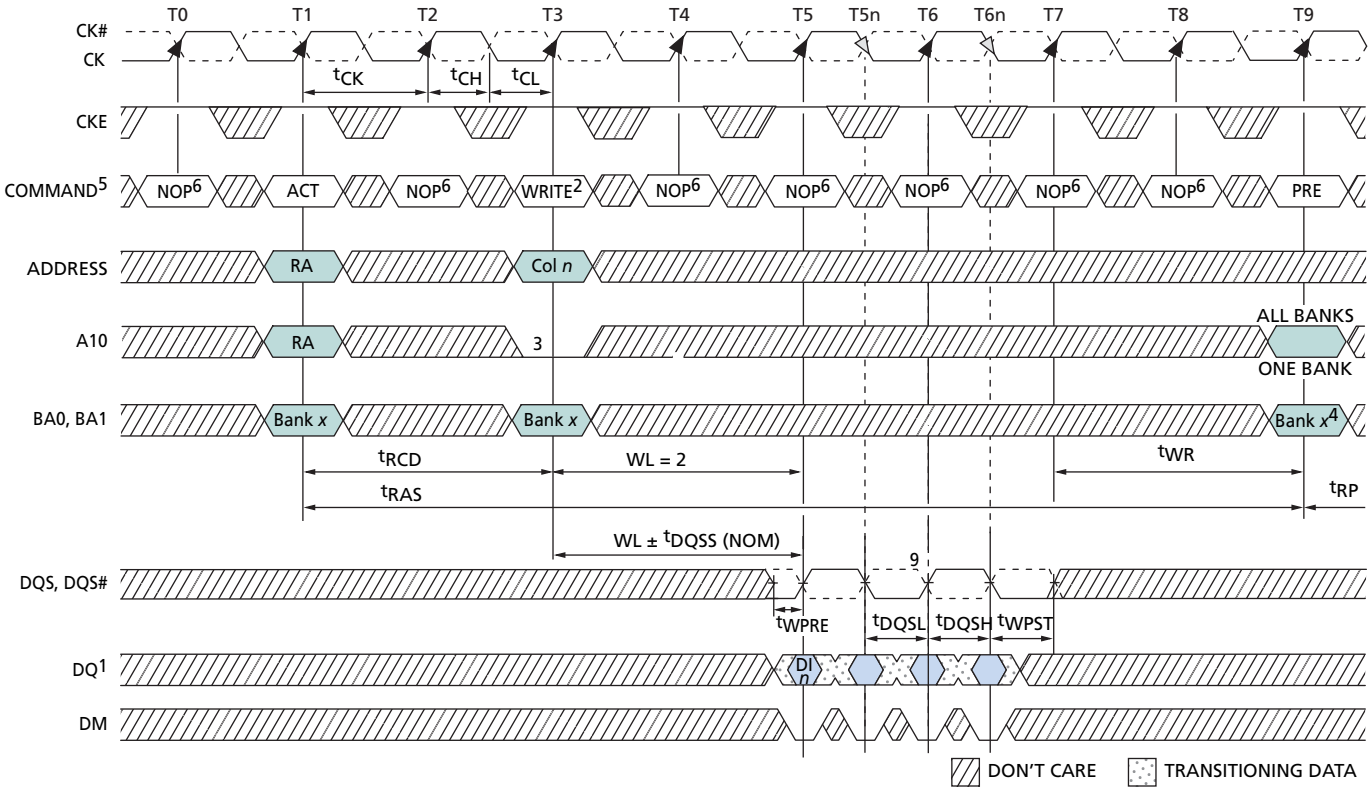
Notes:
1. DI *b* = data-in for column *b*; DOUT n = data out from column n.
2. BL = 4, AL = 0, CL = 3; thus, WL = 2.
3. One subsequent element of data-in is applied in the programmed order following DI *b*.
4. ^{t}WTR is referenced from the first positive CK edge after the last data-in pair.
5. A10 is LOW with the WRITE command (auto precharge is disabled).
6. The number of clock cycles required to meet ^{t}WTR is either 2 or ^{t}WTR/^{t}CK, whichever is greater.
7. ^{t}WTR is required for any READ following a WRITE to the same device, but it is not required between module ranks.
8. Subsequent rising DQS signals must align to the clock within ^{t}DQSS.

Figure 37: WRITE-To-PRECHARGE



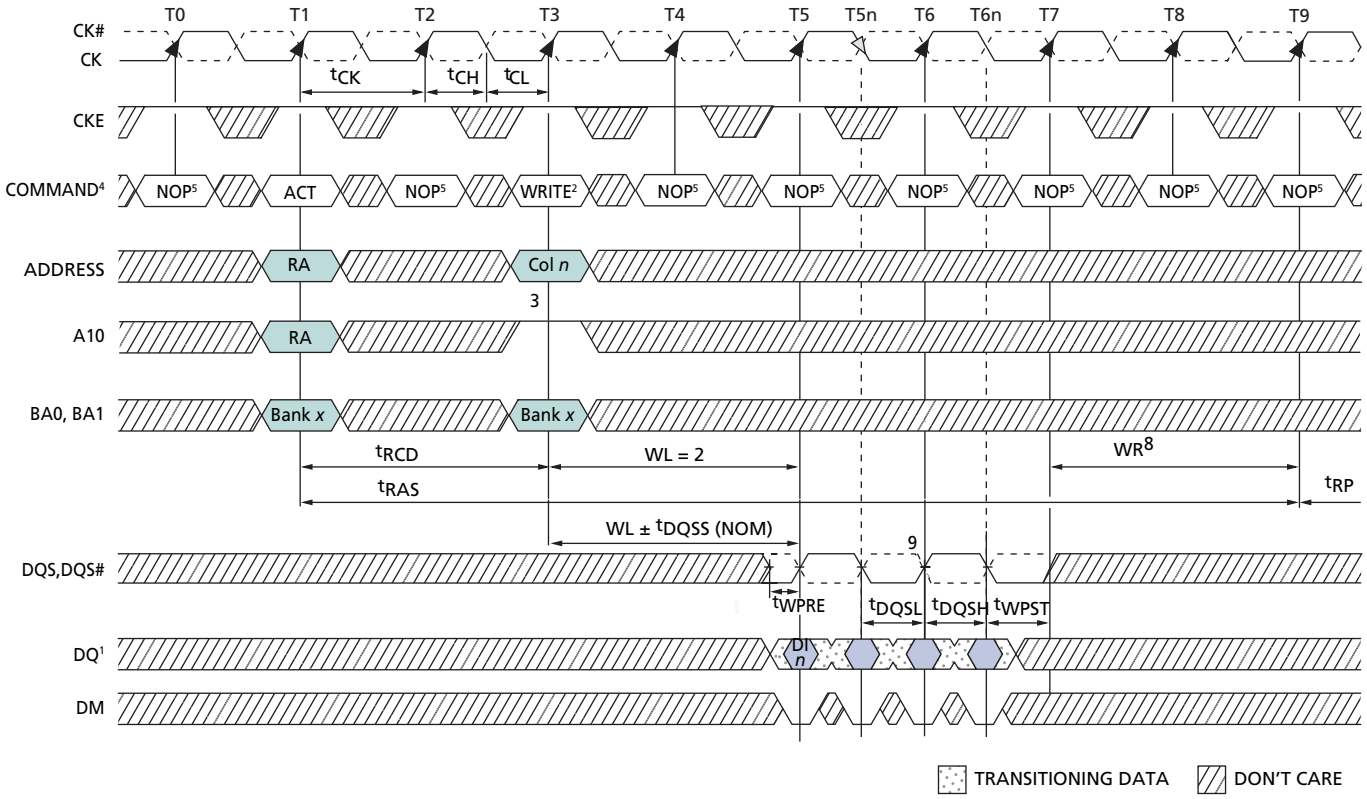
Notes:
1. DI *b* = data-in for column *b*.
2. Three subsequent elements of data-in are applied in the programmed order following DI *b*.
3. BL = 4, CL = 3, AL = 0; thus, WL = 2.
4. ^{t}WR is referenced from the first positive CK edge after the last data-in pair.
5. The PRECHARGE and WRITE commands are to the same bank. However, the PRECHARGE and WRITE commands may be to different banks, in which case ^{t}WR is not required and the PRECHARGE command could be applied earlier.
6. A10 is LOW with the WRITE command (auto precharge is disabled).
7. PRE = PRECHARGE command.
8. Subsequent rising DQS signals must align to the clock within ^{t}DQSS.

Figure 38: Bank Write – Without Auto Precharge



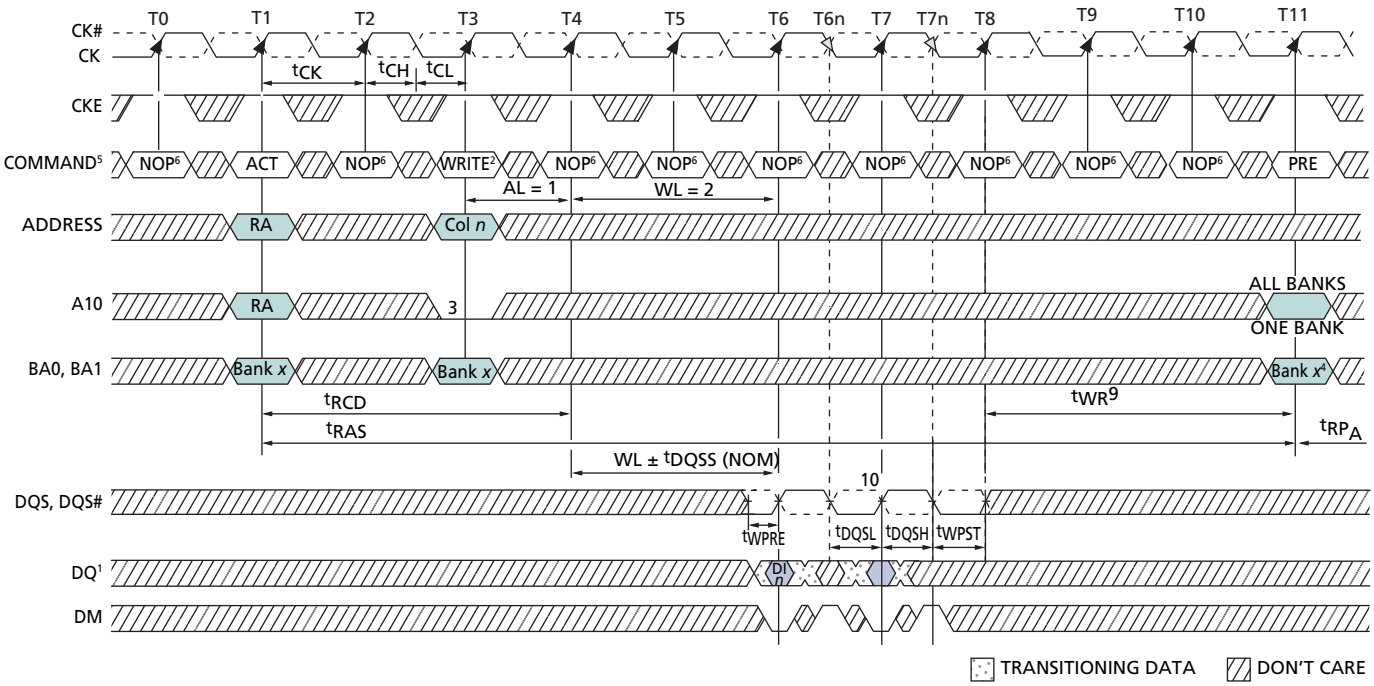
Notes:
1. DI *n* = data-in from column *n*; subsequent elements are applied in the programmed order.
2. BL = 4, AL = 0, and WL = 2 in the case shown.
3. Disable auto precharge.
4. "Don't Care" if A10 is HIGH at T9.
5. PRE = PRECHARGE, ACT = ACTIVE, RA = row address, BA = bank address.
6. NOP commands are shown for ease of illustration; other commands may be valid at these times.
7. ^{t}DSH is applicable during ^{t}DQSS (MIN) and is referenced from CK T5 or T6.
8. ^{t}DSS is applicable during ^{t}DQSS (MAX) and is referenced from CK T6 or T7.
9. Subsequent rising DQS signals must align to the clock within ^{t}DQSS.

Figure 39: Bank Write – With Auto Precharge



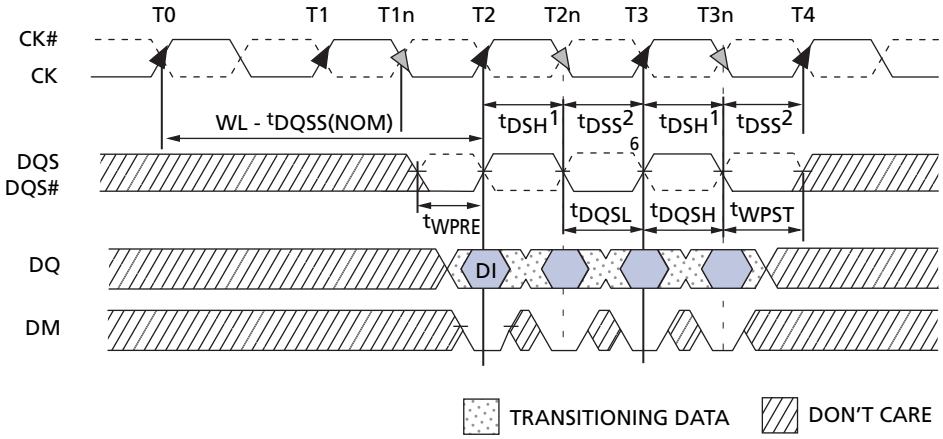
Notes:
1. DI *n* = data-in from column *n*; subsequent elements are applied in the programmed order.
2. BL = 4, AL = 0, and WL = 2 shown.
3. Enable auto precharge.
4. ACT = ACTIVE, RA = row address, BA = bank address.
5. NOP commands are shown for ease of illustration; other commands may be valid at these times.
6. ^{t}DSH is applicable during ^{t}DQSS (MIN) and is referenced from CK T5 or T6.
7. ^{t}DSS is applicable during ^{t}DQSS (MAX) and is referenced from CK T6 or T7.
8. WR is programmed via MR[11, 10, 9] and is calculated by dividing ^{t}WR (in ns) by ^{t}CK and rounding up to the next integer value.
9. Subsequent rising DQS signals must align to the clock within ^{t}DQSS.

Figure 40: WRITE – DM Operation



Notes:
1. DI *n* = data-in from column *n*; subsequent elements are applied in the programmed order.
2. Burst length = 4, AL = 1, and WL = 2 in the case shown.
3. Disable auto precharge.
4. "Don't Care" if A10 is HIGH at T11.
5. PRE = PRECHARGE, ACT = ACTIVE, RA = row address, BA = bank address.
6. NOP commands are shown for ease of illustration; other commands may be valid at these times.
7. ^{t}DSH is applicable during ^{t}DQSS (MIN) and is referenced from CK T6 or T7.
8. ^{t}DSS is applicable during ^{t}DQSS (MAX) and is referenced from CK T7 or T8.
9. ^{t}WR starts at the end of the data burst regardless of the data mask condition.
10. Subsequent rising DQS signals must align to the clock within ^{t}DQSS.

Figure 41: Data Input Timing



Notes:
1. ^{t}DSH (MIN) generally occurs during ^{t}DQSS (MIN).
2. ^{t}DSS (MIN) generally occurs during ^{t}DQSS (MAX).
3. WRITE command issued at T0.
4. For x16, LDQS controls the lower byte and UDQS controls the upper byte.
5. WRITE command with WL = 2 (CL = 3, AL = 0) issued at T0.
6. Subsequent rising DQS signals must align to the clock within ^{t}DQSS.

Precharge

PRECHARGE Command

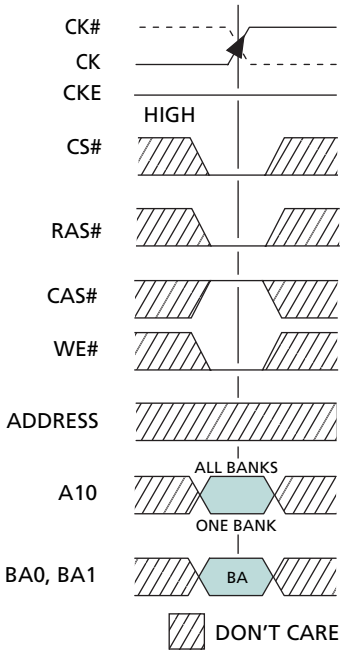
The PRECHARGE command, illustrated in Figure 42 on page 60, is used to deactivate the open row in a particular bank or the open row in all banks. The bank(s) will be available for a subsequent row activation a specified time (^{t}RP) after the PRECHARGE command is issued, except in the case of concurrent auto precharge, where a READ or WRITE command to a different bank is allowed as long as it does not interrupt the data transfer in the current bank and does not violate any other timing parameters. Once a bank has been precharged, it is in the idle state and must be activated prior to any READ or WRITE commands being issued to that bank. A PRECHARGE command is allowed if there is no open row in that bank (idle state) or if the previously open row is already in the process of precharging. However, the precharge period will be determined by the last PRECHARGE command issued to the bank.

PRECHARGE Operation

Input A10 determines whether one or all banks are to be precharged, and in the case where only one bank is to be precharged, inputs BA1–BA0 select the bank. Otherwise BA1–BA0 are treated as "Don't Care."

When all banks are to be precharged, inputs BA1–BA0 are treated as "Don't Care." Once a bank has been precharged, it is in the idle state and must be activated prior to any READ or WRITE commands being issued to that bank. ^{t}RPA timing applies when the PRECHARGE (ALL) command is issued, regardless of the number of banks already open or closed. If a single-bank PRECHARGE command is issued, ^{t}RP timing applies.

Figure 42: PRECHARGE Command



Note: BA = bank address (if A10 is LOW; otherwise "Don't Care").

Self Refresh

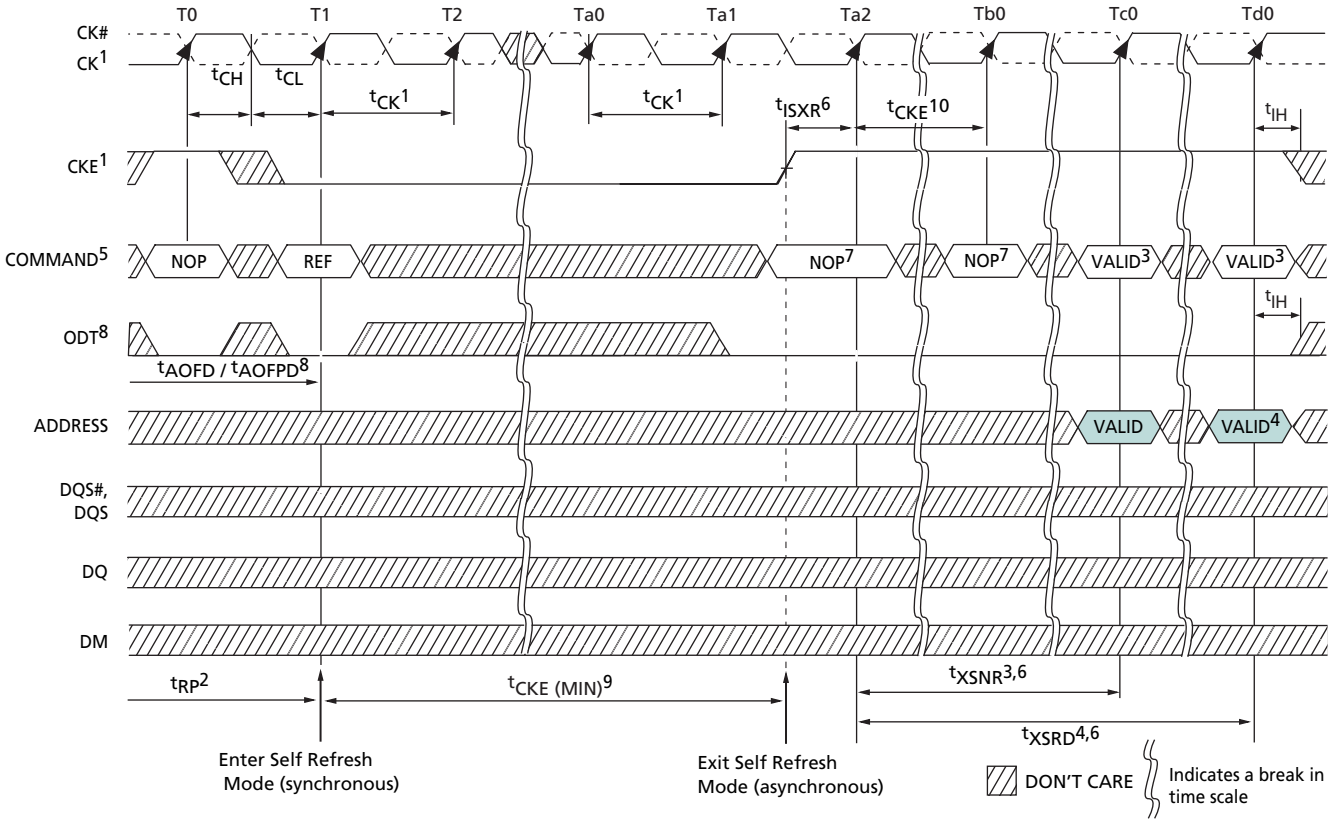
SELF REFRESH Command

The SELF REFRESH command can be used to retain data in the DDR2 SDRAM, even if the rest of the system is powered down. When in the self refresh mode, the DDR2 SDRAM retains data without external clocking. All power supply inputs (including V_{REF}) must be maintained at valid levels upon entry/exit *and* during SELF REFRESH operation.

The SELF REFRESH command is initiated like a REFRESH command except CKE is LOW. The DLL is automatically disabled upon entering self refresh and is automatically enabled upon exiting self refresh (200 clock cycles must then occur before a READ command can be issued). The differential clock should remain stable and meet ^{t}CKE specifications at least 1 x ^{t}CK after entering self refresh mode. All command and address input signals except CKE are "Don't Care" during self refresh.

The procedure for exiting self refresh requires a sequence of commands. First, the differential clock must be stable and meet ^{t}CK specifications at least 1 x ^{t}CK prior to CKE going back HIGH. Once CKE is HIGH (^{t}CKE [MIN] has been satisfied with four clock registrations), the DDR2 SDRAM must have NOP or DESELECT commands issued for ^{t}XSNR because time is required for the completion of any internal refresh in progress. A simple algorithm for meeting both refresh and DLL requirements is to apply NOP or DESELECT commands for 200 clock cycles before applying any other command.

Figure 43: Self Refresh



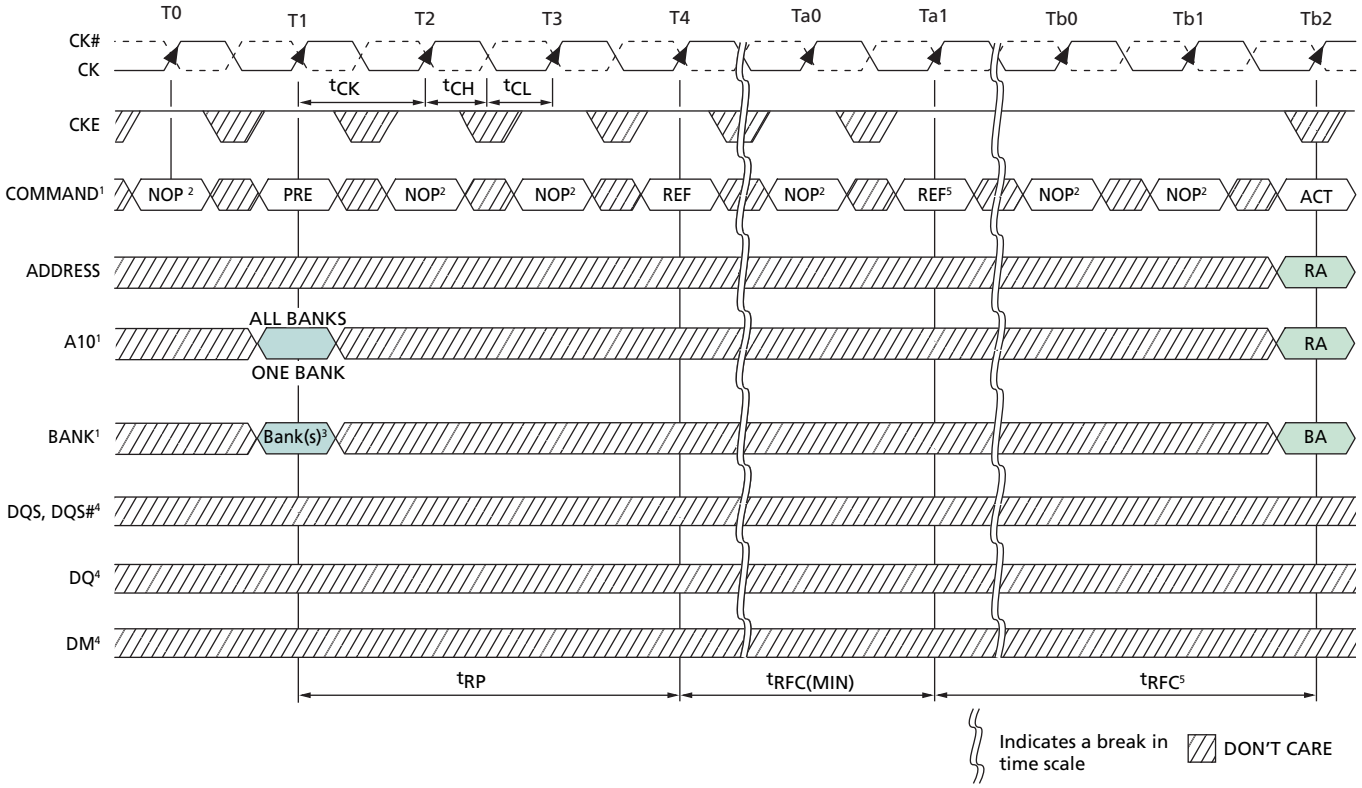
Notes:
1. Clock must be stable and meeting tCK specifications at least 1 x tCK after entering self refresh and at least 1 x tCK prior to exiting self refresh mode.
2. Device must be in the all banks idle state prior to entering self refresh mode.
3. tXSNR is required before any non-READ command can be applied.
4. tXSRD (200 cycles of CK) is required before a READ command can be applied at state Td0.
5. REF = REFRESH command.
6. Self refresh exit is asynchronous; however, tXSNR and tXSRD timing starts at the first rising clock edge where CKE HIGH satisfies tISXR.
7. NOP or DESELECT commands are required prior to exiting self refresh until state Tc0, which allows any non-READ command.
8. ODT must be disabled and RTT off (tAOFD and tAOFPD have been satisfied) prior to entering SELF REFRESH at state T1.
9. Once SELF REFRESH has been entered, tCKE (MIN) must be satisfied prior to exiting self refresh.
10. CKE must stay HIGH until tXSRD is met; however, if self refresh is being re-entered, CKE may go back low after tXSNR is satisfied.
11. Once exiting SELF REFRESH, ODT must remain low until tXSRD is satisfied.

REFRESH

REFRESH Command

REFRESH is used during normal operation of the DDR2 SDRAM and is analogous to CAS#-BEFORE-RAS# (CBR) refresh. This command is nonpersistent, so it must be issued each time a refresh is required. The addressing is generated by the internal refresh controller. This makes the address bits a "Don't Care" during an REFRESH command. The 256Mb DDR2 SDRAM requires REFRESH cycles at an average interval of 7.8125µs (MAX). To allow for improved efficiency in scheduling and switching between tasks, some flexibility in the absolute refresh interval is provided. A maximum of eight REFRESH commands can be posted (to defer issuing of REFRESH commands) to any given DDR2 SDRAM, meaning that the maximum absolute interval between any REFRESH command and the next REFRESH command is 9 × 7.8125µs (70.3µs). The REFRESH period begins when the REFRESH command is registered and ends ^{t}RFC (MIN) later.

Figure 44: Refresh Mode



Notes:
1. PRE = PRECHARGE, ACT = ACTIVE, AR = REFRESH, RA = row address, BA = bank address.
2. NOP commands are shown for ease of illustration; other valid commands may be possible at these times. CKE must be active during clock positive transitions.
3. "Don't Care" if A10 is HIGH at this point; A10 must be HIGH if more than one bank is active (i.e., must precharge all active banks).
4. DM, DQ, and DQS signals are all "Don't Care"/High-Z for operations shown.
5. The second REFRESH is not required and is only shown as an example of two back-to-back REFRESH commands.

Power-Down Mode

DDR2 SDRAMs support multiple power-down modes that allow significant power savings over normal operating modes. CKE is used to enter and exit different power-down modes. Power-down entry and exit timings are shown in Figure 45 on page 65. Detailed power-down entry conditions are shown in Figure 46 through Figure 53. The CKE Truth Table, Table 11, is shown on page 66.

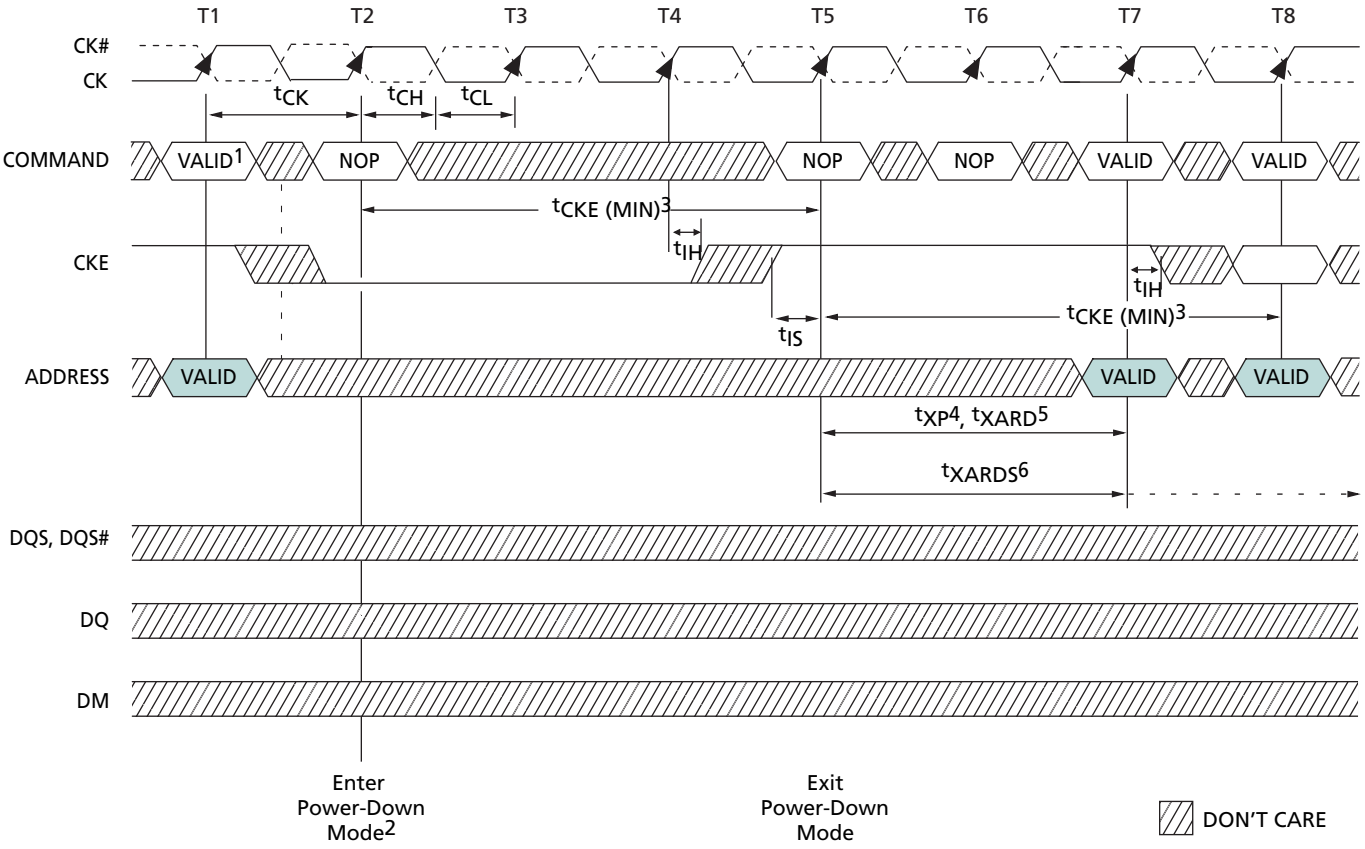
DDR2 SDRAMs require CKE to be registered HIGH (active) at all times that an access is in progress: from the issuing of a READ or WRITE command until completion of the burst. Thus a clock suspend is not supported. For READs, a burst completion is defined when the read postamble is satisfied; for WRITEs, a burst completion is defined when the write postamble and ^{t}WR or ^{t}WTR are satisfied, as shown in Figures 48 and 49 on page 68. The number of clock cycles required to meet ^{t}WTR is either 2 or ^{t}WTR/^{t}CK, whichever is greater.

Power-down (Figure 45) is entered when CKE is registered LOW coincident with a NOP or DESELECT command. CKE is not allowed to go LOW during a mode register or extended mode register command time, or while a READ or WRITE operation is in progress. If power-down occurs when all banks are idle, this mode is referred to as precharge power-down. If power-down occurs when there is a row active in any bank, this mode is referred to as active power-down. Entering power-down deactivates the input and output buffers, excluding CK, CK#, ODT, and CKE. For maximum power savings, the DLL is frozen during precharge power-down. Exiting active power-down requires the device to be at the same voltage and frequency as when it entered power-down. Exiting precharge power-down requires the device to be at the same voltage as when it entered power-down; however, the clock frequency is allowed to change. See "Precharge Power-Down Clock Frequency Change" on page 6

The maximum duration for either active or precharge power-down is limited by the refresh requirements of the device ^{t}RFC (MAX). The minimum duration for power-down entry and exit is limited by ^{t}CKE (MIN) parameter. While in power-down mode, CKE LOW, a stable clock signal, and stable power supply signals must be maintained at the inputs of the DDR2 SDRAM, while all other input signals are “Don’t Care” except ODT. Detailed ODT timing diagrams for different power-down modes are shown in Figures 81 through 86.

The power-down state is synchronously exited when CKE is registered HIGH (in conjunction with a NOP or DESELECT command), as shown in Figure 45 on page 65.

Figure 45: Power-Down



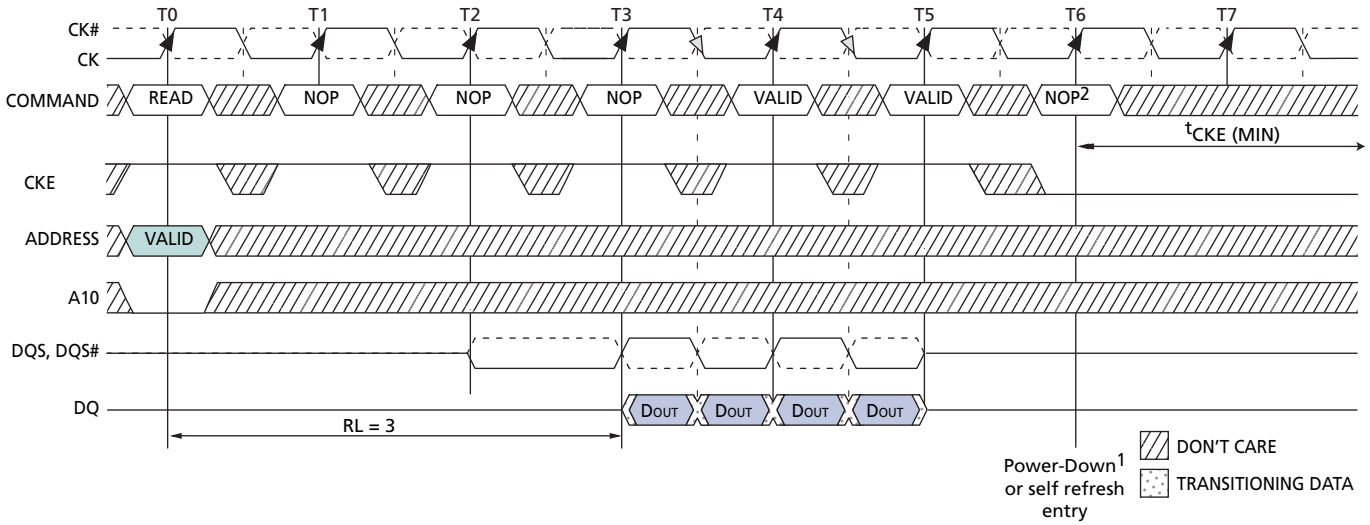
Notes:
1. If this command is a PRECHARGE (or if the device is already in the idle state), then the power-down mode shown is precharge power-down. If this command is an ACTIVE (or if at least one row is already active), then the power-down mode shown is active power-down.
2. No column accesses are allowed to be in progress at the time power-down is entered. If the DLL was not in a locked state when CKE went LOW, the DLL must be reset after exiting power-down mode for proper READ operation.
3. ^{t}CKE (MIN) of three clocks means CKE must be registered on three consecutive positive clock edges. CKE must remain at the valid input level the entire time it takes to achieve the three clocks of registration. Thus, after any CKE transition, CKE may not transition from its valid level during the time period of ^{t}IS + 2 x ^{t}CK + ^{t}IH. CKE must not transition during its ^{t}IS and ^{t}IH window.
4. ^{t}XP timing is used for exit precharge power-down and active power-down to any non-READ command.
5. ^{t}XARD timing is used for exit active power-down to READ command if fast exit is selected via MR (bit 12 = 0).
6. ^{t}XARDS timing is used for exit active power-down to READ command if slow exit is selected via MR (bit 12 = 1).

Table 11: CKE Truth Table
Notes 1–3, 12

Current State	CKE		Command (*n*) CS#, RAS#, CAS#, WE#	Action (*n*)	Notes
	Previous Cycle (*n*-1)	Current Cycle (*n*)			
Power down	L	L	X	Maintain power-down	13, 14
	L	H	DESELECT or NOP	Power-Down Exit	4, 8
Self refresh	L	L	X	Maintain self refresh	14
	L	H	DESELECT or NOP	Self refresh exit	4, 5, 9
Bank(s) active	H	L	DESELECT or NOP	Active power-down Entry	4, 8, 10, 11
All banks idle	H	L	DESELECT or NOP	Precharge power-downdntry	4, 8, 10
	H	L	REFRESH	Self refresh entry	6, 9, 11
	H	H	Shown in Table 6 on page 1.		7

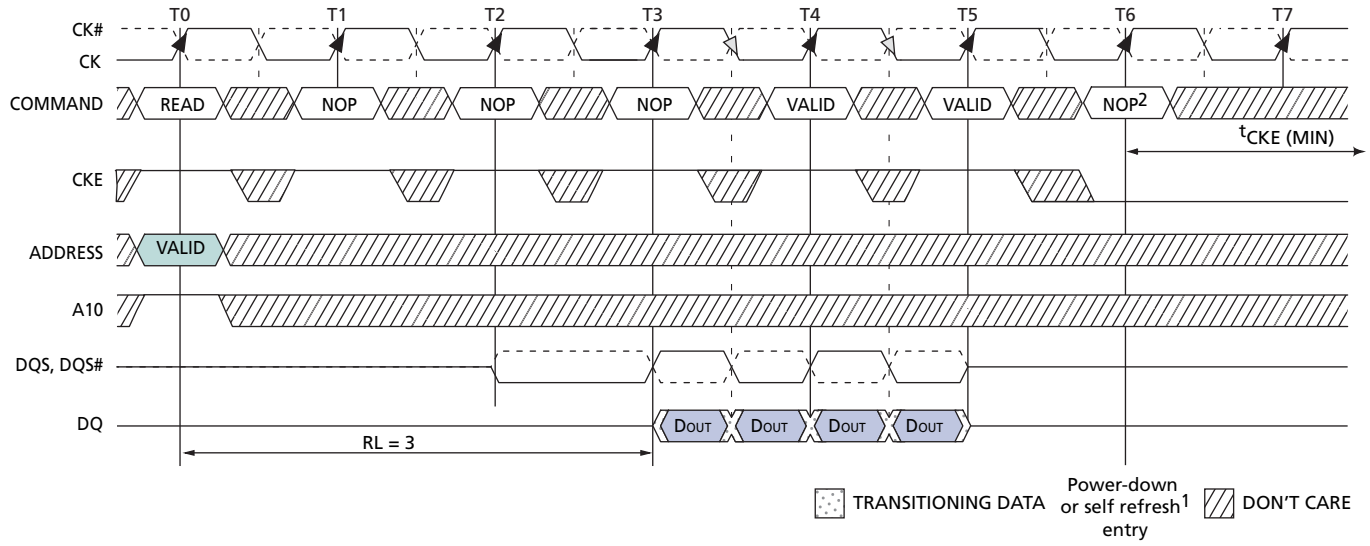
Notes:
1. CKE (*n*) is the logic state of CKE at clock edge *n*; CKE (*n*-1) was the state of CKE at the previous clock edge.
2. Current state is the state of the DDR2 SDRAM immediately prior to clock edge *n*.
3. Command (*n*) is the command registered at clock edge *n*, and action (*n*) is a result of command (*n*).
4. All states and sequences not shown are illegal or reserved unless explicitly described elsewhere in this document.
5. On self refresh exit, DESELECT or NOP commands must be issued on every clock edge occurring during the ^{t}XSNR period. READ commands may be issued only after ^{t}XSRD (200 clocks) is satisfied.
6. Self refresh mode can only be entered from the all banks idle state.
7. Must be a legal command as defined in the Command Truth Table, Table 6 on page 1.
8. Valid commands for power-down entry and exit are NOP and DESELECT only.
9. Valid commands for self refresh exit are NOP and DESELECT only.
10. Power-down and self refresh can not be entered while READ or WRITE operations, LOAD MODE operations, or PRECHARGE operations are in progress. See "Power-Down Mode" on page 64 and See "Self Refresh" on page 61 for a list of detailed restrictions.
11. Minimum CKE HIGH time is ^{t}CKE = 3 x ^{t}CK. Minimum CKE LOW time is ^{t}CKE = 3 x ^{t}CK. This requires a minimum of 3 clock cycles of registration.
12. The state of ODT does not affect the states described in this table. The ODT function is not available during self refresh. See "On-Die Termination (ODT)" on page 12 for more details and specific restrictions.
13. Power-down modes do not perform any REFRESH operations. The duration of power-down mode is therefore limited by the refresh requirements.
14. "X" means "Don't Care" (including floating around V_{REF}) in self refresh and power-down. However, ODT must be driven HIGH or LOW in power-down if the ODT function is enabled via EMR(1).

Figure 46: READ to Power-Down or Self Refresh Entry



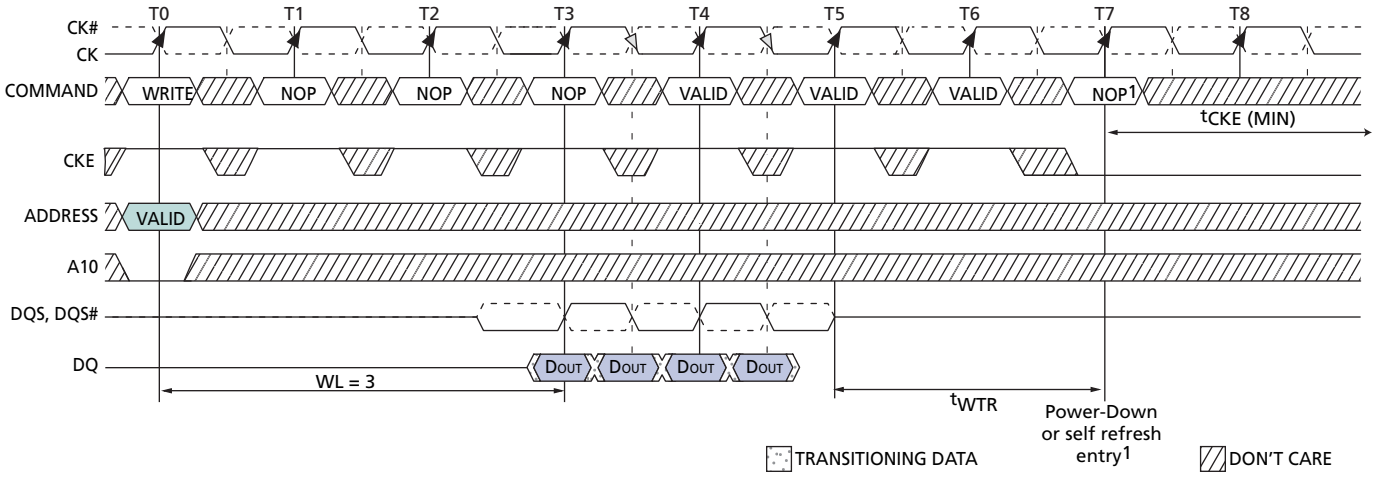
Notes: 1. Power-down or self refresh entry may occur after the READ burst completes.
2. In the example shown, READ burst completes at T5; earliest power-down or self refresh entry is at T6.

Figure 47: READ with Auto Precharge to Power-Down or Self Refresh Entry



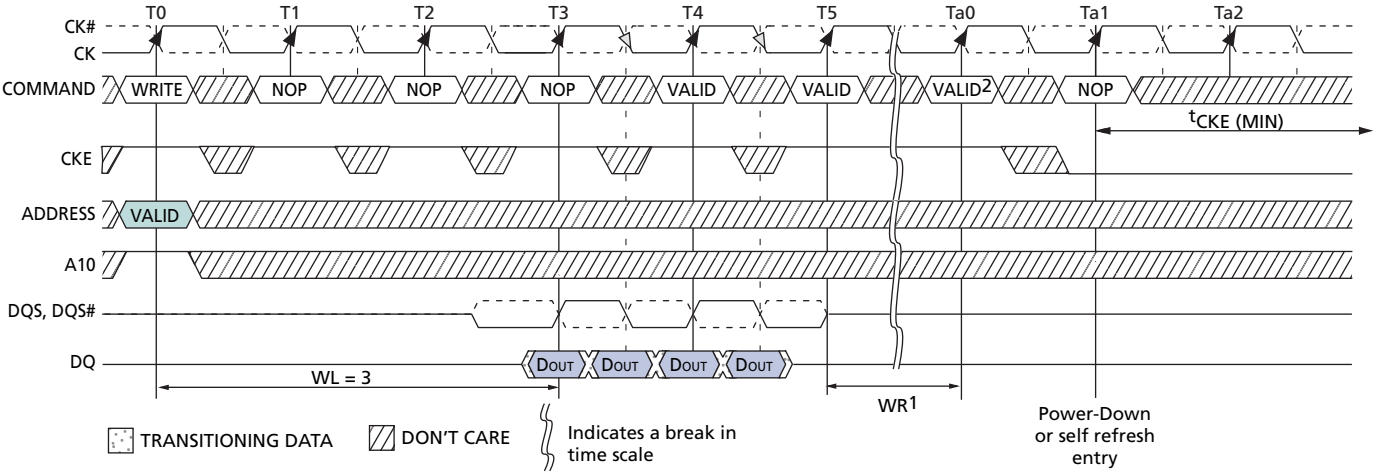
Notes: 1. Power-down or self refresh entry may occur after the READ burst completes.
2. In the example shown, READ burst completes at T5; earliest power-down or self refresh entry is at T6.

Figure 48: WRITE to Power-Down or Self-Refresh Entry



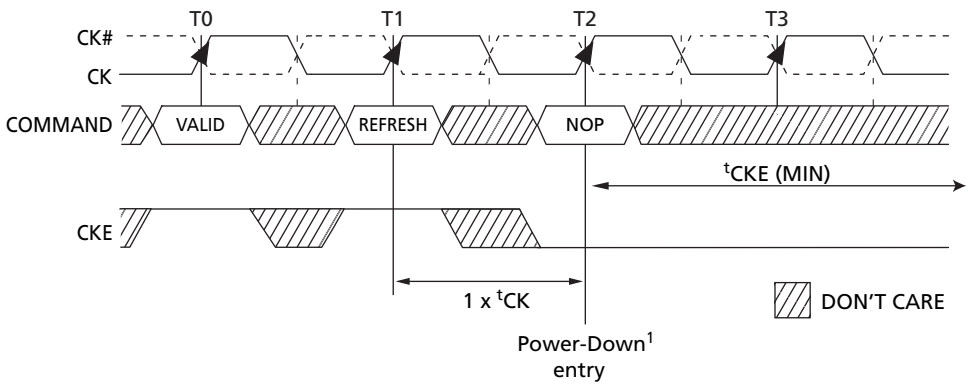
Notes: 1. Power-down or self refresh entry may occur after the WRITE burst completes.

Figure 49: WRITE with Auto Precharge to Power-Down or Self Refresh Entry



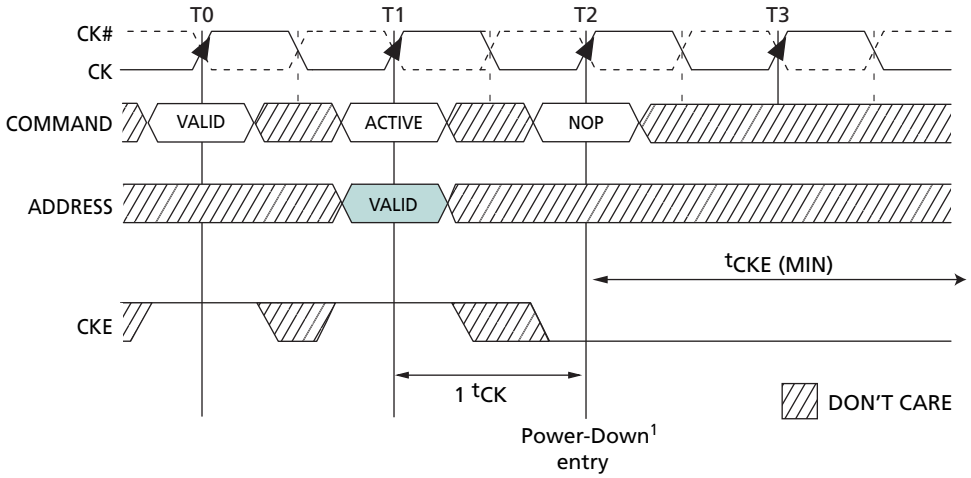
Notes: 1. WR is programmed through MR[9, 10, 11] and represents (^{t}WR [MIN] ns / ^{t}CK) rounded up to next integer ^{t}CK.
2. Internal PRECHARGE occurs at Ta0 when WR has completed; power-down entry may occur 1 x ^{t}CK later at Ta1 prior to ^{t}RP being satisfied.

Figure 50: REFRESH Command to Power-Down Entry



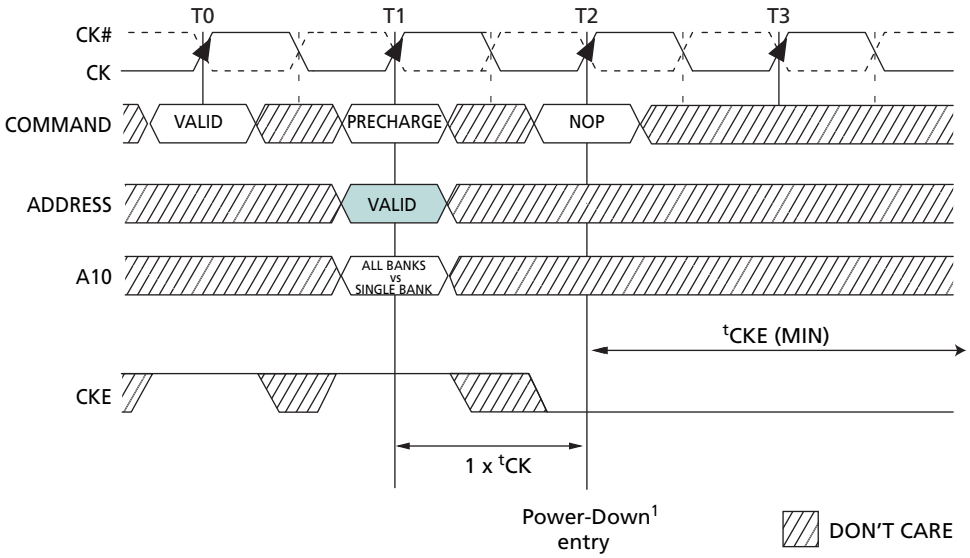
Notes: 1. The earliest PRECHARGE power-down entry may occur is at T2 which is 1 x ^{t}CK after the REFRESH command. Precharge power down entry occurs prior to ^{t}RFC (MIN) being satisfied.

Figure 51: ACTIVE Command to Power-Down Entry



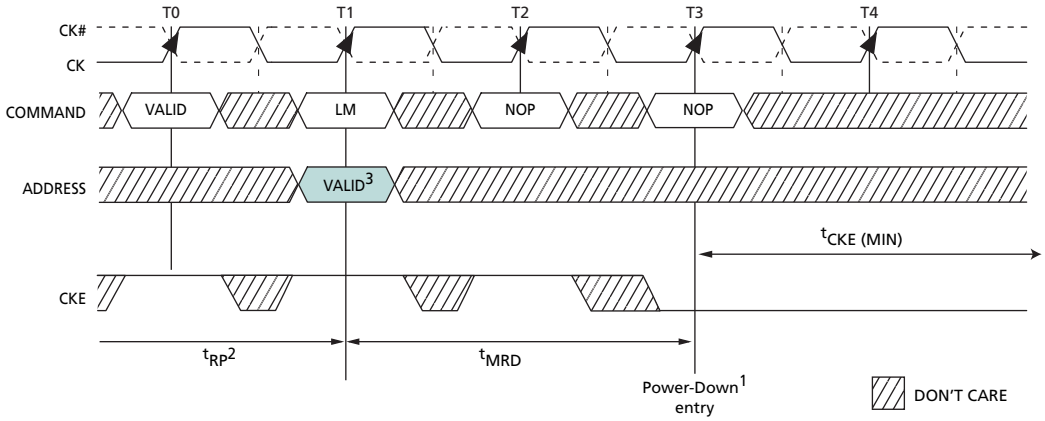
Notes: 1. The earliest PRECHARGE power-down entry may occur is at T2, which is 1 x ^{t}CK after the ACTIVE command. Active power-down entry occurs prior to ^{t}RCD (MIN) being satisfied.

Figure 52: PRECHARGE Command to Power-Down Entry



Notes: 1. The earliest power-down entry may occur is at T2, which is 1 x ^{t}CK after the PRECHARGE command. Power-down entry occurs prior to ^{t}RP (MIN) being satisfied.

Figure 53: LOAD MODE Command to Power-Down Entry

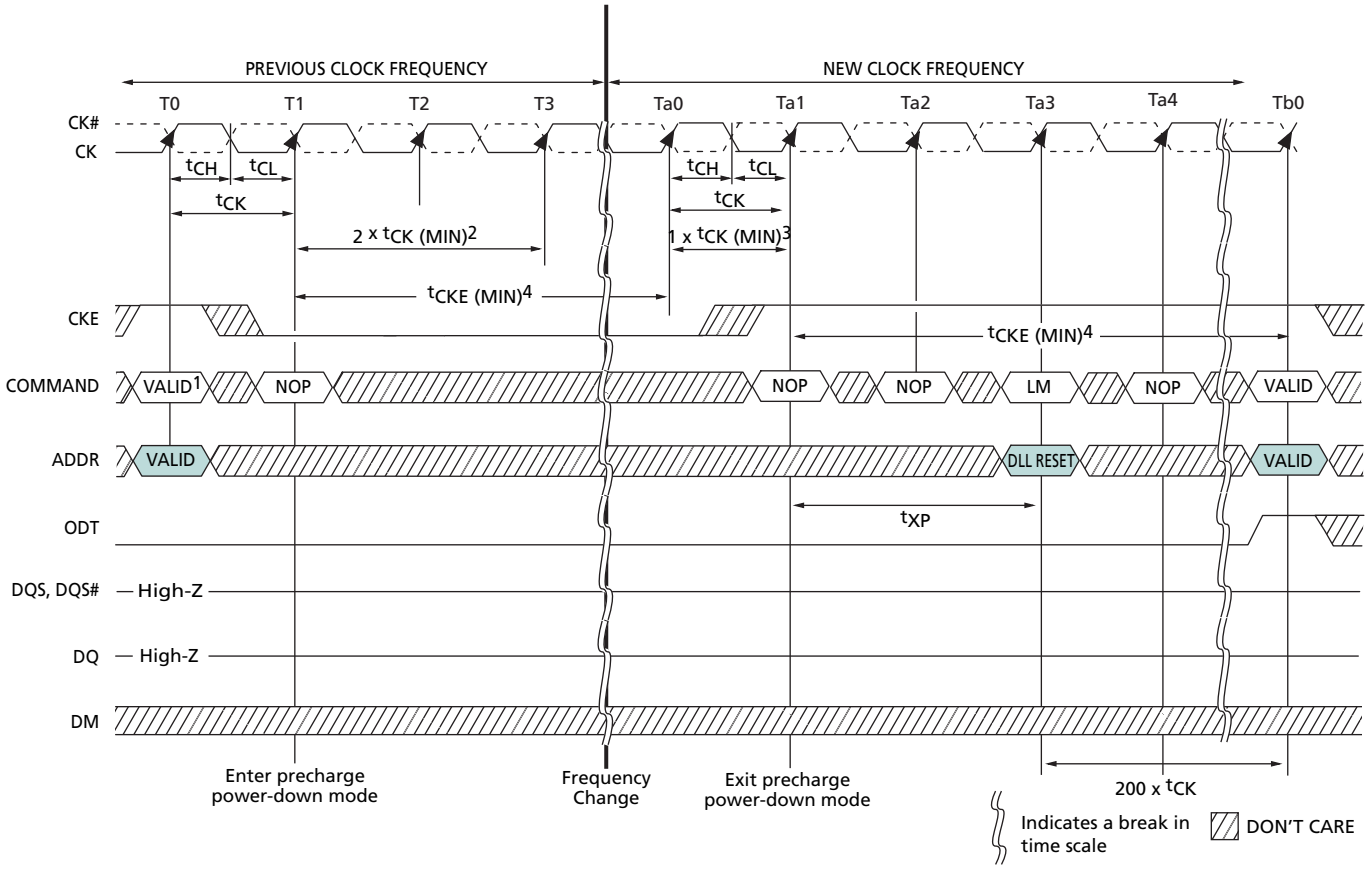


Notes: 1. The earliest PRECHARGE power-down entry is at T3, which is after ^{t}MRD is satisfied.
2. All banks must be in the precharged state and ^{t}RP met prior to issuing LM command.
3. Valid address for LM command includes MR, EMR, EMR(2), and EMR(3) registers.

Precharge Power-Down Clock Frequency Change

When the DDR2 SDRAM is in precharged power-down mode, ODT must be turned off and CKE must be at a logic LOW level. A minimum of two differntial clock cycles must pass after CKE goes LOW before clock frequency may change. The device input clock frequency is allowed to change only within minimum and maximum operating frequencies specified for the particular speed grade. During input clock frequency change, ODT and CKE must be held at stable LOW levels. Once the input clock frequency is changed, new stable clocks must be provided to the device before precharge power-down may be exited, and DLL must be reset via EMR after precharge power-down exit. Depending on the new clock frequency, an additional LM command might be required to appropriately set the WR MR[11, 10, 9]. During the DLL relock period of 200 cycles, ODT must remain off. After the DLL lock time, the DRAM is ready to operate with a new clock frequency.

Figure 54: Input Clock Frequency Change During PRECHARGE Power Down Mode



Notes:
1. If this command is a PRECHARGE (or if the device is already in the idle state), then the power-down mode shown is precharge power-down, which is required prior to the clock frequency change.
2. A minimum of 2 x ^{t}CK is required after entering precharge power-down prior to changing clock frequencies.
3. Once the new clock frequency has changed and is stable, a minimum of 1 x ^{t}CK is required prior to exiting precharge power-down.
4. Minimum CKE HIGH time is ^{t}CKE = 3 x ^{t}CK. Minimum CKE LOW time is ^{t}CKE = 3 x ^{t}CK. This requires a minimum of three clock cycles of registration.

RESET Function

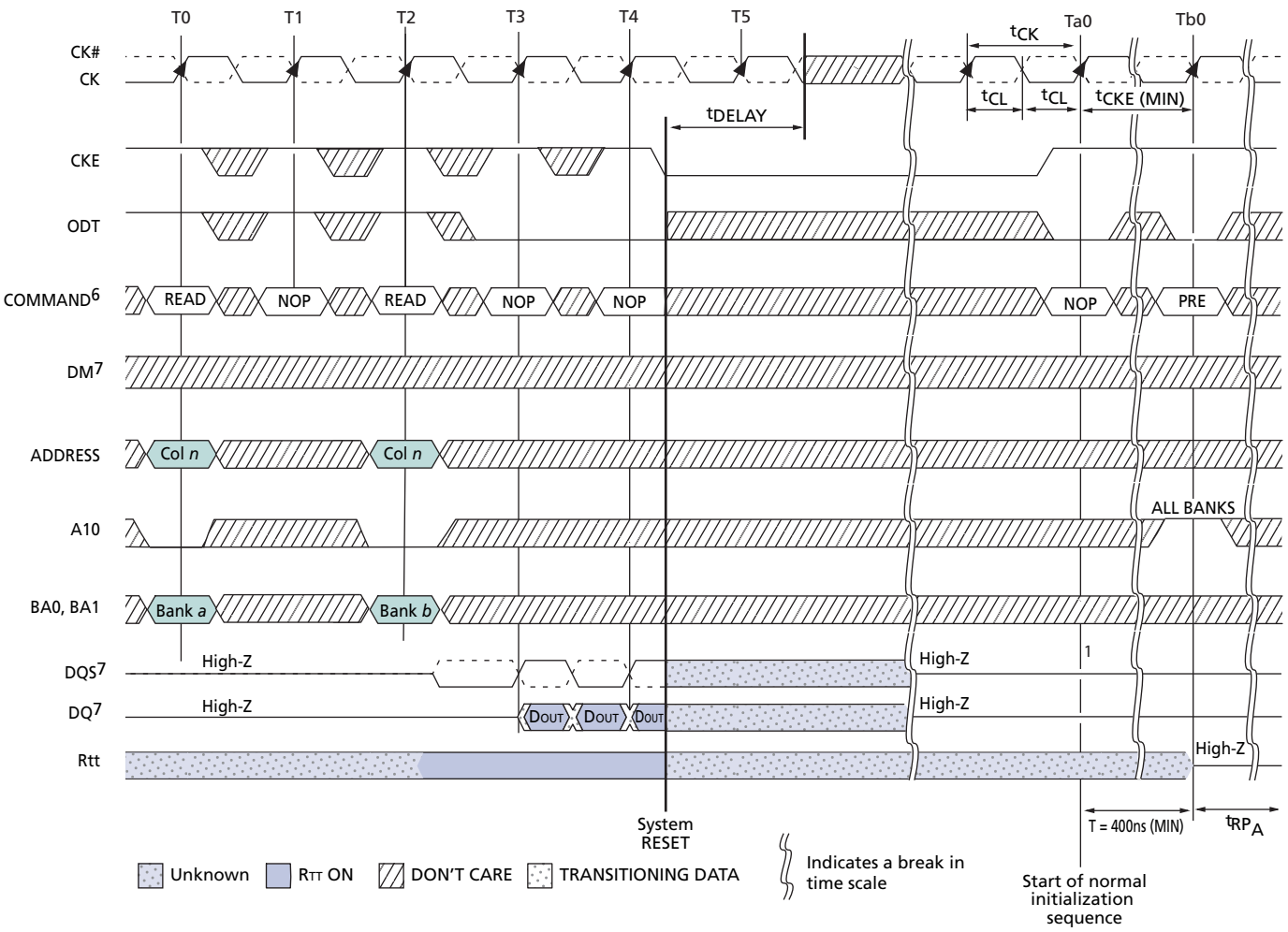
(CKE LOW Anytime)

DDR2 SDRAM applications may go into a reset state at any time during normal operation. If an application enters a reset condition, CKE is used to ensure the DDR2 SDRAM device resumes normal operation after re-initializing. All data will be lost during a reset condition; however, the DDR2 SDRAM device will continue to operate properly if the following conditions outlined in this section are satisfied.

The reset condition defined here assumes all supply voltages (V_{DD}, $V_{DD}Q$, $V_{DD}L$, and V_{REF}) are stable and meet all DC specifications prior to, during, and after the RESET operation. All other input pins of the DDR2 SDRAM device are a "Don't Care" during RESET with the exception of CKE.

If CKE asynchronously drops LOW during any valid operation (including a READ or WRITE burst), the memory controller must satisfy the timing parameter ^{t}DELAY before turning off the clocks. Stable clocks must exist at the CK, CK# inputs of the DRAM before CKE is raised HIGH, at which time the normal initialization sequence must occur. See "Initialization" on page 3t. The DDR2 SDRAM device is now ready for normal operation after the initialization sequence. Figure 55 on page 73 shows the proper sequence for a RESET operation.

Figure 55: RESET Function



Notes: 1. In certain cases where a READ cycle is interrupted, CKE going HIGH may result in the completion of the burst.
2. Initialization timing is shown in Figure 12 on page 5.

ODT Timing

Once a 12ns delay (^{t}MOD) has been satisfied, after the ODT function has been enabled via the EMR LOAD MODE command, ODT can be accessed under two timing categories. ODT will operate in either synchronous mode or asynchronous mode, depending on the state of CKE. ODT can switch anytime except during self refresh mode and a few clocks after being enabled via EMR, as shown in Figure 56 on page 75.

There are two timing categories for ODT—turn-on and turn-off. During active mode (CKE HIGH) and fast-exit power-down mode (any row of any bank open, CKE LOW, MR[12 = 0]), ^{t}AOND, ^{t}AON, ^{t}AOFD, and ^{t}AOF timing parameters are applied, as shown in Figure 58 and Table 12 on page 76. During slow-exit power-down mode (any row of any bank open, CKE LOW, MR[12] = 1) and precharge power-down mode (all banks/rows precharged and idle, CKE LOW), ^{t}AONPD and ^{t}AOFPD timing parameters are applied, as shown in Figure 59 and Table 13 on page 77.

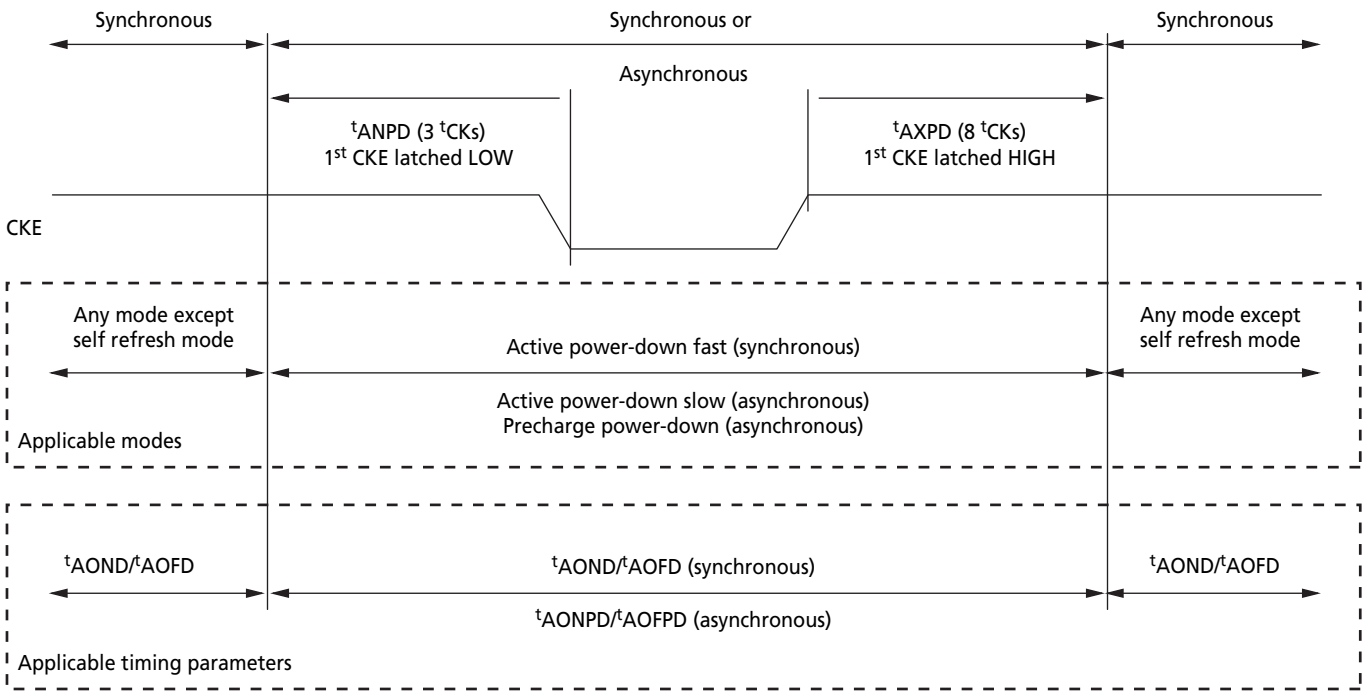
ODT turn-off timing, prior to entering any power-down mode, is determined by the parameter ^{t}ANPD (MIN), shown in Figure 60 on page 78. At state T2, the ODT HIGH signal satisfies ^{t}ANPD (MIN) prior to entering power-down mode at T5. When ^{t}ANPD (MIN) is satisfied, ^{t}AOFD and ^{t}AOF timing parameters apply. Figure 60 on page 78 also shows the example where ^{t}ANPD (MIN) is ***not*** satisfied since ODT HIGH does not occur until state T3. When ^{t}ANPD (MIN) is ***not*** satisfied, ^{t}AOFPD timing parameters apply.

ODT turn-on timing prior to entering any power-down mode is determined by the parameter ^{t}ANPD, as shown in Figure 61. At state T2, the ODT HIGH signal satisfies ^{t}ANPD (MIN) prior to entering power-down mode at T5. When ^{t}ANPD (MIN) is satisfied, ^{t}AOND and ^{t}AON timing parameters apply. Figure 61 also shows the example where ^{t}ANPD (MIN) is ***not*** satisfied since ODT HIGH does not occur until state T3. When ^{t}ANPD (MIN) is ***not*** satisfied, ^{t}AONPD timing parameters apply.

ODT turn-off timing after exiting any power-down mode is determined by the parameter ^{t}AXPD (MIN) shown in Figure 62. At state Ta1, the ODT LOW signal satisfies ^{t}AXPD (MIN) after exiting power-down mode at state T1. When ^{t}AXPD (MIN) is satisfied, ^{t}AOFD and ^{t}AOF timing parameters apply. Figure 62 also shows the example where ^{t}AXPD (MIN) is ***not*** satisfied since ODT LOW occurs at state Ta0. When ^{t}AXPD (MIN) is NOT satisfied, ^{t}AOFPD timing parameters apply.

ODT turn-on timing after exiting either slow-exit power-down mode or precharge power-down mode is determined by the parameter ^{t}AXPD (MIN) shown in Figure 63. At state Ta1, the ODT HIGH signal satisfies ^{t}AXPD (MIN) after exiting power-down mode at state T1. When ^{t}AXPD (MIN) is satisfied, ^{t}AOND and ^{t}AON timing parameters apply. Figure 63 also shows the example where ^{t}AXPD (MIN) is NOT satisfied since ODT HIGH occurs at state Ta0. When ^{t}AXPD (MIN) is NOT satisfied, ^{t}AONPD timing parameters apply.

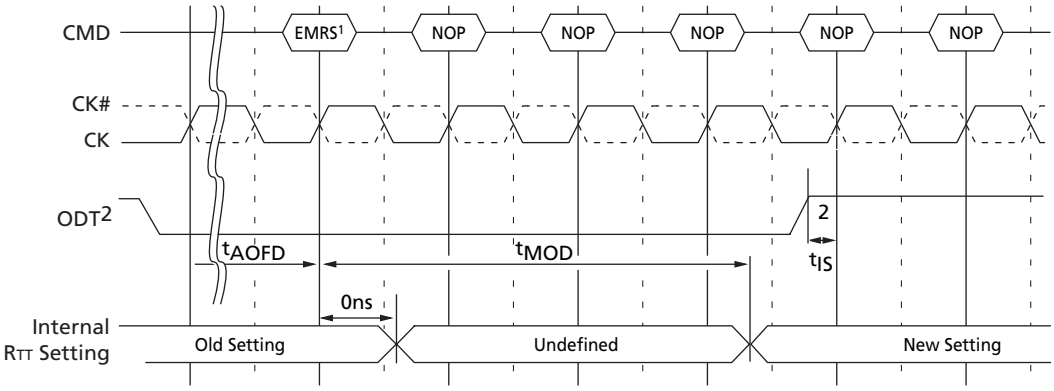
Figure 56: ODT Timing for Entering and Exiting Power-Down Mode



MRS Command to ODT Update Delay

During normal operation, the value of the effective termination resistance can be changed with an EMRS set command. ^{t}MOD (MAX) updates the RTT setting.

Figure 57: MRS Command to ODT Update Delay



Notes: 1. LM command directed to mode register, which updates the information in EMR(1)[A6, A2], i.e. RTT (nominal).
2. To prevent any impedance glitch on the channel, the following conditions must be met: ^{t}AOFD must be met before issuing the LM command; ODT must remain LOW for the entire duration of the ^{t}MOD window, until ^{t}MOD is met.

Figure 58: ODT Timing for Active or Fast-Exit Power-Down Mode

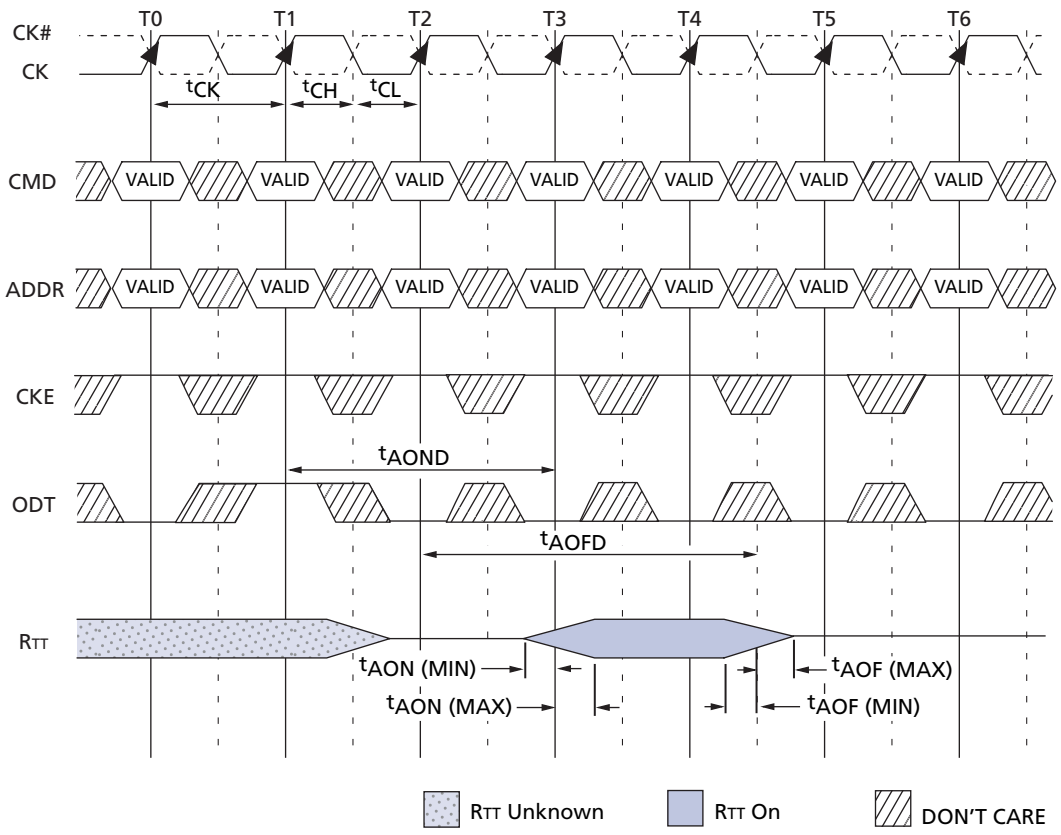


Table 12: DDR2-400/533 ODT Timing for Active and Fast-Exit Power-Down Modes

Parameter	Symbol	Min	Max	Units
ODT turn-on delay	^{t}AOND	2	2	^{t}CK
ODT turn-on	^{t}AON	^{t}AC (MIN)	^{t}AC (MAX) + 1,000	ps
ODT turn-off delay	^{t}AOFD	2.5	2.5	^{t}CK
ODT turn-off	^{t}AOF	^{t}AC (MIN)	^{t}AC (MAX) + 600	ps

Note: The half-clock of ^{t}AOFD's 2.5 ^{t}CK assumes a 50/50 clock duty cycle. This half-clock value must be derated by the amount of half-clock duty cycle error. For example, if the clock duty cycle was 47/53, ^{t}AOFD would actually be 2.5 - 0.03, or 2.47 for ^{t}AOF (MIN) and 2.5 + 0.03 or 2.53 for^{t}AOF (MAX).

Figure 59: ODT timing for Slow-Exit or Precharge Power-Down Modes

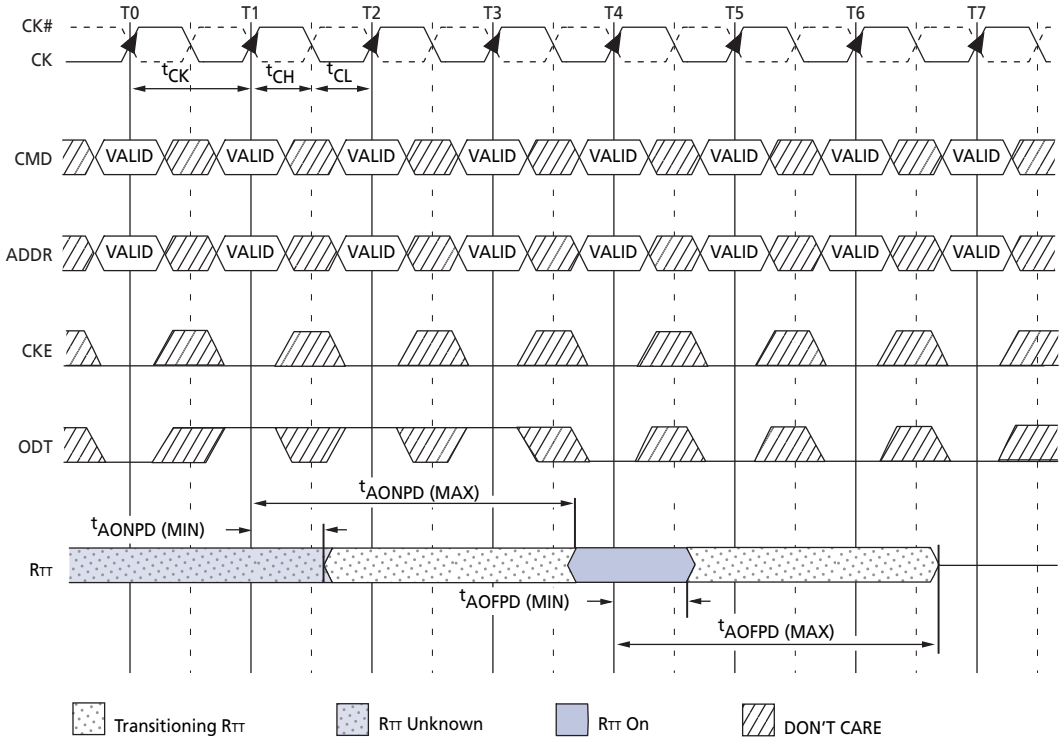


Table 13: DDR2-400/533 ODT timing for Slow-Exit and Precharge Power-Down Modes

Parameter	Symbol	Min	Max	Units
ODT turn-on (power-down mode)	^{t}AONPD	^{t}AC (MIN) + 2,000	2 x ^{t}CK + ^{t}AC (MAX) + 1,000	ps
ODT turn-off (power-down mode)	^{t}AOFPD	^{t}AC (MIN) + 2,000	2.5 x ^{t}CK + ^{t}AC (MAX) + 1,000	ps

Figure 60: ODT Turn-Off Timings when Entering Power-Down Mode

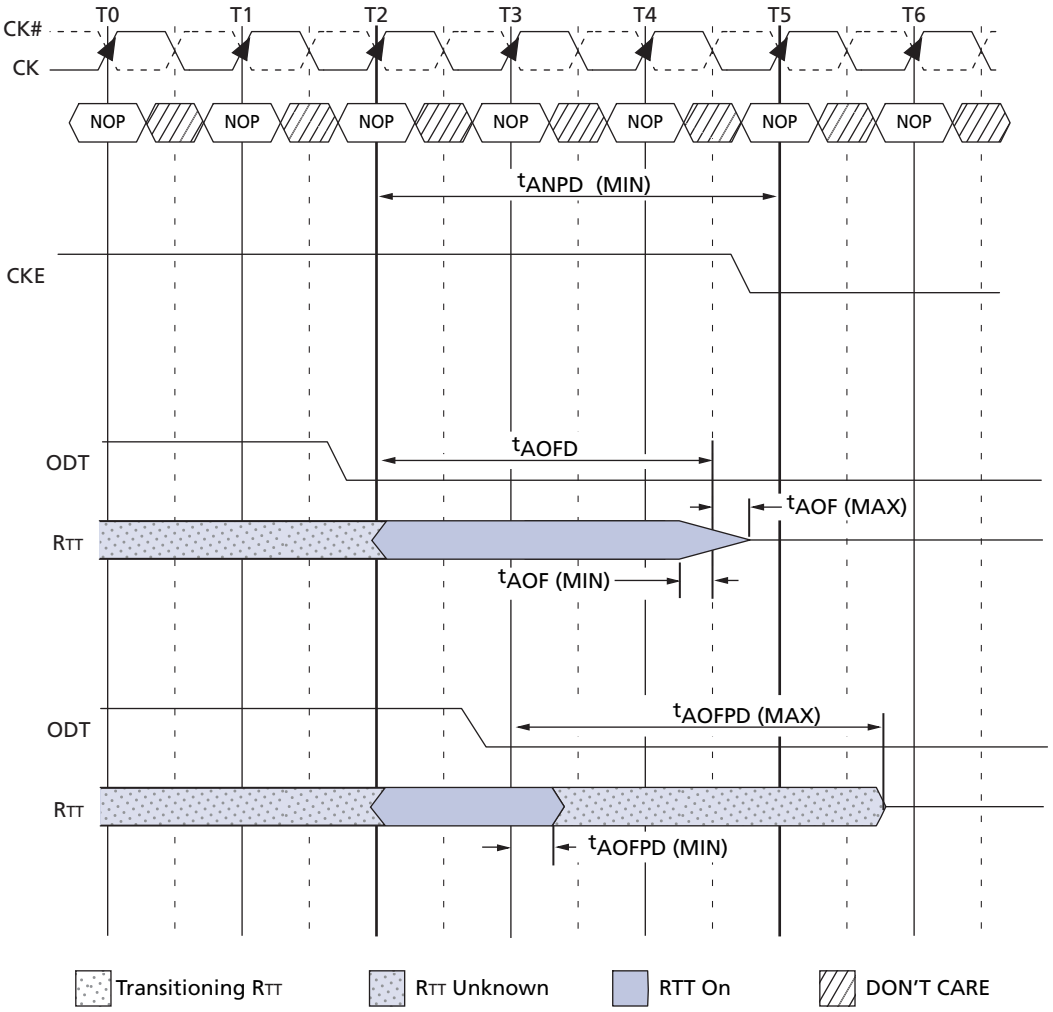


Table 14: DDR2-400/533 ODT Turn-Off Timings when Entering Power-Down Mode

Parameter	Symbol	Min	Max	Units
ODT turn-off delay	^{t}AOFD	2.5	2.5	^{t}CK
ODT turn-off	^{t}AOF	^{t}AC (MIN)	^{t}AC (MAX) + 600	ps
ODT turn-off (power-down mode)	^{t}AOFPD	^{t}AC (MIN) + 2,000	2.5 x ^{t}CK + ^{t}AC (MAX) + 1,000	ps
ODT to power-down entry latency	^{t}ANPD	3		^{t}CK

Note: The half-clock of ^{t}AOFD's 2.5 ^{t}CK assumes a 50/50 clock duty cycle. This half-clock value must be derated by the amount of half-clock duty cycle error. For example, if the clock duty cycle was 47/53, ^{t}AOFD would actually be 2.5 - 0.03, or 2.47 for ^{t}AOF (MIN) and 2.5 + 0.03 or 2.53 for ^{t}AOF (MAX).

Figure 61: ODT Turn-On Timing when Entering Power-Down Mode

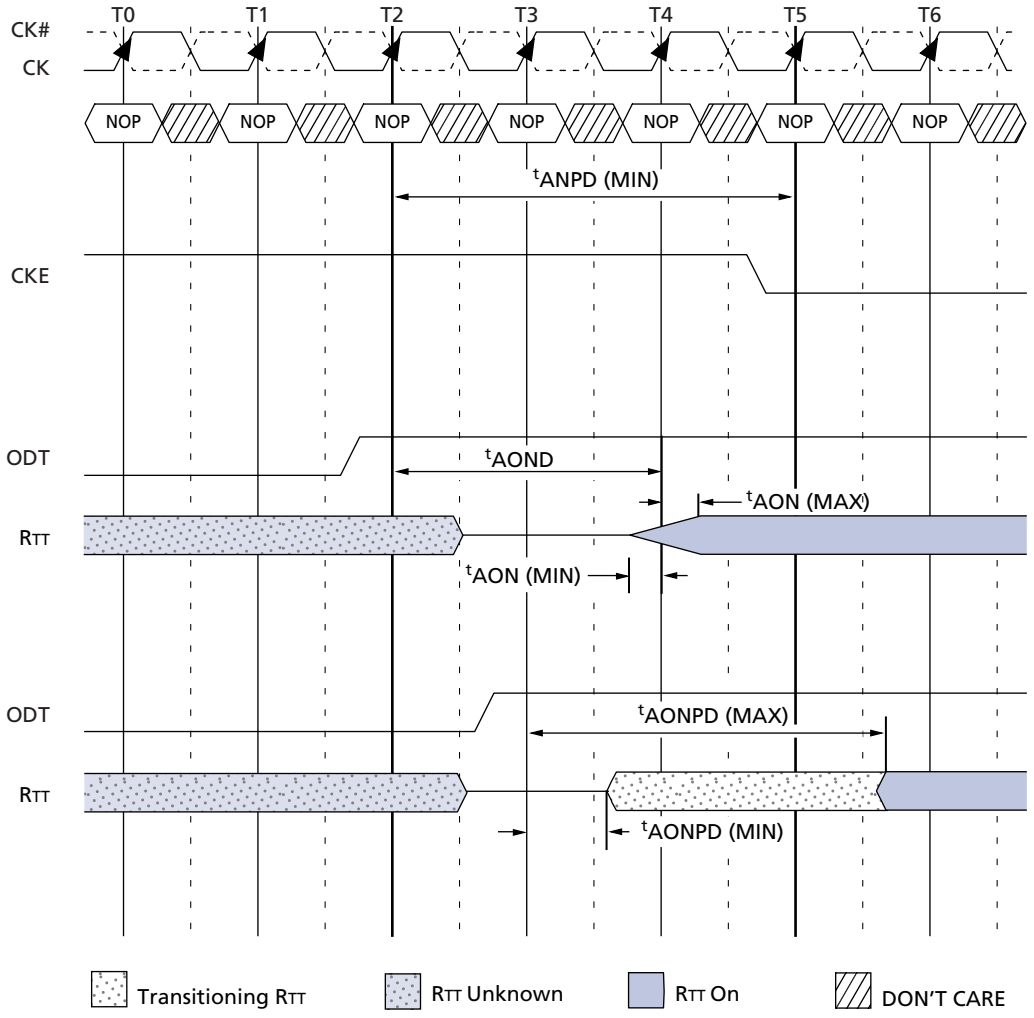


Table 15: DDR2-400/533 ODT Turn-On Timing when Entering Power-Down Mode

Parameter	Symbol	Min	Max	Units
ODT turn-on delay	^{t}AOND	2	2	^{t}CK
ODT turn-on	^{t}AON	^{t}AC (MIN)	^{t}AC (MAX) + 1,000	ps
ODT turn-on (power-down mode)	^{t}AONPD	^{t}AC (MIN) + 2,000	2 x ^{t}CK + ^{t}AC (MAX) + 1,000	ps
ODT to power-down entry latency	^{t}ANPD	3		^{t}CK

Figure 62: ODT Turn-Off Timing when Exiting Power-Down Mode

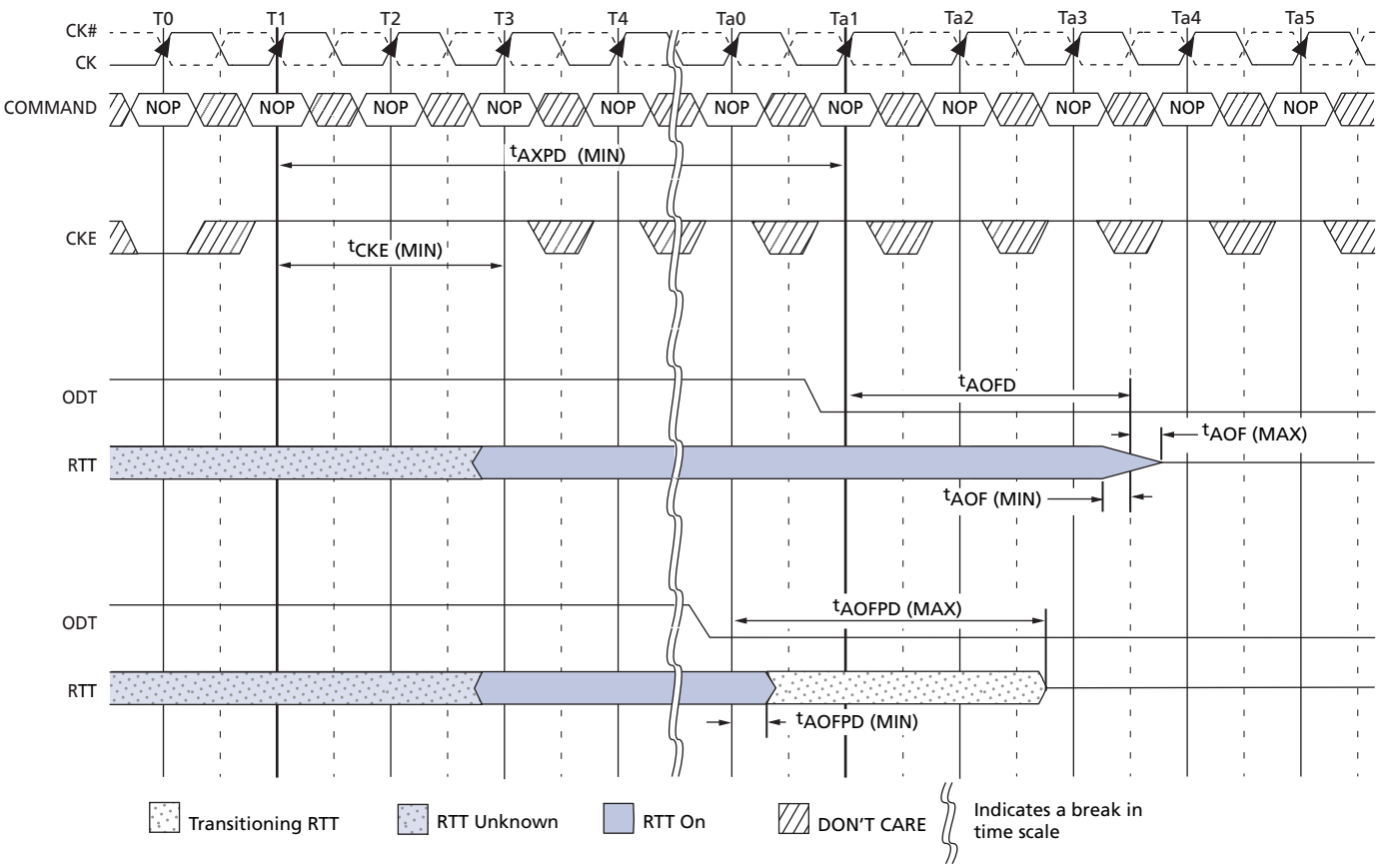


Table 16: DDR2-400/533 ODT Turn-Off Timing when Exiting Power-Down Mode

Parameter	Symbol	Min	Max	Units
ODT turn-off delay	^{t}AOFD	2.5	2.5	^{t}CK
ODT turn-off	^{t}AOF	^{t}AC (MIN)	^{t}AC (MAX) + 600	ps
ODT turn-off (power-down mode)	^{t}AOFPD	^{t}AC (MIN) + 2,000	2.5 x ^{t}CK + ^{t}AC (MAX) + 1,000	ps
ODT to power-down exit latency	^{t}AXPD	8		^{t}CK

Note: The half-clock of ^{t}AOFD's 2.5 ^{t}CK assumes a 50/50 clock duty cycle. This half-clock value must be derated by the amount of half-clock duty cycle error. For example, if the clock duty cycle was 47/53, ^{t}AOFD would actually be 2.5 - 0.03, or 2.47 for ^{t}AOF (MIN) and 2.5 + 0.03 or 2.53 for ^{t}AOF (MAX).

Figure 63: ODT Turn-On Timing when Exiting Power-Down Mode

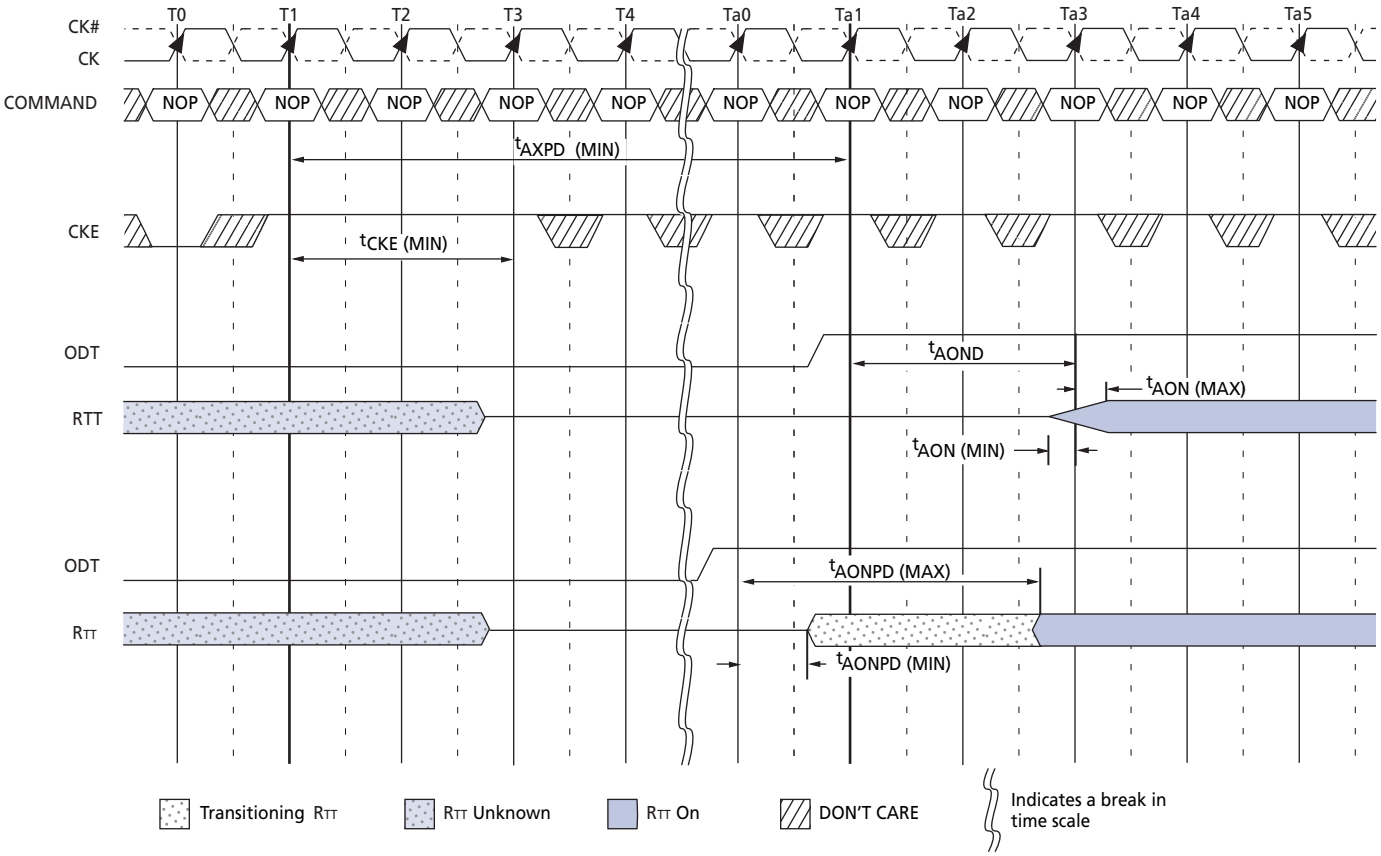


Table 17: DDR2-400/533 ODT Turn-On Timing when Exiting Power-Down Mode

Parameter	Symbol	Min	Max	Units
ODT turn-on delay	tAOND	2	2	tCK
ODT turn-on	tAON	tAC (MIN)	tAC (MAX) + 1,000	ps
ODT turn-on (power-down mode)	tAONPD	tAC (MIN) + 2,000	2 x tCK + tAC (MAX) + 1,000	ps
ODT to power-down exit latency	tAXPD	8		tCK

Absolute Maximum Ratings

Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Table 17: Absolute Maximum DC Ratings

Parameter	Symbol	Min	Max	Units	Notes
VDD supply voltage relative to VSS	VDD	-1.0	2.3	V	1
VDDQ supply voltage relative to VSSQ	VDDQ	-0.5	2.3	V	1, 2
VDDL supply voltage relative to VSSL	VDDL	-0.5	2.3	V	1
Voltage on any ball relative to VSS	VIN, VOUT	-0.5	2.3	V	3
Input leakage current; any input 0V ≤ VIN ≤ VDD; all other balls not under test = 0V)	I_I	-5	5	µA	
Output leakage current; 0V ≤ VOUT ≤ VDDQ; DQ and ODT disabled	I_{OZ}	-5	5	µA	
VREF leakage current; VREF = Valid VREF level	I_{VREF}	-2	2	µA	

Notes: 1. VDD, VDDQ, and VDDL must be within 300mV of each other at all times.
2. VREF ≤ 0.6 x VDDQ; however, VREF may be ≥ VDDQ provided that VREF ≤ 300mV.
3. Voltage on any I/O may not exceed voltage on VDDQ.

Temperature and Thermal Impedance

It is imperative that the DDR2 SDRAM device's temperature specifications, shown in Table 18 on page 83, be maintained in order to ensure the junction temperature is in the proper operating range to meet data sheet specifications. An important step in maintaining the proper junction temperature is using the device's thermal impedances correctly. The thermal impedances are listed in for the applicable die revision and packages being made available.

Incorrectly using thermal impedances can produce significant errors. Read Micron Technical Note TN-00-08, "Thermal Applications" prior to using the thermal impedances listed below. For designs that are expected to last several years and require the flexibility to use several designs, consider using final target theta values, rather than existing values, to account for larger thermal impedances.

The DDR2 SDRAM device's safe junction temperature range can be maintained when the T_C specification is not exceeded. In application where the device's ambient temperature is too high, use of forced air and/or heat sinks may be required in order to satisfy the case temperature specifications.

Table 18: Temperature Limits

Parameter	Symbol	Min	Max	Units	Notes
Storage temperature	T_{STG}	-55	100	°C	1
Operating temperature – commercial	T_C	0	85	°C	2, 3
Operating temperature – industrial	T_C	-40	95	°C	2, 3, 4
	T_{AMB}	-40	85	°C	4, 5

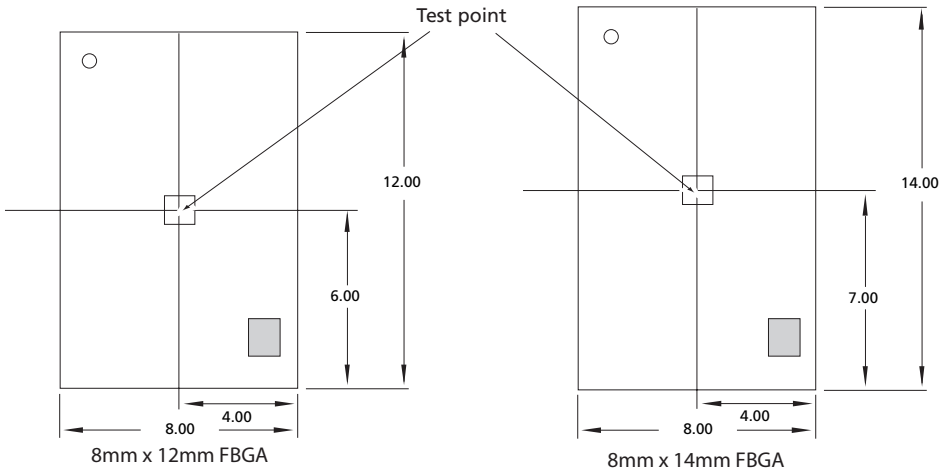
Notes: 1. MAX storage case temperature; T_{STG} is measured in the center of the package, as shown in Figure 64 on page 83. This case temperature limit is allowed to be exceeded briefly during package reflow, as noted in TN-00-11.
2. MAX operating case temperature; T_C is measured in the center of the package, as shown in Figure 64 on page 83.
3. Device functionality is not guaranteed if the device exceeds maximum T_C during operation.
4. Both temperature specifications must be satisfied.
5. Operating ambient temperature surrounding the package.

Table 19: Thermal Impedance

Die Rev	Package	Substrate	θ JA (°C/W) Airflow = 0m/s	θ JA (°C/W) Airflow = 1m/s	θ JA (°C/W) Airflow = 2m/s	θ JB (°C/W)	θ JB (°C/W)
B[1]	60-ball	2-layer	59.0	46.7	43.1	25	4.4
		4-layer	37.8	32.5	30.7	20.5	
	84-ball	2-layer	53.6	40.0	35.2	20.0	5.2
		4-layer	36.6	29.9	27.5	19.2	
Last shrink target[2]	60-ball	2-layer	60.0	48.0	45.0	27.0	5.0
		4-layer	39.0	34.0	32.0	22.0	
	84-ball	2-layer	55.0	42.0	37.0	22.0	6.0
		4-layer	38.0	32.0	30.0	21.0	

Notes: 1. Thermal resistance data is based on a number of samples from multiple lots and should be viewed as a typical number.
2. This is an estimate; simulated number and actual results could vary.

Figure 64: Example Temperature Test Point Location



AC and DC Operating Conditions

Table 20: Recommended DC Operating Conditions (SSTL_18)
All voltages referenced to V_{SS}

Parameter	Symbol	Min	Nom	Max	Units	Notes
Supply voltage	V_{DD}	1.7	1.8	1.9	V	1, 5
V_{DD}L supply voltage	V_{DD}L	1.7	1.8	1.9	V	4, 5
I/O supply voltage	V_{DD}Q	1.7	1.8	1.9	V	4, 5
I/O reference voltage	V_{REF}(DC)	0.49 x V_{DD}Q	0.50 x V_{DD}Q	0.51 x V_{DD}Q	V	2
I/O termination voltage (system)	V_{TT}	V_{REF}(DC) - 40	V_{REF}(DC)	V_{REF}(DC) + 40	mV	3

Notes:
1. V_{DD} and V_{DD}Q must track each other. V_{DD}Q must be ≤ V_{DD}.
2. V_{REF} is expected to equal V_{DD}Q/2 of the transmitting device and to track variations in the DC level of the same. Peak-to-peak noise (non-common mode) on V_{REF} may not exceed ±1 percent of the DC value. Peak-to-peak AC noise on V_{REF} may not exceed ±2 percent of V_{REF}(DC). This measurement is to be taken at the nearest V_{REF} bypass capacitor.
3. V_{TT} is not applied directly to the device. V_{TT} is a system supply for signal termination resistors, is expected to be set equal to V_{REF}, and must track variations in the DC level of V_{REF}.
4. V_{DD}Q tracks with V_{DD}; V_{DD}L tracks with V_{DD}.
5. VssQ = VssL = Vss

Table 21: ODT DC Electrical Characteristics
All voltages referenced to V_{SS}

Parameter	Symbol	Min	Nom	Max	Units	NOTES
R_{TT} effective impedance value for 75Ω setting EMR (A6, A2) = 0, 1	$R_{TT1(EFF)}$	60	75	90	Ω	1, 3
R_{TT} effective impedance value for 150Ω setting EMR (A6, A2) = 1, 0	$R_{TT2(EFF)}$	120	150	180	Ω	1, 3
R_{TT} effective impedance value for 50Ω setting EMR (A6, A2) = 1, 1	$R_{TT3(EFF)}$	40	50	60	Ω	1, 3
Deviation of VM with respect to V_{DD}Q/2	ΔVM	-6		6	%	2

Notes:
1. $R_{TT1(EFF)}$ and $R_{TT2(EFF)}$ are determined by separately applying $V_{IH(AC)}$ and $V_{IL(AC)}$ to the ball being tested, and then measuring current, $I(V_{IH(AC)})$ and $I(V_{IL(AC)})$, respectively.

$$R_{TT(EFF)} = \frac{V_{IH(AC)} - V_{IL(AC)}}{I(V_{IH(AC)}) - I(V_{IL(AC)})}$$

2. Measure voltage (VM) at tested ball with no load.

$$\Delta VM = \left(\frac{2 \times VM}{V_{DDQ}} - 1\right) \times 100$$

3. IT device minimum values are derated by six percent when device operates between -40°C and 0°C (T_C).

Input Electrical Characteristics and Operating Conditions

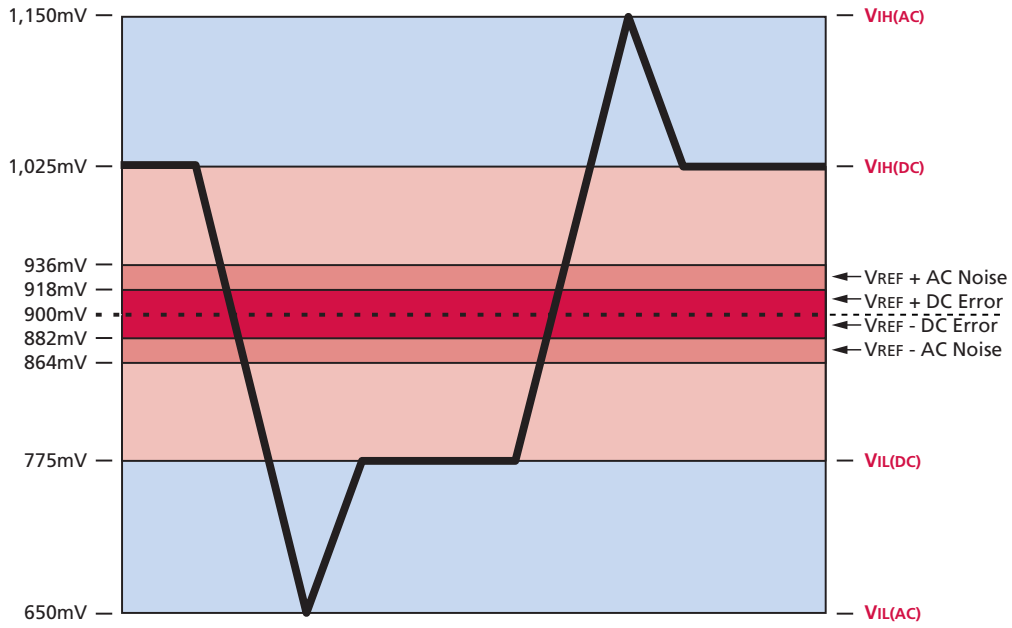
Table 22: Input DC Logic Levels
All voltages referenced to V_{SS}

Parameter	Symbol	Min	Max	Units
Input HIGH (logic 1) voltage	$V_{IH(DC)}$	$V_{REF(DC)}$ + 125	V_{DDQ} + 300	mV
Input LOW (logic 0) voltage	$V_{IL(DC)}$	-300	$V_{REF(DC)}$ - 125	mV

Table 23: Input AC Logic Levels
All voltages referenced to V_{SS}

Parameter	Symbol	Min	Max	Units
Input HIGH (logic 1) voltage (-5E/-37E)	$V_{IH(AC)}$	$V_{REF(DC)}$ + 250	-	mV
Input HIGH (logic 1) voltage (-3/-3E/-25E)	$V_{IH(AC)}$	$V_{REF(DC)}$ + 200	-	mV
Input LOW (logic 0) voltage (-5E/-37E)	$V_{IL(AC)}$	–	$V_{REF(DC)}$ - 250	mV
Input LOW (logic 0) voltage (-3/-3E/-25E)	$V_{IL(AC)}$	–	$V_{REF(DC)}$ - 200	mV

Figure 65: Single-Ended Input Signal Levels



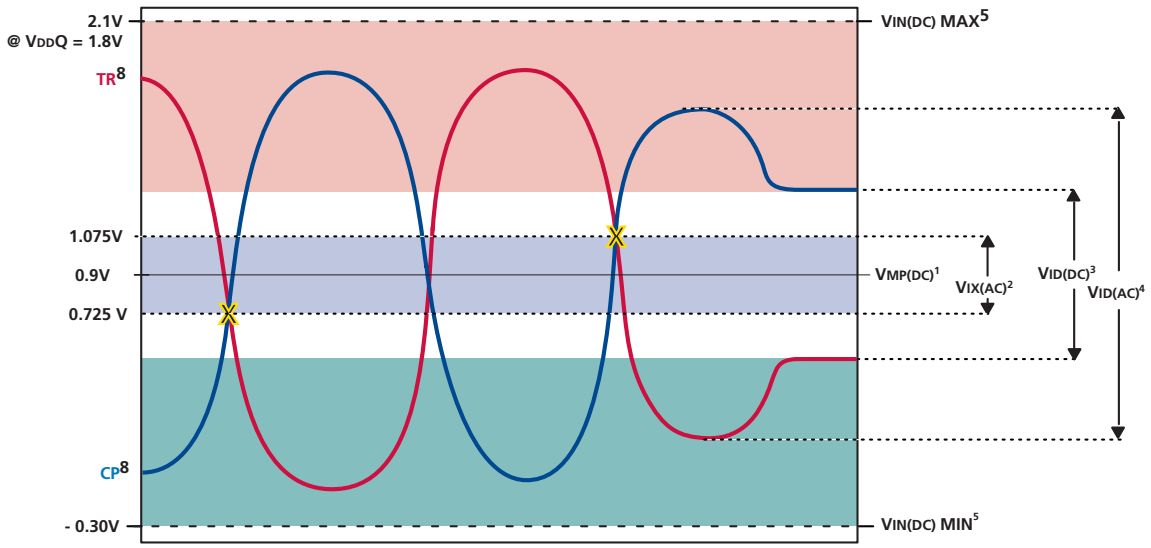
Note: Numbers in diagram reflect nomimal values.

Table 24: Differential Input Logic Levels
All voltages referenced to V_{SS}

Parameter	Symbol	Min	Max	Units	Notes
DC input signal voltage	$V_{IN(DC)}$	-300	V_{DDQ} + 300	mV	1
DC differential input voltage	$V_{ID(DC)}$	250	V_{DDQ} + 600	mV	2
AC differential input voltage	$V_{ID(AC)}$	500	V_{DDQ} + 600	mV	3
AC differential cross-point voltage	$V_{IX(AC)}$	0.50 x V_{DDQ} - 175	0.50 x V_{DDQ} + 175	mV	4
Input midpoint voltage	$V_{MP(DC)}$	850	950	mV	5

Notes:
1. $V_{IN(DC)}$ specifies the allowable DC execution of each input of differential pair such as CK, CK#, DQS, DQS#, LDQS, LDQS#, UDQS, UDQS#, and RDQS, RDQS#.
2. $V_{ID(DC)}$ specifies the input differential voltage | V_{TR} - V_{CP} | required for switching, where V_{TR} is the true input (such as CK, DQS, LDQS, UDQS) level and V_{CP} is the complementary input (such as CK#, DQS#, LDQS#, UDQS#). The minimum value is equal to $V_{IH(DC)}$ - $V_{IL(DC)}$. Differential input signal levels are shown in Figure 66.
3. $V_{ID(AC)}$ specifies the input differential voltage | V_{TR} - V_{CP} | required for switching, where V_{TR} is the true input (such as CK, DQS, LDQS, UDQS, RDQS) level and V_{CP} is the complementary input (such as CK#, DQS#, LDQS#, UDQS#, RDQS#). The minimum value is equal to $V_{IH(AC)}$ - $V_{IL(AC)}$, as shown in Table 23 on page 85.
4. The typical value of $V_{IX(AC)}$ is expected to be about 0.5 x V_{DDQ} of the transmitting device and $V_{IX(AC)}$ is expected to track variations in V_{DDQ}. $V_{IX(AC)}$ indicates the voltage at which differential input signals must cross, as shown in Figure 66.
5. $V_{MP(DC)}$ specifies the input differential common mode voltage (V_{TR} + V_{CP})/2 where V_{TR} is the true input (CK, DQS) level and V_{CP} is the complementary input (CK#, DQS#). $V_{MP(DC)}$ is expected to be approximately 0.5 x V_{DDQ}.

Figure 66: Differential Input Signal Levels



Notes:
1. This provides a minimum of 850mV to a maximum of 950mV and is expected to be V_{DDQ}/2.
2. TR and CP must cross in this region.
3. TR and CP must meet at least $V_{ID(DC)}$ MIN when static and is centered around $V_{MP(DC)}$.
4. TR and CP must have a minimum 500mV peak-to-peak swing.
5. TR and CP may not be more positive than V_{DDQ} + 0.3V or more negative than V_{SS} - 0.3V.
6. For AC operation, all DC clock requirements must also be satisfied.
7. Numbers in diagram reflect nominal values.
8. TR represents the CK, DQS, RDQS, LDQS, and UDQS signals; CP represents CK#, DQS#, RDQS#, LDQS#, and UDQS# signals.

Table 25: AC Input Test Conditions

Parameter	Symbol	Min	Max	Units	Notes
Input setup timing measurement reference level BA1–BA0, A0–A12 , CS#, RAS#, CAS#, WE#, ODT, DM, UDM, LDM, and CKE	V_{RS}	See Note 2			1, 2, 8
Input hold timing measurement reference level BA1–BA0, A0–A12, CS#, RAS#, CAS#, WE#, ODT, DM, UDM, LDM, and CKE	V_{RH}	See Note3			1, 3, 8
Input timing measurement reference level (single-ended) DQS for x4, x8; UDQS, LDQS for x16	$V_{REF(DC)}$	V_{DDQ} x 0.49	V_{DDQ} x 0.51	V	1, 4, 9
Input timing measurement reference level (differential) CK, CK# for x4, x8, x16 DQS, DQS# for x4, x8; RDQS, RDQS# for x8 UDQS, UDQS#, LDQS, LDQS# for x16	V_{RD}	$V_{IX(AC)}$		V	1, 5, 6, 9

Notes:
1. All voltages referenced to V_{SS}.
2. Input waveform setup timing ($^{t}IS_b$) is referenced from the input signal crossing at the $V_{IH(AC)}$ level for a rising signal and $V_{IL(AC)}$ for a falling signal applied to the device under test, as shown in Figure 75 on page 102.
3. Input waveform hold ($^{t}IH_b$) timing is referenced from the input signal crossing at the $V_{IL(DC)}$ level for a rising signal and $V_{IH(DC)}$ for a falling signal applied to the device under test, as shown in Figure 75 on page 102.
4. Input waveform setup timing (^{t}DS) and hold timing (^{t}DH) for single-ended data strobe is referenced from the crossing of DQS, UDQS, or LDQS through the V_{REF} level applied to the device under test, as shown in Figure 77 on page 103.
5. Input waveform setup timing (^{t}DS) and hold timing (^{t}DH) when differential data strobe is enabled is referenced from the crosspoint of DQS/DQS#, UDQS/UDQS#, or LDQS/LDQS#, as shown in Figure 76 on page 102.
6. Input waveform timing is referenced to the crossing point level (V_{IX}) of two input signals (V_{TR} and V_{CP}) applied to the device under test, where V_{TR} is the "true" input signal and V_{CP} is the complementary input signal, as shown in Figure 78 on page 103.
7. See "Input Slew Rate Derating" on page 88.
8. The slew rate for single-ended inputs is measured from DC-level to AC-level, ($V_{IL(DC)}$ to $V_{IH(AC)}$ on the rising edge and $V_{IL(AC)}$ to $V_{IH(DC)}$ on the falling edge. For signals referenced to V_{REF}, the valid intersection is where the "tangent" line intersects V_{REF}, as shown in Figures 72, 74, 76, and 78.
9. The slew rate for differentially ended inputs is measured from twice the DC-level to twice the AC-level — 2 x $V_{IL(DC)}$ to 2 x $V_{IH(AC)}$ on the rising edge and 2 x $V_{IL(AC)}$ to 2 x $V_{IH(DC)}$ on the falling edge). For example, the CK/CK# would be -250mV to +500mV for CK rising edge and would be +250mV to -500mV for CK falling edge.

Input Slew Rate Derating

For all input signals, the total ^{t}IS (setup time) and ^{t}IH (hold time) required is calculated by adding the data sheet ^{t}IS (base) and ^{t}IH (base) value to the Δ^{t}IS and Δ^{t}IH derating value respectively. Example: ^{t}IS (total setup time) = ^{t}IS (base) + Δ^{t}IS.

^{t}IS, the nominal slew rate for a rising signal, is defined as the slew rate between the last crossing of VREF(DC) and the first crossing of VIH(AC) MIN. Setup nominal slew rate (^{t}IS) for a falling signal is defined as the slew rate between the last crossing of VREF(DC) and the first crossing of VIL(AC) MAX.

If the actual signal is always earlier than the nominal slew rate line between shaded "VREF(DC) to AC region," use nominal slew rate for derating value (Figure 67 on page 90).

If the actual signal is later than the nominal slew rate line anywhere between shaded "VREF(DC) to ac region," the slew rate of a tangent line to the actual signal from the AC level to DC level is used for derating value (see Figure 68 on page 91).

^{t}IH, the nominal slew rate for a rising signal, is defined as the slew rate between the last crossing of VIL(DC) MAX and the first crossing of VREF(DC). ^{t}IH, nominal slew rate for a falling signal, is defined as the slew rate between the last crossing of VIH(DC) MIN and the first crossing of VREF(DC).

If the actual signal is always later than the nominal slew rate line between shaded "DC to VREF(DC) region," use nominal slew rate for derating value (Figure 69 on page 92).

If the actual signal is earlier than the nominal slew rate line anywhere between shaded "DC to VREF(DC)) region," the slew rate of a tangent line to the actual signal from the DC level to VREF(DC) level is used for the derating value (Figure 70 on page 93).

Although the total setup time might be negative for slow slew rates (a valid input signal will not have reached VIH(AC)/VIL(AC) at the time of the rising clock transition), a valid input signal is still required to complete the transition and reach VIH(AC)/VIL(AC).

For slew rates in between the values listed in Table 26, the derating values may obtained by linear interpolation.

Table 26: DDR2-400/533 Setup and Hold Time Derating Values

Command/ Address Slew Rate (V/ns)	CK, CK# Differential Slew Rate						Units
	2.0 V/ns		1.5 V/ns		1.0 V/ns		
	Δ^tIS	Δ^tIH	Δ^tIS	Δ^tIH	Δ^tIS	Δ^tIH	
4.0	+187	+94	+217	+124	+247	+154	ps
3.5	+179	+89	+209	+119	+239	+149	ps
3.0	+167	+83	+197	+113	+227	+143	ps
2.5	+150	+75	+180	+105	+210	+135	ps
2.0	+125	+45	+155	+75	+185	+105	ps
1.5	+83	+21	+113	+51	+143	+81	ps
1.0	0	0	+30	+30	+60	+60	ps
0.9	-11	-14	+19	+16	+49	+46	ps
0.8	-25	-31	+5	-1	+35	+29	ps
0.7	-43	-54	-13	-24	+17	+6	ps
0.6	-67	-83	-37	-53	-7	-23	ps
0.5	-110	-125	-80	-95	-50	-65	ps
0.4	-175	-188	-145	-158	-115	-128	ps
0.3	-285	-292	-255	-262	-225	-232	ps
0.25	-350	-375	-320	-345	-290	-315	ps
0.2	-525	-500	-495	-470	-465	-440	ps
0.15	-800	-708	-770	-678	-740	-648	ps
0.1	-1450	-1125	-1420	-1095	-1390	-1065	ps

Table 27: DDR2-667 Setup and Hold Time Derating Values

Command/ Address Slew Rate (V/ns)	CK, CK# Differential Slew Rate						Units
	2.0 V/ns		1.5 V/ns		1.0 V/ns		
	Δ^tIS	Δ^tIH	Δ^tIS	Δ^tIH	Δ^tIS	Δ^tIH	
4.0	+150	+94	+180	+124	+210	+154	ps
3.5	+143	+89	+173	+119	+203	+149	ps
3.0	+133	+83	+163	+113	+193	+143	ps
2.5	+120	+75	+150	+105	+180	+135	ps
2.0	+100	+45	+160	+75	+160	+105	ps
1.5	+67	+21	+97	+51	+127	+81	ps
1.0	0	0	+30	+30	+60	+60	ps
0.9	-5	-14	+25	+16	+55	+46	ps
0.8	-13	-31	+17	-1	+47	+29	ps
0.7	-22	-54	+8	-24	+38	+6	ps
0.6	-34	-83	-4	-53	+36	-23	ps
0.5	-60	-125	-30	-95	0	-65	ps
0.4	-100	-188	-70	-158	-40	-128	ps
0.3	-168	-292	-138	-262	-108	-232	ps
0.25	-200	-375	-170	-345	-140	-315	ps
0.2	-325	-500	-295	-470	-265	-440	ps
0.15	-517	-708	-487	-678	-457	-648	ps
0.1	-1,000	-1,125	-970	-1,095	-940	-1,065	ps

Figure 67: Nominal Slew Rate for ^{t}IS

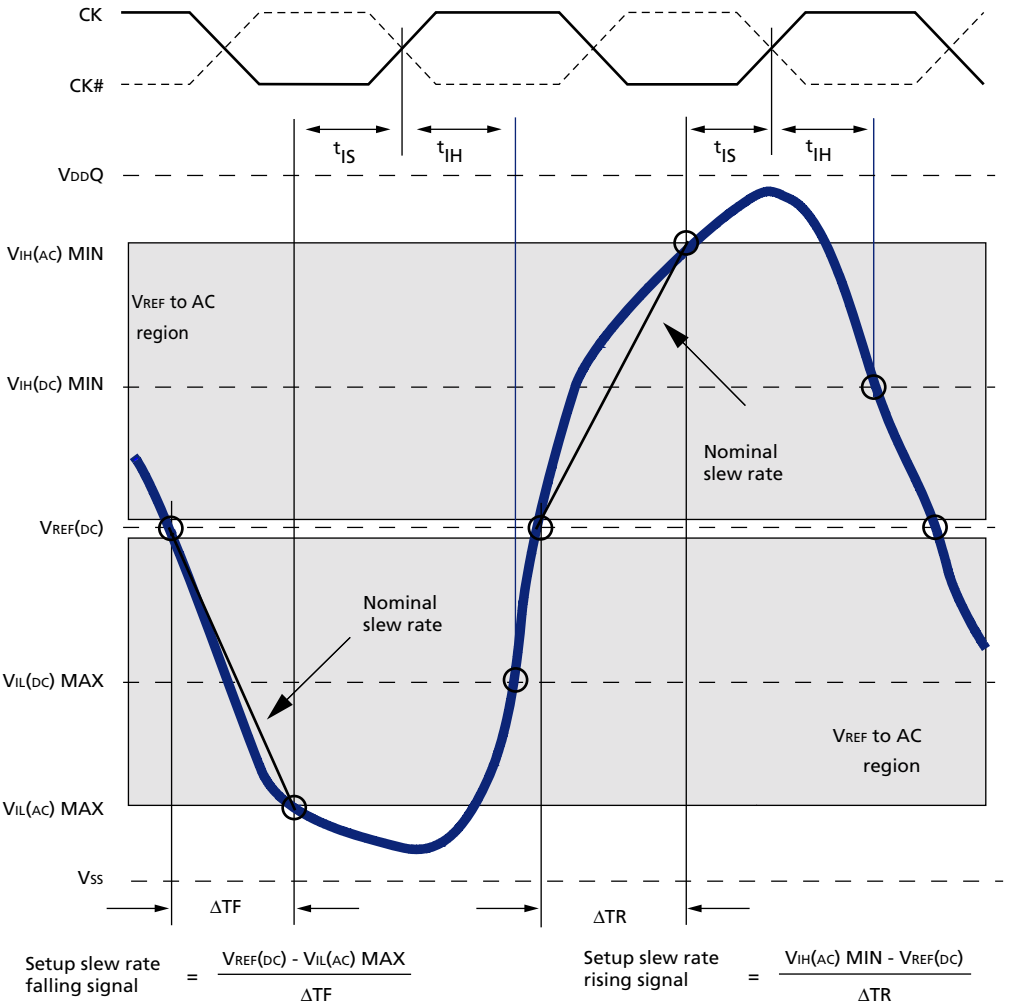


Figure 68: Tangent Line for ^{t}IS

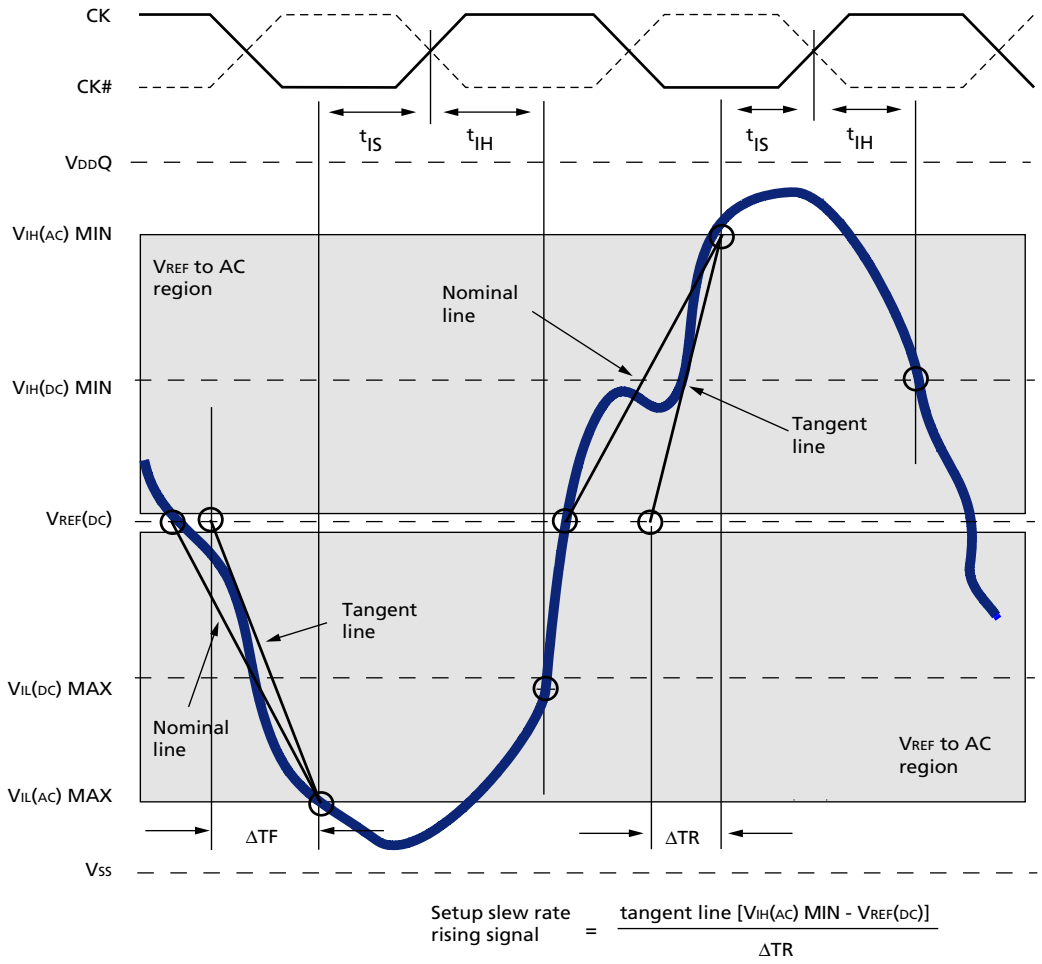


Figure 69: Nominal Slew Rate for ^{t}IH

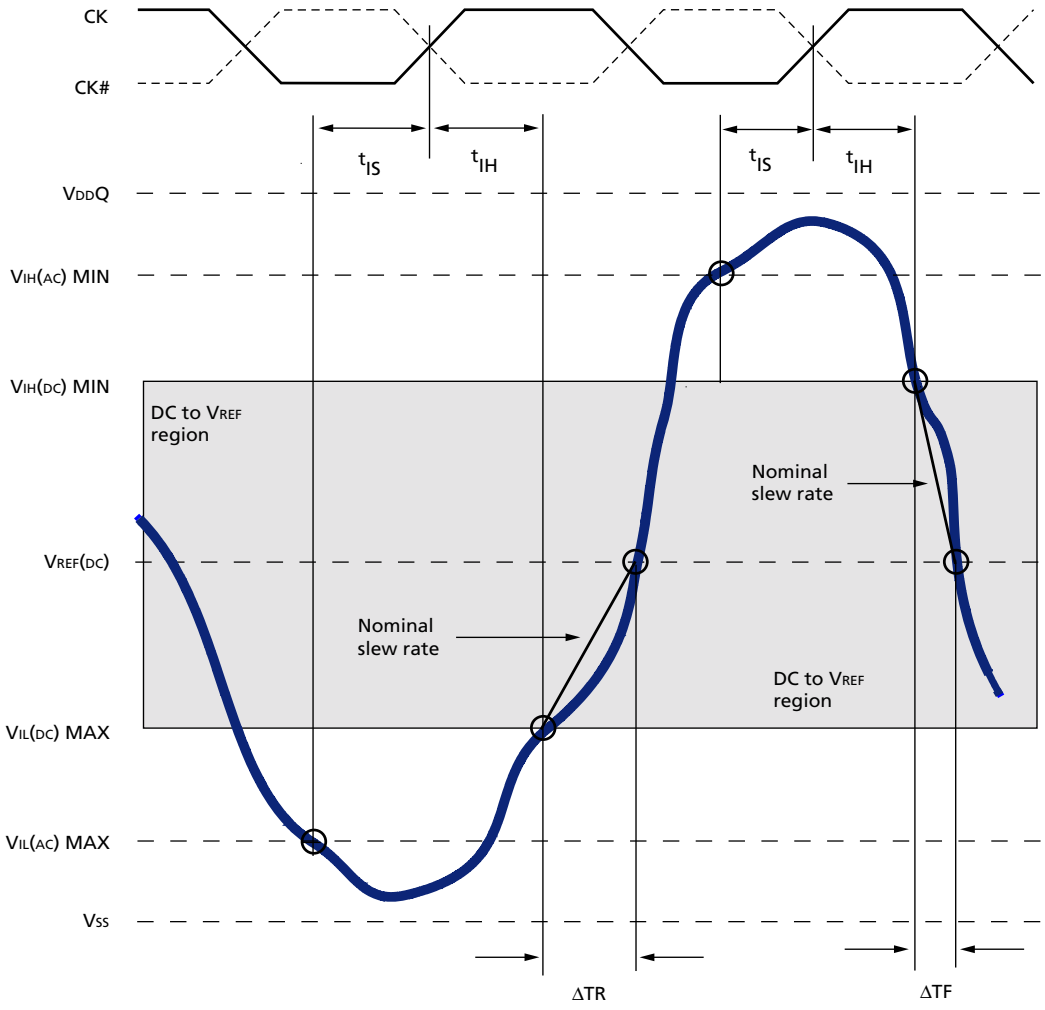
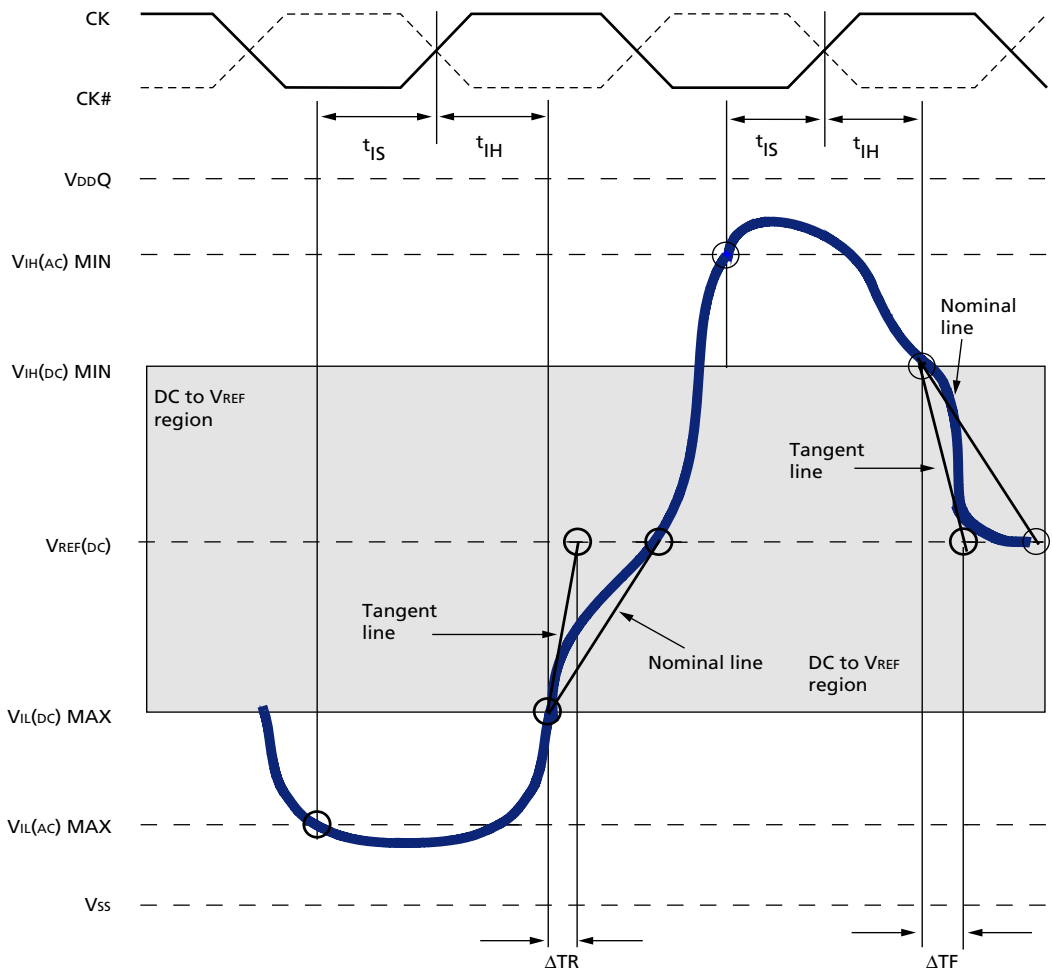


Figure 70: Tangent Line for ^{t}IH



$$\text{Hold slew rate rising signal} = \frac{\text{tangent line } [V_{REF(DC)} - V_{IL(DC)}\ \text{MAX}]}{\Delta TR}$$

$$\text{Hold slew rate falling signal} = \frac{\text{tangent line } [V_{IH(DC)}\ \text{MIN} - V_{REF(DC)}]}{\Delta TF}$$

Table 28: DDR2-400/533 ^{t}DS, ^{t}DH Derating Values
Notes: 1–7; all units in ps

DQ Slew Rate (V/ns)	DQS, DQS# Differential Slew Rate																	
	4.0 V/ns		3.0 V/ns		2.0 V/ns		1.8 V/ns		1.6 V/ns		1.4 V/ns		1.2 V/ns		1.0 V/ns		0.8 V/ns	
	Δ^{t}DS	Δ^{t}DH	Δ^{t}DS	Δ^{t}DH	Δ^{t}DS	Δ^{t}DH	Δ^{t}DS	Δ^{t}DH	Δ^{t}DS	Δ^{t}DH	Δ^{t}DS	Δ^{t}DH	Δ^{t}DS	Δ^{t}DH	Δ^{t}DS	Δ^{t}DH	Δ^{t}DS	Δ^{t}DH
2.0	125	45	125	45	125	45	–	–	–	–	–	–	–	–	–	–	–	–
1.5	83	21	83	21	83	21	95	33	–	–	–	–	–	–	–	–	–	–
1.0	0	0	0	0	0	0	12	12	24	24	–	–	–	–	–	–	–	–
0.9	–	–	-11	-14	-11	-14	1	-2	13	10	25	22	–	–	–	–	–	–
0.8	–	–	–	–	-25	-31	-13	-19	-1	-7	11	5	23	17	–	–	–	–
0.7	–	–	–	–	–	–	-31	-42	-19	-30	-7	-18	5	-6	17	6	–	–
0.6	–	–	–	–	–	–	–	–	-43	-59	-31	-47	-19	-35	-7	-23	5	-11
0.5	–	–	–	–	–	–	–	–	–	–	-74	-89	-62	-77	-50	-65	-38	-53
0.4	–	–	–	–	–	–	–	–	–	–	–	–	-127	-140	-115	-128	-103	-116

Notes:
1. For all input signals, the total ^{t}DS and ^{t}DH required is calculated by adding the data sheet value to the derating value listed in Table 28.
2. ^{t}DS nominal slew rate for a rising signal is defined as the slew rate between the last crossing of V_{REF}(DC) and the first crossing of V_{IH}(AC) MIN. ^{t}DS nominal slew rate for a falling signal is defined as the slew rate between the last crossing of V_{REF}(DC) and the first crossing of V_{IL}(AC) MAX. If the actual signal is always earlier than the nominal slew rate line between shaded "V_{REF}(DC) to AC region," use nominal slew rate for derating value (see Figure 71). If the actual signal is later than the nominal slew rate line anywhere between shaded "V_{REF}(DC) to AC region," the slew rate of a tangent line to the actual signal from the AC level to DC level is used for derating value (see Figure 72).
3. ^{t}DH nominal slew rate for a rising signal is defined as the slew rate between the last crossing of V_{IL}(DC) MAX and the first crossing of V_{REF}(DC). ^{t}DH nominal slew rate for a falling signal is defined as the slew rate between the last crossing of V_{IH}(DC) MIN and the first crossing of V_{REF} (DC). If the actual signal is always later than the nominal slew rate line between shaded "DC level to V_{REF}(DC) region," use nominal slew rate for derating value (see Figure 73). If the actual signal is earlier than the nominal slew rate line anywhere between shaded "DC to V_{REF}(DC) region," the slew rate of a tangent line to the actual signal from the DC level to V_{REF}(DC) level is used for derating value (see Figure 74).
4. Although the total setup time might be negative for slow slew rates (a valid input signal will not have reached V_{IH}(AC)/V_{IL}(AC) at the time of the rising clock transition), a valid input signal is still required to complete the transition and reach V_{IH}(AC)/V_{IL}(AC).
5. For slew rates between the values listed in this table, the derating values may obtained by linear interpolation.
6. These values are typically not subject to production test. They are verified by design and characterization.
7. Single-ended DQS requires special derating. The values in Table 30 are the DQS single-ended slew rate derating with DQS referenced at V_{REF} and DQ referenced at the logic levels $^{t}DS_{b}$ and $^{t}DH_{b}$). Tables 32 and 33 provide the V_{REF}-based, fully derated values for the DQ ($^{t}DS_{a}$ and $^{t}DH_{a}$) for DDR2-400 and DDR2-533, respectively.

Table 29: DDR2-667 ^{t}DS, ^{t}DH Derating Values
Notes: 1–7; all units in ps

DQ Slew Rate (V/ns)	DQS, DQS# Differential Slew Rate																	
	2.8 V/ns		2.4 V/ns		2.0 V/ns		1.8 V/ns		1.6 V/ns		1.4 V/ns		1.2 V/ns		1.0 V/ns		0.8 V/ns	
	Δ^{t}DS	Δ^{t}DH	Δ^{t}DS	Δ^{t}DH	Δ^{t}DS	Δ^{t}DH	Δ^{t}DS	Δ^{t}DH	Δ^{t}DS	Δ^{t}DH	Δ^{t}DS	Δ^{t}DH	Δ^{t}DS	Δ^{t}DH	Δ^{t}DS	Δ^{t}DH	Δ^{t}DS	Δ^{t}DH
2.0	100	63	100	63	100	63	112	75	124	87	136	99	148	111	160	123	172	135
1.5	67	42	67	42	67	42	79	54	91	66	103	78	115	90	127	102	139	114
1.0	0	0	0	0	0	0	12	12	24	24	36	36	48	48	60	60	72	72
0.9	-5	-14	-5	-14	-5	-14	7	-2	19	10	31	22	43	34	55	46	67	58
0.8	-13	-31	-13	-31	-13	-31	-1	-19	11	-7	23	5	35	17	47	29	59	41
0.7	-22	-54	-22	-54	-22	-54	-10	-42	2	-30	14	-18	26	-6	38	6	50	18
0.6	-34	-83	-34	-83	-34	-83	-22	-71	-10	-59	2	-47	14	-35	26	-23	38	-11
0.5	-60	-125	-60	-125	-60	-125	-48	-113	-36	-101	-24	-89	-12	-77	0	-65	12	-53
0.4	-100	-188	-100	-188	-100	-188	-88	-176	-76	-164	-64	-152	-52	-140	-40	-128	-28	-116

Notes:
1. For all input signals the total ^{t}DS and ^{t}DH required is calculated by adding the data sheet value to the derating value listed in Table 28.
2. ^{t}DS nominal slew rate for a rising signal is defined as the slew rate between the last crossing of VREF(DC) and the first crossing of VIH(AC) MIN. ^{t}DS nominal slew rate for a falling signal is defined as the slew rate between the last crossing of VREF(DC) and the first crossing of VIL(AC) MAX. If the actual signal is always earlier than the nominal slew rate line between shaded "VREF(DC) to AC region," use nominal slew rate for derating value (see Figure 71). If the actual signal is later than the nominal slew rate line anywhere between shaded "VREF(DC) to AC region," the slew rate of a tangent line to the actual signal from the AC level to DC level is used for derating value (see Figure 72).
3. ^{t}DH nominal slew rate for a rising signal is defined as the slew rate between the last crossing of VIL(DC) MAX and the first crossing of VREF(DC). ^{t}DH nominal slew rate for a falling signal is defined as the slew rate between the last crossing of VIH(DC) MIN and the first crossing of VREF (DC). If the actual signal is always later than the nominal slew rate line between shaded "DC level to VREF(DC) region," use nominal slew rate for derating value (see Figure 73). If the actual signal is earlier than the nominal slew rate line anywhere between shaded "DC to VREF(DC) region," the slew rate of a tangent line to the actual signal from the DC level to VREF(DC) level is used for derating value (see Figure 74).
4. Although the total setup time might be negative for slow slew rates (a valid input signal will not have reached VIH(AC)/VIL(AC) at the time of the rising clock transition), a valid input signal is still required to complete the transition and reach VIH(AC)/VIL(AC).
5. For slew rates between the values listed in this table, the derating values may obtained by linear interpolation.
6. These values are typically not subject to production test. They are verified by design and characterization.
7. Single-ended DQS requires special derating. The values in Table 30 are the DQS single-ended slew rate derating with DQS referenced at VREF and DQ referenced at the logic levels $^{t}DS_{b}$ and $^{t}DH_{b}$). Table 31 provides the VREF-based fully derated values for the DQ ($^{t}DS_{a}$ and $^{t}DH_{a}$) for DDR2-667. Table 32 provides the VREF-based fully derated values for the DQ ($^{t}DS_{a}$ and $^{t}DH_{a}$) for DDR2-533. Table 33 provides the VREF-based fully derated values for the DQ ($^{t}DS_{a}$ and $^{t}DH_{a}$) for DDR2-400.

Table 30: Single-Ended DQS Slew Rate Derating Values
Reference points indicated in bold

DQ (V/ns)	DQS Single-Ended Slew Rate Derated (at VREF)																	
	2.0 V/ns		1.8 V/ns		1.6 V/ns		1.4 V/ns		1.2 V/ns		1.0 V/ns		0.8 V/ns		0.6 V/ns		0.4V/ns	
	tDS	tDH	tDS	tDH	tDS	tDH	tDS	tDH	tDS	tDH	tDS	tDH	tDS	tDH	tDS	tDH	tDS	tDH
2	130	53	130	53	130	53	130	53	130	53	145	48	155	45	165	41	175	38
1.5	97	32	97	32	97	32	97	32	97	32	112	27	122	24	132	20	142	17
1	30	-10	30	-10	30	-10	30	-10	30	-10	**45**	**-15**	55	-18	65	-22	75	-25
0.9	25	-24	25	-24	25	-24	25	-24	25	-24	40	-29	50	-32	60	-36	70	-39
0.8	17	-41	17	-41	17	-41	17	-41	17	-41	32	-46	42	-49	52	-53	61	-56
0.7	5	-64	5	-64	5	-64	5	-64	5	-64	20	-69	30	-72	40	-75	50	-79
0.6	-7	-93	-7	-93	-7	-93	-7	-93	-7	-93	8	-98	18	-102	28	-105	38	-108
0.5	-28	-135	-28	-135	-28	-135	-28	-135	-28	-135	-13	-140	-3	-143	7	-147	17	-150
0.4	-78	-198	-78	-198	-78	-198	-78	-198	-78	-198	-63	-203	-53	-206	-43	-210	-33	-213

Notes: 1. Derating values, to be used with base tDS- and tDH-specified values.

Table 31: Single-Ended DQS Slew Rate Derated (DQS, DQ at VREF) at DDR2-667
Reference points indicated in bold

DQ (V/ns)	DQS Single-Ended Slew Rate Derated (at VREF)																	
	2.0 V/ns		1.8 V/ns		1.6 V/ns		1.4 V/ns		1.2 V/ns		1.0 V/ns		0.8 V/ns		0.6 V/ns		0.4V/ns	
	tDS	tDH	tDS	tDH	tDS	tDH	tDS	tDH	tDS	tDH	tDS	tDH	tDS	tDH	tDS	tDH	tDS	tDH
2	330	291	330	291	330	291	330	291	330	291	345	286	355	282	365	29	375	276
1.5	330	290	330	290	330	290	330	290	330	290	345	285	355	282	365	279	375	275
1	330	290	330	290	330	290	330	290	330	290	**345**	**285**	355	282	365	278	375	275
0.9	347	290	347	290	347	290	347	290	347	290	362	285	372	282	382	278	392	275
0.8	367	290	367	290	367	290	367	290	367	290	382	285	392	282	402	278	412	275
0.7	391	290	391	290	391	290	391	290	391	290	406	285	416	281	426	278	436	275
0.6	426	290	426	290	426	290	426	290	426	290	441	285	451	282	461	278	471	275
0.5	472	290	472	290	472	290	472	290	472	290	487	285	497	282	507	278	517	275
0.4	522	289	522	289	522	289	522	289	522	289	537	284	547	281	557	278	567	274

Notes: 1. Derating values, to be used with base tDS- and tDH-specified values.

Table 32: Single-Ended DQS Slew Rate Derated (DQS, DQ at VREF) at DDR2-533
Reference points indicated in bold

DQ (V/ns)	DQS Single-Ended Slew Rate Derated (at VREF)																	
	2.0 V/ns		1.8 V/ns		1.6 V/ns		1.4 V/ns		1.2 V/ns		1.0 V/ns		0.8 V/ns		0.6 V/ns		0.4V/ns	
	tDS	tDH	tDS	tDH	tDS	tDH	tDS	tDH	tDS	tDH	tDS	tDH	tDS	tDH	tDS	tDH	tDS	tDH
2	355	341	355	341	355	341	355	341	355	341	370	336	380	332	390	329	400	326
1.5	364	340	364	340	364	340	364	340	364	340	379	335	389	332	399	329	409	325
1	380	340	380	340	380	340	380	340	380	340	**395**	**335**	405	332	415	328	425	325
0.9	402	340	402	340	402	340	402	340	402	340	417	335	427	332	437	328	447	325
0.8	429	340	429	340	429	340	429	340	429	340	444	335	454	332	464	328	474	325
0.7	463	340	463	340	463	340	463	340	463	340	478	335	488	331	498	328	508	325
0.6	510	340	510	340	510	340	510	340	510	340	525	335	535	332	545	328	555	325
0.5	572	340	572	340	572	340	572	340	572	340	587	335	597	332	607	328	617	325
0.4	647	339	647	339	647	339	647	339	647	339	662	334	672	331	682	328	692	324

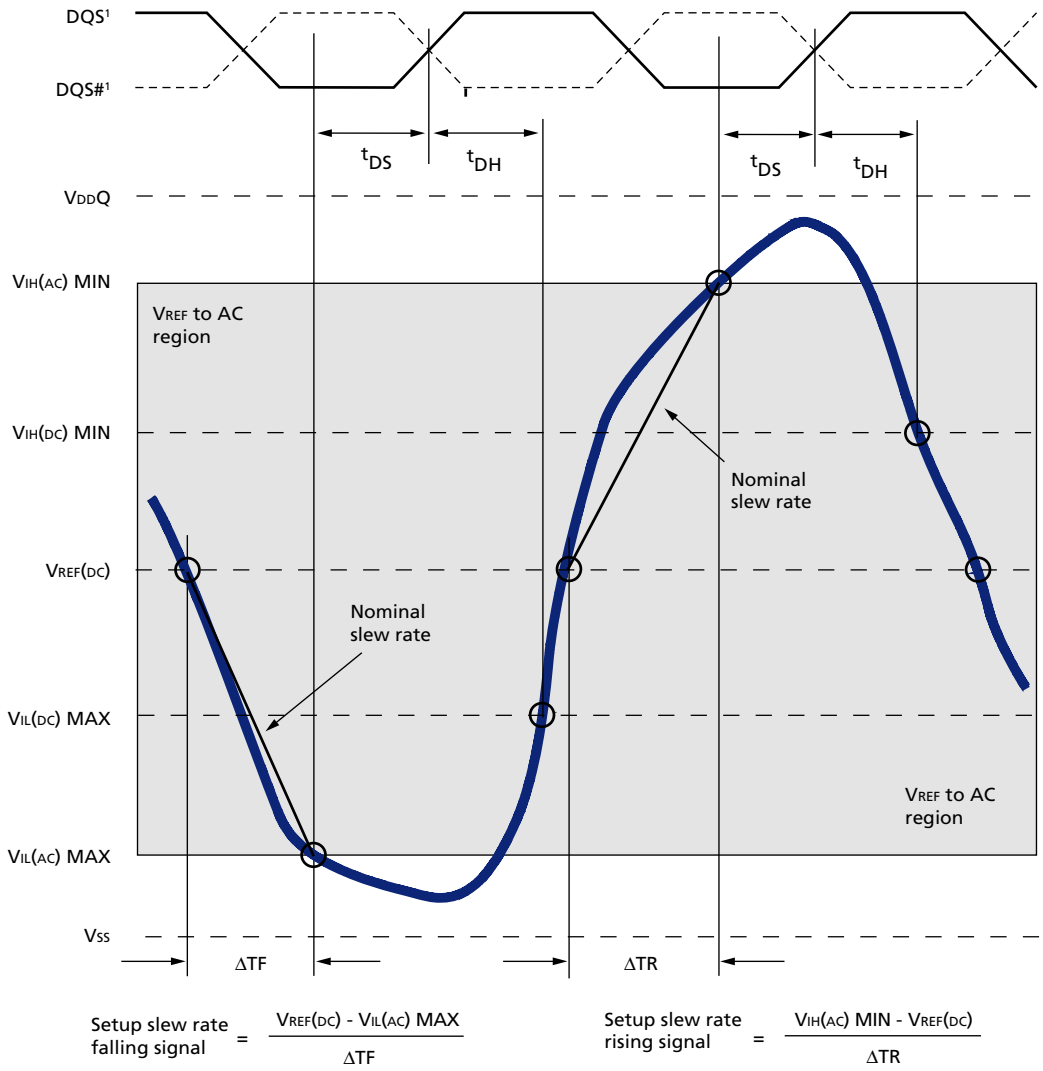
Notes: 1. Derating values, to be used with base tDS- and tDH-specified values.

Table 33: Single-Ended DQS Slew Rate Derated (DQS, DQ at VREF) at DDR2-400
Reference points indicated in bold

DQ (V/ns)	DQS Single-Ended Slew Rate Derated (at VREF)																	
	2.0 V/ns		1.8 V/ns		1.6 V/ns		1.4 V/ns		1.2 V/ns		1.0 V/ns		0.8 V/ns		0.6 V/ns		0.4V/ns	
	tDS	tDH	tDS	tDH	tDS	tDH	tDS	tDH	tDS	tDH	tDS	tDH	tDS	tDH	tDS	tDH	tDS	tDH
2	405	391	405	391	405	391	405	391	405	391	420	386	430	382	440	379	450	376
1.5	414	390	414	390	414	390	414	390	414	390	429	385	439	382	449	379	459	375
1	430	390	430	390	430	390	430	390	430	390	**445**	**385**	455	382	465	378	475	375
0.9	452	390	452	390	452	390	452	390	452	390	467	385	477	382	487	378	497	375
0.8	479	390	479	390	479	390	479	390	479	390	494	385	504	382	514	378	524	375
0.7	513	390	513	390	513	390	513	390	513	390	528	385	538	381	548	378	558	375
0.6	560	390	560	390	560	390	560	390	560	390	575	385	585	382	595	378	605	375
0.5	622	390	622	390	622	390	622	390	622	390	637	385	647	382	657	378	667	375
0.4	697	389	697	389	697	389	697	389	697	389	712	384	722	381	732	378	742	374

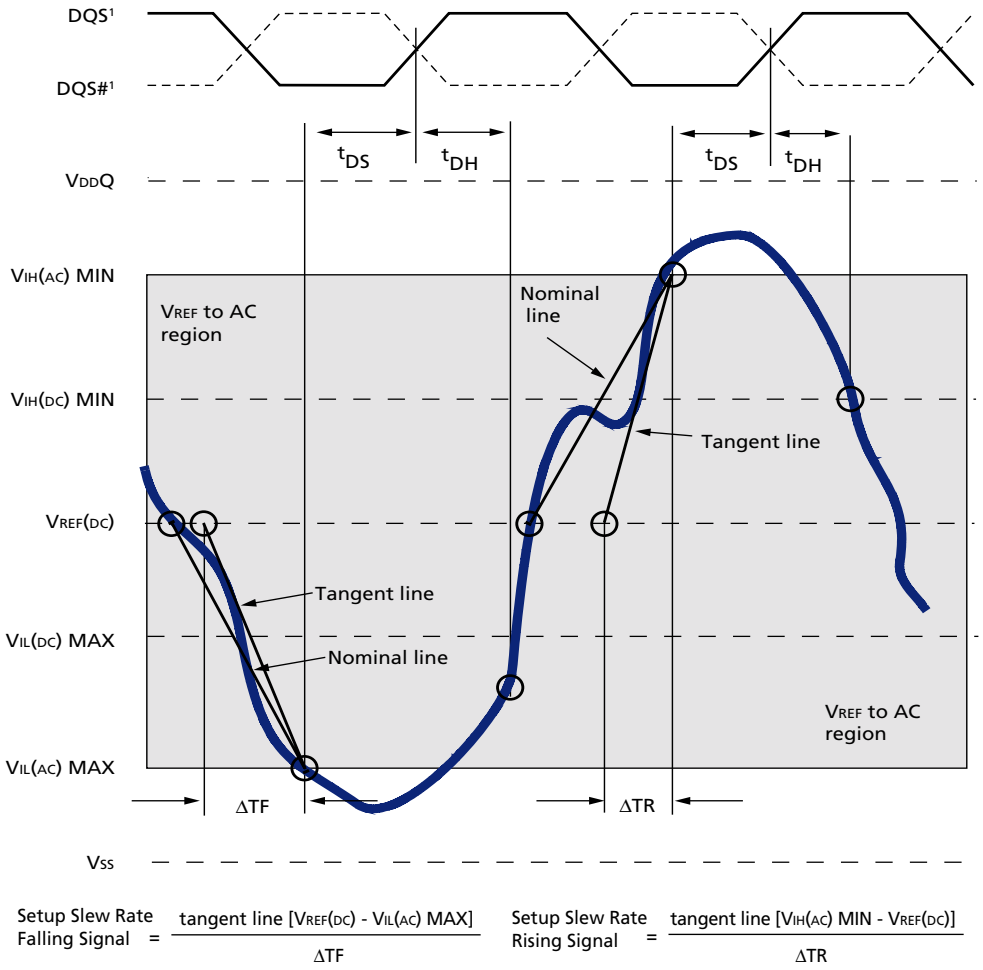
Notes: 1. Derating values, to be used with base tDS- and tDH-specified values.

Figure 71: Nominal Slew Rate for ^{t}DS



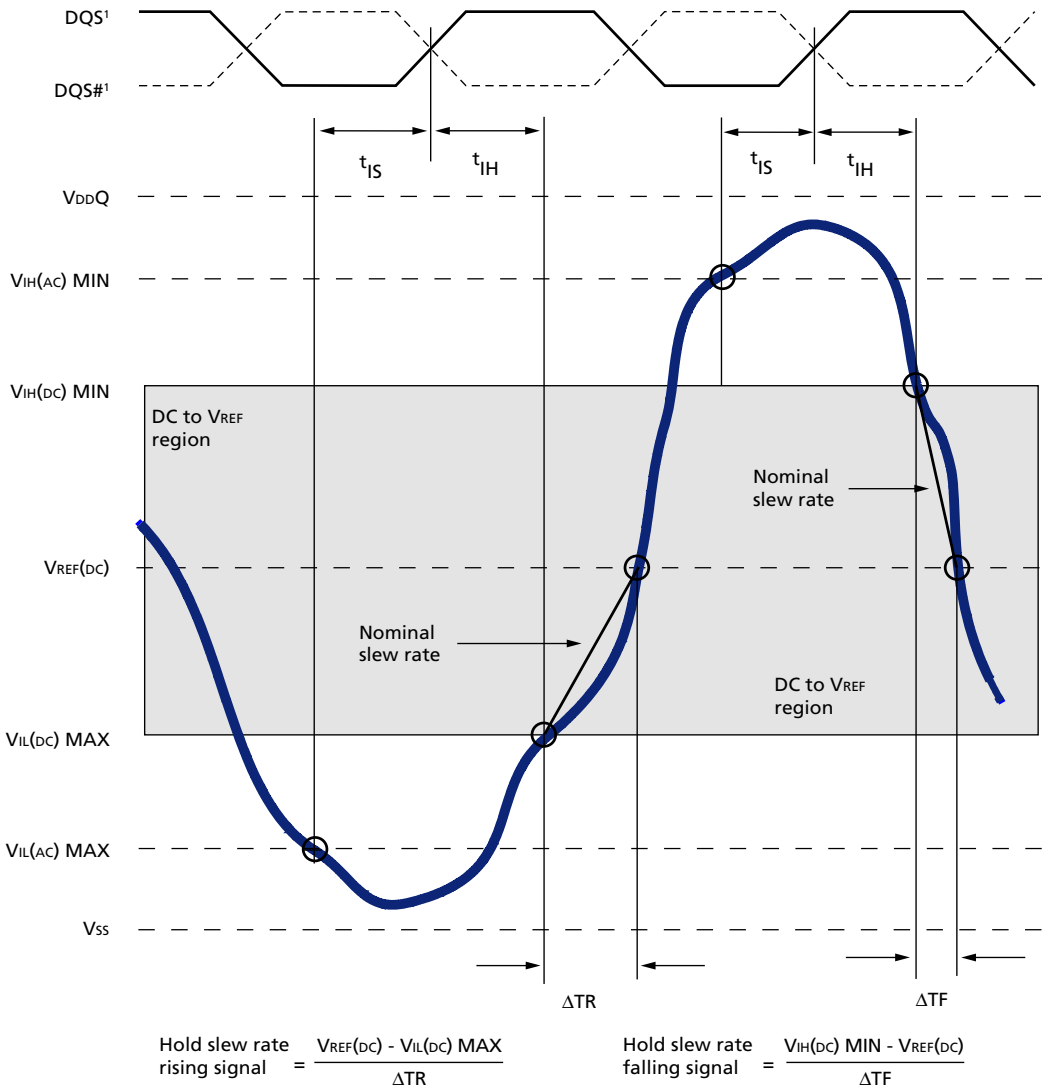
Notes: 1. DQS, DQS# signals must be monotonic between $V_{IL(DC)}$ MAX and $V_{IH(DC)}$ MIN.

Figure 72: Tangent Line for ^{t}DS



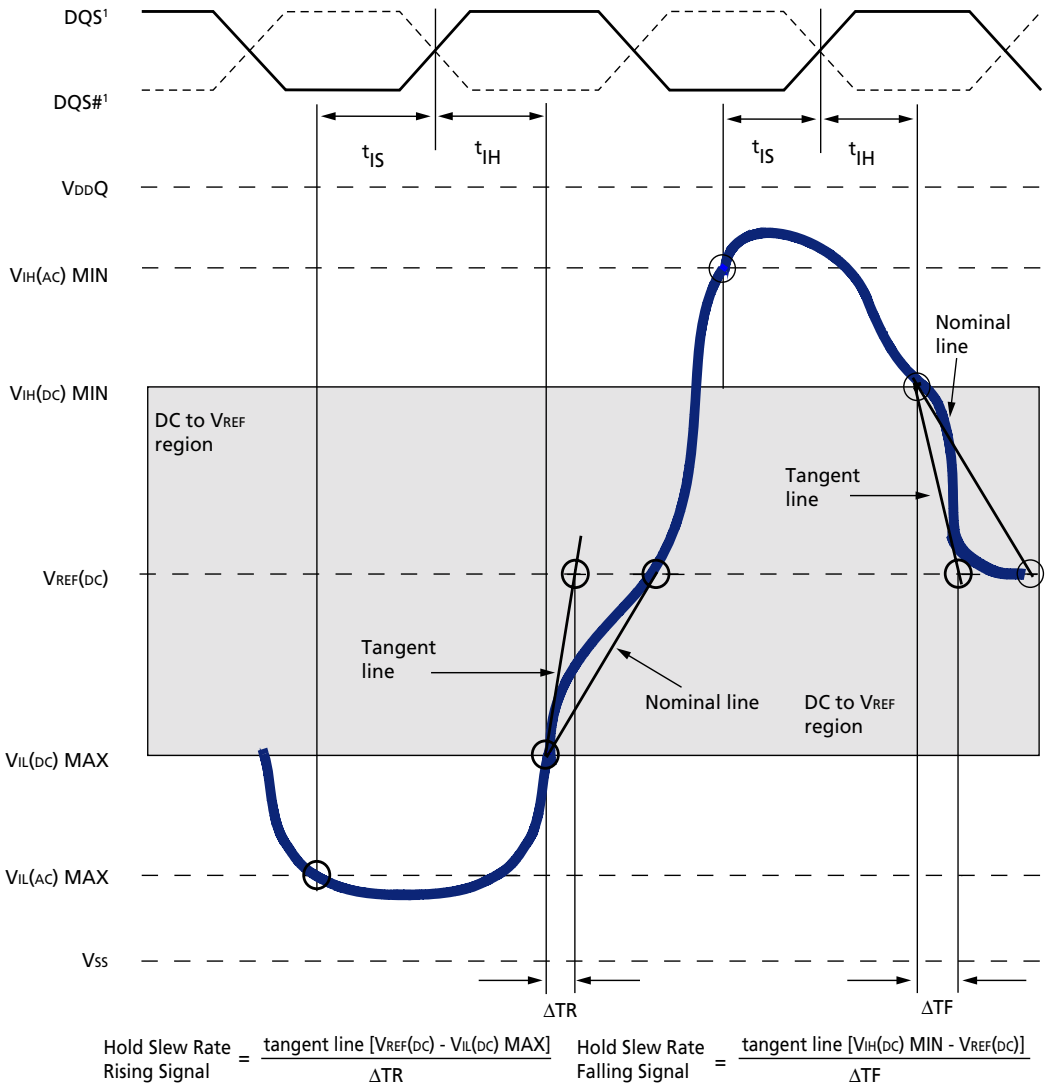
Notes: 1. DQS, DQS# signals must be monotonic between V_{IL}(DC) MAX and V_{IH}(DC) MIN.

Figure 73: Nominal Slew Rate for ^{t}DH



Notes: 1. DQS, DQS# signals must be monotonic between $V_{IL(DC)}$ MAX and $V_{IH(DC)}$ MIN.

Figure 74: Tangent Line for ^{t}DH



Notes: 1. DQS, DQS# signals must be monotonic between $V_{IL(DC)}$ MAX and $V_{IH(DC)}$ MIN.

Figure 75: AC Input Test Signal Waveform Command/Address Balls

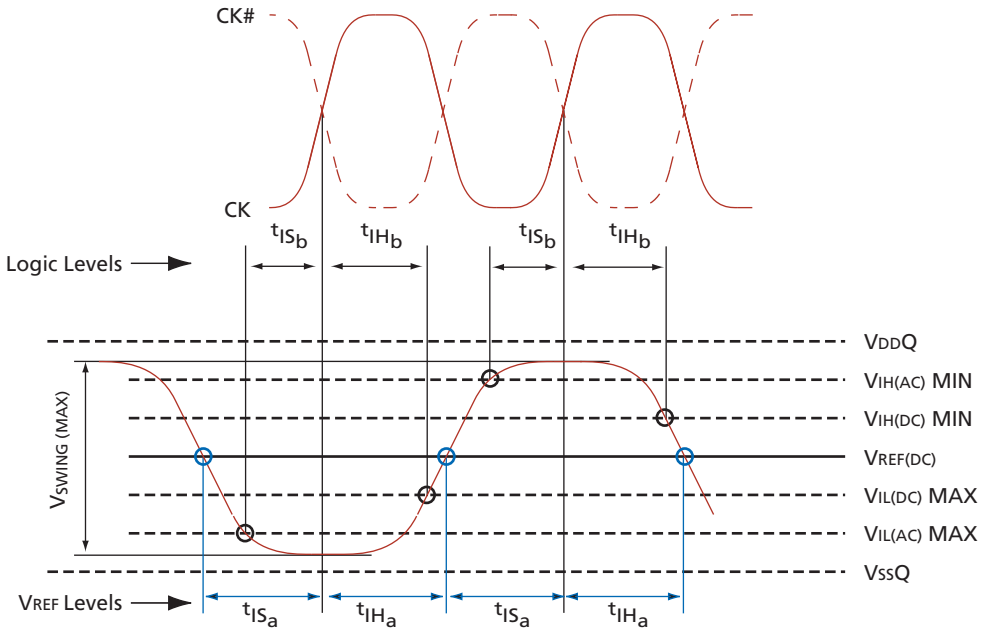


Figure 76: AC Input Test Signal Waveform for Data with DQS, DQS# (Differential)

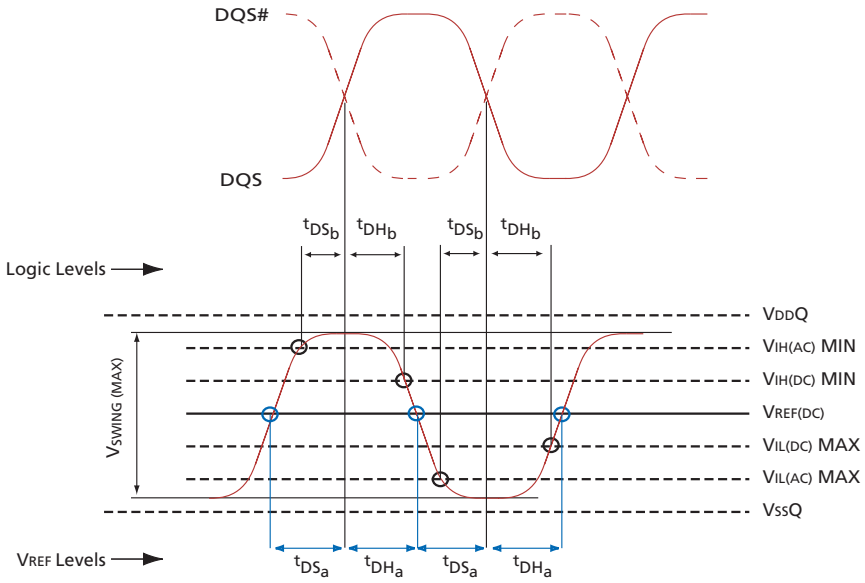


Figure 77: AC Input Test Signal Waveform for Data with DQS (Single-Ended)

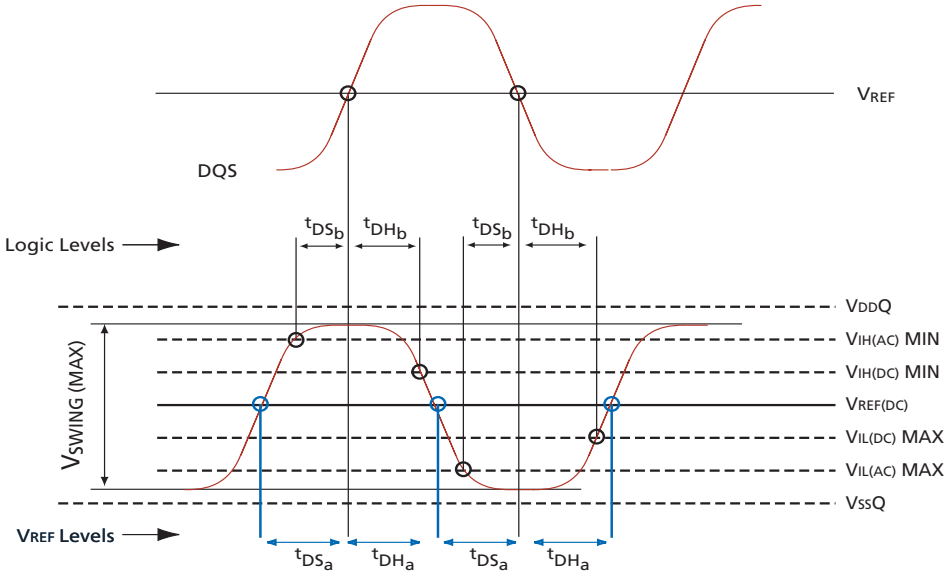
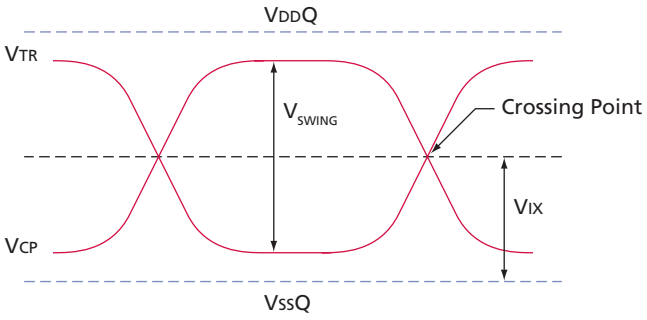


Figure 78: AC Input Test Signal Waveform (Differential)



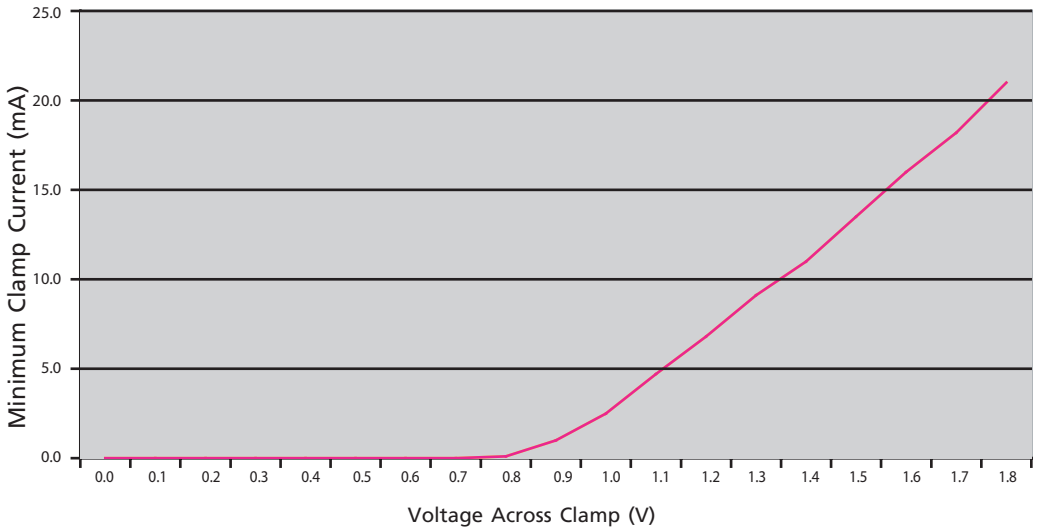
Power and Ground Clamp Characteristics

Power and ground clamps are provided on the following input-only balls: BA1–BA0, A0–A12, CS#, RAS#, CAS#, WE#, ODT, and CKE.

Table 34: Input Clamp Characteristics

Voltage Across Clamp (V)	Minimum Power Clamp Current (mA)	Minimum Ground Clamp Current (mA)
0.0	0.0	0.0
0.1	0.0	0.0
0.2	0.0	0.0
0.3	0.0	0.0
0.4	0.0	0.0
0.5	0.0	0.0
0.6	0.0	0.0
0.7	0.0	0.0
0.8	0.1	0.1
0.9	1.0	1.0
1.0	2.5	2.5
1.1	4.7	4.7
1.2	6.8	6.8
1.3	9.1	9.1
1.4	11.0	11.0
1.5	13.5	13.5
1.6	16.0	16.0
1.7	18.2	18.2
1.8	21.0	21.0

Figure 79: Input Clamp Characteristics



AC Overshoot/Undershoot Specification

Some revisions will support the 0.9V maximum average amplitude instead of the 0.5V maximum average amplitude shown in Table 35 and Table 36.

Table 35: Address and Control Balls

Applies to BA1–BA0, A0–A12, CS#, RAS#, CAS#, WE#, CKE, ODT

Parameter	Specification			
	-5E	-37E	-3/-3E	-25E
Maximum peak amplitude allowed for overshoot area (see Figure 80)	0.50V	0.50V	0.50V	0.50V
Maximum peak amplitude allowed for undershoot area (see Figure 81)	0.50V	0.50V	0.50V	0.50V
Maximum overshoot area above V_{DD} (see Figure 80)	1.33 Vns	1.00 Vns	0.80 Vns	0.66 Vns
Maximum undershoot area below V_{SS} (see Figure 81)	1.33 Vns	1.00 Vns	0.80 Vns	0.66 Vns

Table 36: Clock, Data, Strobe, and Mask Balls

Applies to DQ, DQS, DQS#, RDQS, RDQS#, UDQS, UDQS#, LDQS, LDQS#, DM, UDM, LDM

Parameter	Specification			
	-5E	-37E	-3/-3E	-25E
Maximum peak amplitude allowed for overshoot area (see Figure 80)	0.50V	0.50V	0.50V	0.50V
Maximum peak amplitude allowed for undershoot area (see Figure 80)	0.50V	0.50V	0.50V	0.50V
Maximum overshoot area above V_{DDQ} (see Figure 80)	0.38 Vns	0.28 Vns	0.23 Vns	0.19 Vns
Maximum undershoot area below V_{SSQ} (see Figure 81)	0.38 Vns	0.28 Vns	0.23 Vns	0.19 Vns

Figure 80: Overshoot

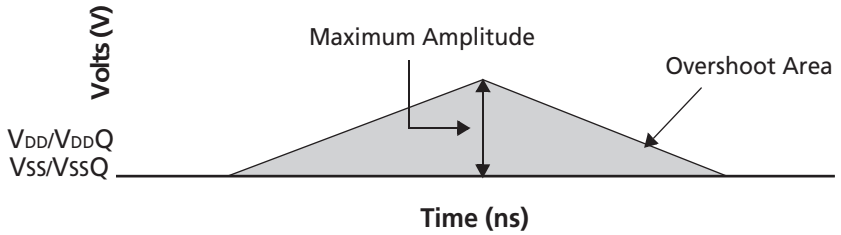
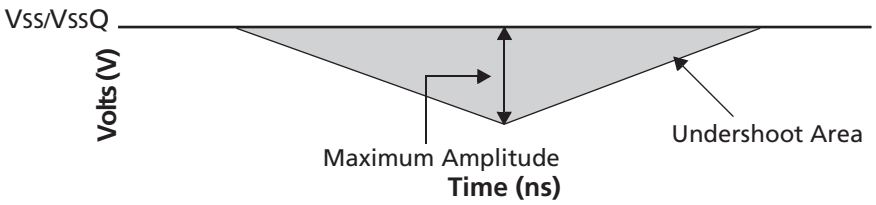


Figure 81: Undershoot



Output Electrical Characteristics and Operating Conditions

Table 37: Differential AC Output Parameters

Parameter	Symbol	Min	Max	Units	Notes
AC Differential Cross-Point Voltage	$V_{OX}(AC)$	0.50 x $V_{DD}Q$ - 125	0.50 x $V_{DD}Q$ + 125	mV	1
AC Differential Voltage Swing	V_{SWING}	1.0		mV	

Notes: 1. The typical value of $V_{OX}(AC)$ is expected to be about 0.5 x $V_{DD}Q$ of the transmitting device and $V_{OX}(AC)$ is expected to track variations in $V_{DD}Q$. $V_{OX}(AC)$ indicates the voltage at which differential output signals must cross.

Figure 82: Differential Output Signal Levels

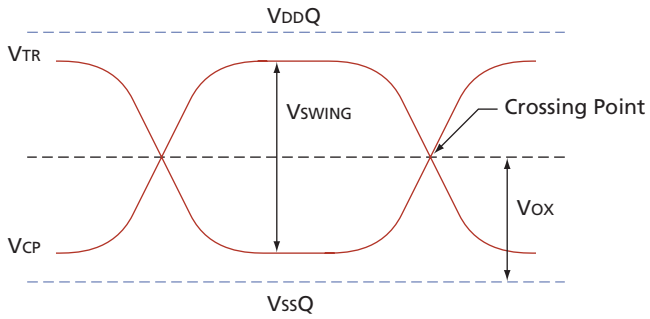


Table 38: Output DC Current Drive

Parameter	Symbol	Value	Units	Notes
Output minimum source DC current	I_{OH}	-13.4	mA	1, 3, 4
Output minimum sink DC current	I_{OL}	13.4	mA	2, 3, 4

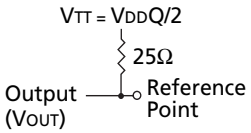
Notes:
1. For I_{OH}(DC); $V_{DD}Q$ = 1.7V, V_{OUT} = 1,420mV. (V_{OUT} - $V_{DD}Q$)/I_{OH} must be less than 21Ω for values of V_{OUT} between $V_{DD}Q$ and $V_{DD}Q$ - 280mV.
2. For I_{OL}(DC); $V_{DD}Q$ = 1.7V, V_{OUT} = 280mV. V_{OUT}/I_{OL} must be less than 21Ω for values of V_{OUT} between 0V and 280mV.
3. The DC value of V_{REF} applied to the receiving device is set to V_{TT}.
4. The values of I_{OH}(DC) and I_{OL}(DC) are based on the conditions given in Notes 1 and 2. They are used to test device drive current capability to ensure V_{IHV}(MIN) plus a noise margin and V_{IL} (MAX) minus a noise margin are delivered to an SSTL_18 receiver. The actual current values are derived by shifting the desired driver operating point (See output IV curves) along a 21Ω load line to define a convenient driver current for measurement.

Table 39: Output Characteristics

Parameter	Min	Nom	Max	Units	Notes
Output impedance	See "Full Strength Pull-Down Driver Characteristics" on page 108			Ω	1, 2
Pull-up and Pull-down mismatch	0		4	Ω	1, 2, 3
Output slew rate	1.5		5	V/ns	1, 4, 5, 6

Notes:
1. Absolute specifications: 0°C ≤ T_{case} ≤ +85°C; $V_{DD}Q$ = +1.8V ±0.1V, V_{DD} = +1.8V ±0.1V.
2. Impedance measurement conditions for output source DC current: $V_{DD}Q$ = 1.7V; V_{OUT} = 1,420mV; (V_{OUT} - $V_{DD}Q$)/I_{OH} must be less than 23.4Ω for values of V_{OUT} between $V_{DD}Q$ and $V_{DD}Q$ - 280mV. Impedance measurement condition for output sink DC current: $V_{DD}Q$ = 1.7V; V_{OUT} = 280mV; V_{OUT}/I_{OL} must be less than 23.4Ω for values of V_{OUT} between 0V and 280mV.
3. Mismatch is absolute value between pull-up and pull-down; both are measured at same temperature and voltage.
4. Output slew rate for falling and rising edges is measured between V_{TT} - 250mV and V_{TT} + 250mV for single-ended signals. For differential signals (DQS - DQS#), output slew rate is measured between DQS - DQS# = -500mV and DQS# - DQS = +500mV. Output slew rate is guaranteed by design, but is not necessarily tested on each device.
5. The absolute value of the slew rate as measured from V_{IL}(DC) MAX to V_{IH}(DC) MIN is equal to or greater than the slew rate as measured from V_{IL}(AC) MAX to V_{IH}(AC) MIN. This is guaranteed by design and characterization.
6. IT devices require an additional 0.4 V/ns in the MAX limit when T_C is between -40°C and 0°C.

Figure 83: Output Slew Rate Load



Full Strength Pull-Down Driver Characteristics

Figure 84: Full Strength Pull-Down Characteristics

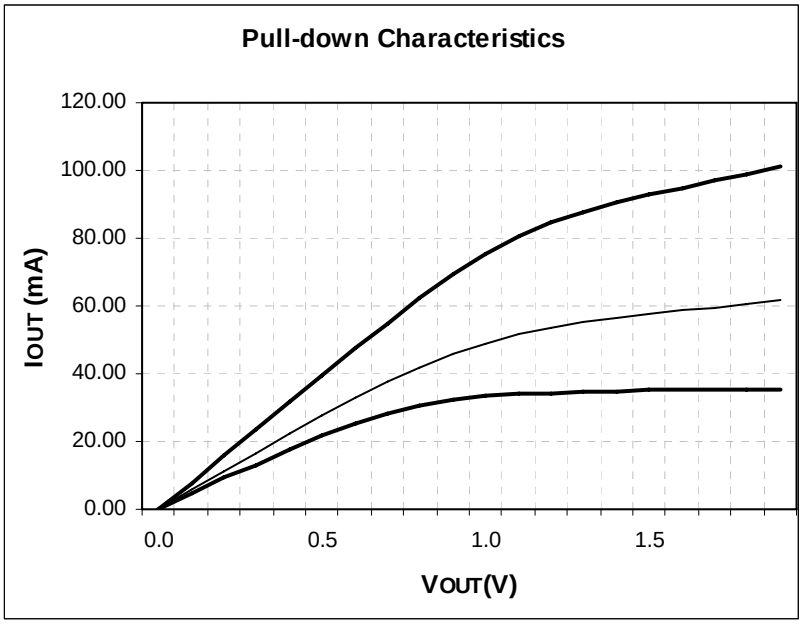


Table 40: Full Strength Pull-Down Current (mA)

Voltage (V)	Minimum	Nominal	Maximum
0.0	0.00	0.00	0.00
0.1	4.3	5.63	7.95
0.2	8.6	11.3	15.90
0.3	12.9	16.52	23.85
0.4	16.9	22.19	31.80
0.5	20.4	27.59	39.75
0.6	23.28	32.39	47.70
0.7	25.44	36.45	55.55
0.8	26.79	40.38	62.95
0.9	27.67	44.01	69.55
1.0	28.38	47.01	75.35
1.1	28.96	49.63	80.35
1.2	29.46	51.71	84.55
1.3	29.90	53.32	87.95
1.4	30.29	54.9	90.70
1.5	30.65	56.03	93.00
1.6	30.98	57.07	95.05
1.7	31.31	58.16	97.05
1.8	31.64	59.27	99.05
1.9	31.96	60.35	101.05

Full Strength Pull-Up Driver Characteristics

Figure 85: Full Strength Pull-up Characteristics

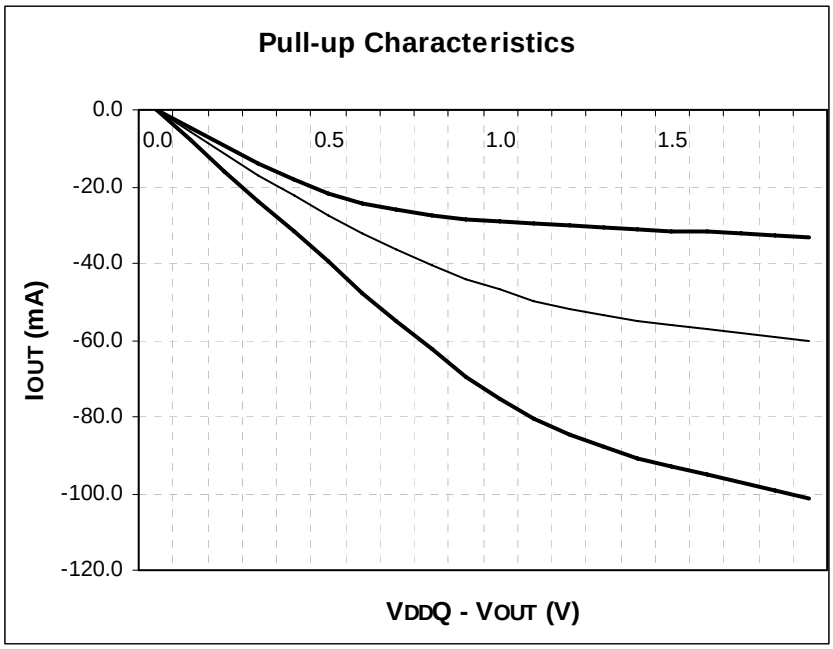


Table 41: Full Strength Pull-Up Current (mA)

Voltage (V)	Minimum	Nominal	Maximum
0.0	0.00	0.00	-0.00
0.1	-4.3	-5.63	-7.95
0.2	-8.6	-11.3	-15.90
0.3	-12.9	-16.52	-23.85
0.4	-16.9	-22.19	-31.80
0.5	-20.4	-27.59	-39.75
0.6	-23.28	-32.39	-47.70
0.7	-25.44	-36.45	-55.55
0.8	-26.79	-40.38	-62.95
0.9	-27.67	-44.01	-69.55
1.0	-28.38	-47.01	-75.35
1.1	-28.96	-49.63	-80.35
1.2	-29.46	-51.71	-84.55
1.3	-29.90	-53.32	-87.95
1.4	-30.29	-54.90	-90.70
1.5	-30.65	-56.03	-93.00
1.6	-30.98	-57.07	-95.05
1.7	-31.31	-58.16	-97.05
1.8	-31.64	-59.27	-99.05
1.9	-31.96	-60.35	-101.05

Reduced Strength Pull-Down Driver Characteristics

Figure 86: Reduced Strength Pull-Down Characteristics

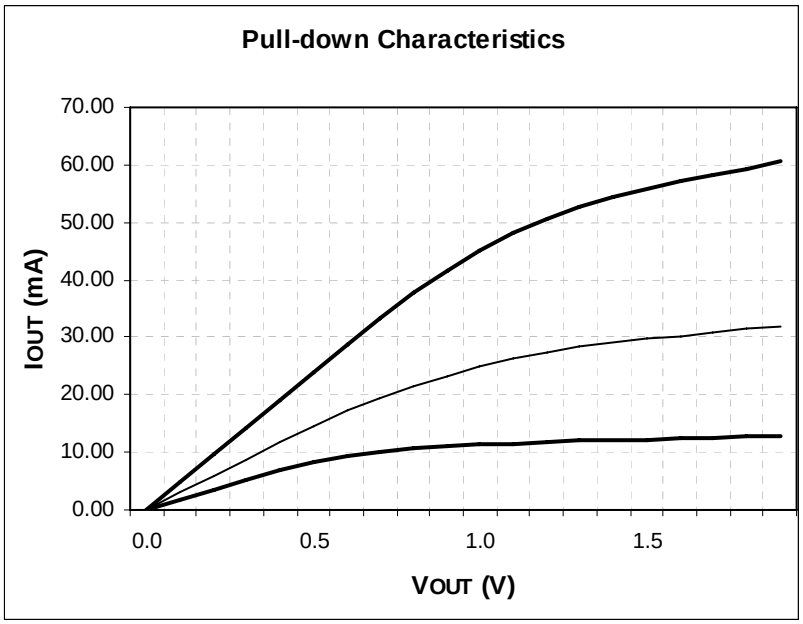


Table 42: Reduced Strength Pull-Down Current (mA)

Voltage (V)	Minimum	Nominal	Maximum
0.0	0.00	0.00	0.00
0.1	1.72	2.98	4.77
0.2	3.44	5.99	9.54
0.3	5.16	8.75	14.31
0.4	6.76	11.76	19.08
0.5	8.16	14.62	23.85
0.6	9.31	17.17	28.62
0.7	10.18	19.32	33.33
0.8	10.72	21.40	37.77
0.9	11.07	23.32	41.73
1.0	11.35	24.92	45.21
1.1	11.58	26.30	48.21
1.2	11.78	27.41	50.73
1.3	11.96	28.26	52.77
1.4	12.12	29.10	54.42
1.5	12.26	29.70	55.80
1.6	12.39	30.25	57.03
1.7	12.52	30.82	58.23
1.8	12.66	31.41	59.43
1.9	12.78	31.98	60.63

Reduced Strength Pull-Up Driver Characteristics

Figure 87: Reduced Strength Pull-up Characteristics

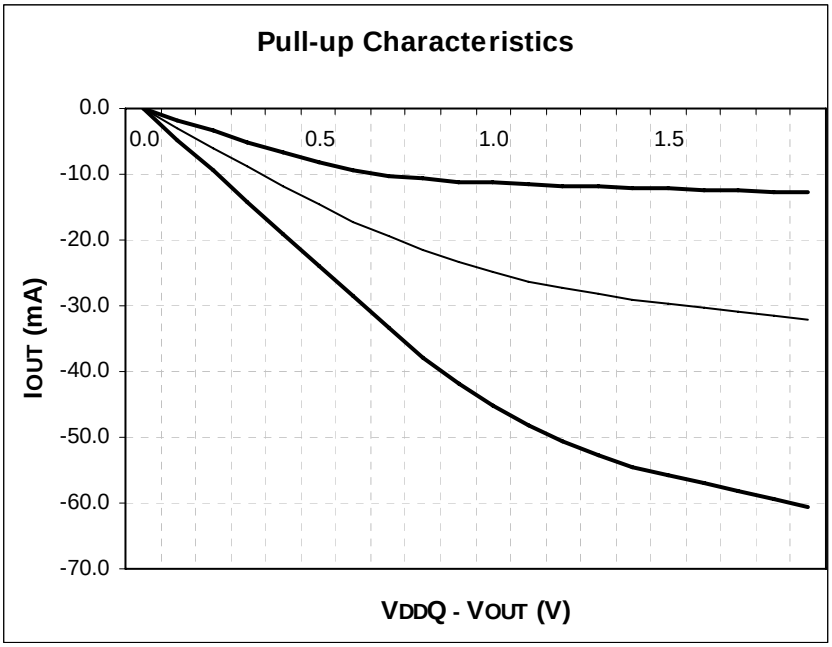


Table 43: Reduced Strength Pull-Up Current (mA)

Voltage (V)	Minimum	Nominal	Maximum
0.0	0.00	0.00	-0.00
0.1	-1.72	-2.98	-4.77
0.2	-3.44	-5.99	-9.54
0.3	-5.16	-8.75	-14.31
0.4	-6.76	-11.76	-19.08
0.5	-8.16	-14.62	-23.85
0.6	-9.31	-17.17	-28.62
0.7	-10.18	-19.32	-33.33
0.8	-10.72	-21.40	-37.77
0.9	-11.07	-23.32	-41.73
1.0	-11.35	-24.92	-45.21
1.1	-11.58	-26.30	-48.21
1.2	-11.78	-27.41	-50.73
1.3	-11.96	-28.26	-52.77
1.4	-12.12	-29.10	-54.42
1.5	-12.26	-29.69	-55.8
1.6	-12.39	-30.25	-57.03
1.7	-12.52	-30.82	-58.23
1.8	-12.66	-31.42	-59.43
1.9	-12.78	-31.98	-60.63

FBGA Package Capacitance

Table 44: Input Capacitance

Parameter	Symbol	Min	Max	Units	Notes
Input capacitance: CK, CK#	CCK	1.0	2.0	pF	1
Delta input capacitance: CK, CK#	CDCK	–	0.25	pF	2
Input capacitance: BA1–BA0, A0–A12, CS#, RAS#, CAS#, WE#, CKE, ODT	CI	1.0	2.0	pF	1
Delta input capacitance: BA1–BA0, A0–A12, CS#, RAS#, CAS#, WE#, CKE, ODT	CDI	–	0.25	pF	2
Input/Output capacitance: DQs, DQS, DM, NF	CIO	2.5	4.0	pF	1, 4
Delta input/output capacitance: DQs, DQS, DM, NF	CDIO	–	0.5	pF	3

Notes:
1. This parameter is sampled. V_{DD} = +1.8V ±0.1V, V_{DDQ} = +1.8V ±0.1V, V_{REF} = V_{SS}, f = 100 MHz, T_C = 25°C, $V_{OUT(DC)}$ = $V_{DDQ}/2$, V_{OUT} (peak to peak) = 0.1V. DM input is grouped with I/O balls, reflecting the fact that they are matched in loading.
2. The input capacitance per ball group will not differ by more than this maximum amount for any given device.
3. The I/O capacitance per DQS and DQ byte/group will not differ by more than this maximum amount for any given device.
4. Reduce MAX limit by 0.5pF for -3/-3E/-25E speed devices.
5. Reduce MAX limit by 0.25pF for -3/-3E/-25E speed devices.

IDD Specifications and Conditions

Table 45: DDR2 IDD Specifications and Conditions
Notes: 1–7; notes appear on page 114

Parameter/Condition	Sym	Config	-25E	-3E	-3	-37E	-5E	Units
Operating one bank active-precharge current: ^{t}CK = ^{t}CK (IDD), ^{t}RC = ^{t}RC (IDD), ^{t}RAS = ^{t}RAS MIN (IDD); CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are switching; Data bus inputs are switching	IDD0	x4, x8	100	90	90	80	75	mA
		x16	100	90	90	80	75	
Operating one bank active-read-precharge current: IOUT = 0mA; BL = 4, CL = CL (IDD), AL = 0; ^{t}CK = ^{t}CK (IDD), ^{t}RC = ^{t}RC (Idd), ^{t}RAS = ^{t}RAS MIN (IDD), ^{t}RCD = ^{t}RCD (IDD); CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are switching; Data pattern is same as IDD4W	IDD1	x4, x8	110	100	100	90	85	mA
		x16	110	100	100	90	85	
Precharge power-down current: All banks idle; ^{t}CK = ^{t}CK (IDD); CKE is LOW; Other control and address bus inputs are stable; Data bus inputs are floating	IDD2P	x4, x8, x16	5	5	5	5	5	mA
Precharge quiet standby current: All banks idle; ^{t}CK = ^{t}CK (IDD); CKE is HIGH, CS# is HIGH; Other control and address bus inputs are stable; Data bus inputs are floating	IDD2Q	x4, x8	45	40	40	35	25	mA
		x16	60	50	50	35	25	
Precharge standby current: All banks idle; ^{t}CK = ^{t}CK (IDD); CKE is HIGH, CS# is HIGH; Other control and address bus inputs are switching; Data bus inputs are switching	IDD2N	x4, x8	45	40	40	35	30	mA
		x16	45	40	40	35	30	
Active power-down current: All banks open; ^{t}CK = ^{t}CK (IDD); CKE is LOW; Other control and address bus inputs are stable; Data bus inputs are floating	IDD3P	Fast PDN Exit MR[12] = 0	35	30	30	25	20	mA
		Slow PDN Exit MR[12] = 1	6	6	6	6	6	
Active standby current: All banks open; ^{t}CK = ^{t}CK (IDD), ^{t}RAS = ^{t}RAS MAX (IDD), ^{t}RP = ^{t}RP (IDD); CKE is HIGH, CS# is HIGH between valid commands; Other control and address bus inputs are switching; Data bus inputs are switching	IDD3N	x4, x8	55	50	50	40	30	mA
		x16	65	55	55	40	30	
Operating burst write current: All banks open, continuous burst writes; BL = 4, CL = CL (IDD), AL = 0; ^{t}CK = ^{t}CK (IDD), ^{t}RAS = ^{t}RAS MAX (IDD), ^{t}RP = ^{t}RP (IDD); CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are switching; Data bus inputs are switching	IDD4W	x4, x8	220	190	190	160	125	mA
		x16	250	215	215	180	140	
Operating burst read current: All banks open, continuous burst reads, IOUT = 0mA; BL = 4, CL = CL (IDD), AL = 0; ^{t}CK = ^{t}CK (IDD), ^{t}RAS = ^{t}RAS MAX (IDD), ^{t}RP = ^{t}RP (IDD); CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are switching; Data bus inputs are switching	IDD4R	x4, x8	210	180	180	150	115	mA
		x16	220	190	190	160	120	
Burst refresh current: ^{t}CK = ^{t}CK (IDD); refresh command at every ^{t}RFC (IDD) interval; CKE is HIGH, CS# is HIGH between valid commands; Other control and address bus inputs are switching; Data bus inputs are switching	IDD5	x4, x8	200	180	180	170	165	mA
		x16	200	180	180	170	165	
Self refresh current: CK and CK# at 0V; CKE ≤ 0.2V; Other control and address bus inputs are floating; Data bus inputs are floating	IDD6	x4, x8, x16	5	5	5	5	5	mA
	IDD6L	x4, x8, x16	3	3	3	3	3	

Table 45: DDR2 IDD Specifications and Conditions (Continued)
Notes: 1–7; notes appear on page 114

Parameter/Condition	Sym	Config	-25E	-3E	-3	-37E	-5E	Units
Operating bank interleave read current: All bank interleaving reads, IOUT= 0mA; BL = 4, CL = CL (IDD), AL = tRCD (IDD) - 1 x tCK (IDD); tCK = tCK (IDD), tRC = tRC (IDD), tRRD = tRRD (IDD), tRCD = tRCD (IDD); CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are stable during deselects; Data bus inputs are switching; See "IDD7 Conditions" on page 115 for detail	IDD7	x4, x8	290	260	250	240	230	mA
		x16						

Notes:
1. IDD specifications are tested after the device is properly initialized. 0°C ≤ T_{case} ≤ +85°C. VDD = +1.8V ±0.1V, VDDQ = +1.8V ±0.1V, VDDL = +1.8V ±0.1V, VREF = VDDQ/2. -37V VDDQ = +1.9V ±0.1V, VDDL = +1.9V ±0.1.
2. Input slew rate is specified by AC Parametric Test Conditions.
3. IDD parameters are specified with ODT disabled.
4. Data bus consists of DQ, DM, DQS, DQS#, RDQS, RDQS#, LDQS, LDQS#, UDQS, and UDQS#. IDD values must be met with all combinations of EMR bits 10 and 11.
5. Definitions for IDD Conditions:
   LOW is defined as VIN ≤ VIL(AC) MAX; HIGH is defined as VIN ≥ VIH(AC) MIN; Stable is defined as inputs stable at a HIGH or LOW level; Floating is defined as inputs at VREF = VDDQ/2; Switching is defined as inputs changing between HIGH and LOW every other clock cycle (once per two clocks) for address and control signals; Switching is defined as inputs changing between HIGH and LOW every other data transfer (once per clock) for DQ signals, not including masks or strobes.
6. IDD1, IDD4R, and IDD7 require A12 in EMR1 to be enabled during testing.
7. The following IDDs must be derated (IDD limits increase) on IT-option devices when operated outside of the range 0°C ≤ T_C ≤ 85°C. When T_C ≤ 0°C, IDD2 and IDD3P(slow) must be derated by 4 percent; IDD4R and IDD5W must be derated by 2 percent; and IDD6 and IDD7 must be derated by 7 percent. When T_C ≥ 85°C, IDD0, IDD1, IDD2N, IDD2Q, IDD3N, IDD3P(fast), IDD4R, IDD4W, and IDD5W must be derated by 2 percent; IDD2P must be derated by 10 percent; IDD3Pslow must be derated by 15 percent; and IDD6 must be derated by 80 percent (IDD6 will increase by this amount if T_C < 85°C and the 2x refresh option is still enabled).

Table 46: General IDD Parameters

IDD Parameter	-25E	-3E	-3	-37E	-5E	Units
CL (IDD)	5	4	5	4	3	tCK
tRCD (IDD)	12.5	12	15	15	15	ns
tRC (IDD)	57.5	57	60	60	55	ns
tRRD (IDD) - x4/x8 (1KB)	7.5	7.5	7.5	7.5	7.5	ns
tRRD (IDD) - x16 (2KB)	10	10	10	10	10	ns
tCK (IDD)	2.5	3	3	3.75	5	ns
tRAS MIN (IDD)	45	45	45	45	40	ns
tRAS MAX (IDD)	70,000	70,000	70,000	70,000	70,000	ns
tRP (IDD)	12.5	12	15	15	15	ns
tRFC (IDD)	75	75	75	75	75	ns
tFAW (1KB)	35	37.5	37.5	37.5	37.5	ns
tFAW (2KB)	45	50	50	50	50	ns

IDD7 Conditions

The detailed timings are shown below for IDD7. Changes will be required if timing parameter changes are made to the specification. Where general IDD parameters in Table 46 conflict with pattern requirements of Table 47, then Table 47 requirements take precedence.

Table 47: IDD7 Timing Patterns (4-bank)
All bank interleave READ operation

Speed Grade	IDD7 Timing Patterns for x4/x8/x16
-5E	A0 RA0 A1 RA1 A2 RA2 A3 RA3 D D D
-37E	A0 RA0 D A1 RA1 D A2 RA2 D A3 RA3 D D D D D
-3	A0 RA0 D D A1 RA1 D D A2 RA2 D D A3 RA3 D D D D D D
-3E	A0 RA0 D D A1 RA1 D D A2 RA2 D D A3 RA3 D D D D D
-25	A0 RA0 D D A1 RA1 D D A2 RA2 D D A3 RA3 D D D D D D D D D D
-25E	A0 RA0 D D A1 RA1 D D A2 RA2 D D A3 RA3 D D D D D D D D D

Notes: 1. A = active; RA = read auto precharge; D = deselect.
2. All banks are being interleaved at minimum tRC (IDD) without violating tRRD (IDD) using a BL = 4.
3. Control and address bus inputs are STABLE during DESELECTs.
4. IOUT = 0mA.

AC Operating Specifications

Table 48: AC Operating Conditions for -3E, -3, -37E and -5E Speeds (Sheet 1 of 6)

Notes: 1–5; notes appear on page 125; VDDQ = +1.8V ±0.1V, VDD = +1.8V ±0.1V

AC Characteristics				-3E		-3		-37E		-5E		Units	Notes
	Parameter		Symbol	Min	Max	Min	Max	Min	Max	Min	Max		
Clock	Clock cycle time	CL = 5	$^{t}CK_{AVG}(5)$	3,000	8,000	3,000	8,000	–	–	–	–	ps	16, 22, 36, 38
		CL = 4	$^{t}CK_{AVG}(4)$	3,000	8,000	3,750	8,000	3,750	8,000	5,000	8,000	ps	
		CL = 3	$^{t}CK_{AVG}(3)$	–	–	5,000	8,000	5,000	8,000	5,000	8,000	ps	
	CK high-level width		$^{t}CH_{AVG}$	0.48	0.52	0.48	0.52	0.48	0.52	0.48	0.52	^{t}CK	45
	CK low-level width		$^{t}CL_{AVG}$	0.48	0.52	0.48	0.52	0.48	0.52	0.48	0.52	^{t}CK	
	Half clock period		^{t}HP	MIN (^{t}CH, ^{t}CL)		MIN (^{t}CH, ^{t}CL)		MIN (^{t}CH, ^{t}CL)		MIN (^{t}CH, ^{t}CL)		ps	46
Clock (absolute)	Absolute ^{t}CK		$^{t}CK_{abs}$	$^{t}CK_{AVG}$ (MIN) + $^{t}JIT_{PER}$ (MIN)	$^{t}CK_{AVG}$ (MAX) + $^{t}JIT_{PER}$ (MAX)	$^{t}CK_{AVG}$ (MIN) + $^{t}JIT_{PER}$ (MIN)	$^{t}CK_{AVG}$ (MAX) + $^{t}JIT_{PER}$ (MAX)	$^{t}CK_{AVG}$ (MIN) + $^{t}JIT_{PER}$ (MIN)	$^{t}CK_{AVG}$ (MAX) + $^{t}JIT_{PER}$ (MAX)	$^{t}CK_{AVG}$ (MIN) + $^{t}JIT_{PER}$ (MIN)	$^{t}CK_{AVG}$ (MAX) + $^{t}JIT_{PER}$ (MAX)	ps	
	Absolute CK high-level width		$^{t}CH_{abs}$	$^{t}CK_{AVG}$ (MIN) * $^{t}CH_{AVG}$ (MIN) + $^{t}JIT_{DTY}$ (MIN)	$^{t}CK_{AVG}$ (MAX) * $^{t}CH_{AVG}$ (MAX) + $^{t}JIT_{DTY}$ (MAX)	$^{t}CK_{AVG}$ (MIN) * $^{t}CH_{AVG}$ (MIN) + $^{t}JIT_{DTY}$ (MIN)	$^{t}CK_{AVG}$ (MAX) * $^{t}CH_{AVG}$ (MAX) + $^{t}JIT_{DTY}$ (MAX)	$^{t}CK_{AVG}$ (MIN) * $^{t}CH_{AVG}$ (MIN) + $^{t}JIT_{DTY}$ (MIN)	$^{t}CK_{AVG}$ (MAX) * $^{t}CH_{AVG}$ (MAX) + $^{t}JIT_{DTY}$ (MAX)	$^{t}CK_{AVG}$ (MIN) * $^{t}CH_{AVG}$ (MIN) + $^{t}JIT_{DTY}$ (MIN)	$^{t}CK_{AVG}$ (MAX) * $^{t}CH_{AVG}$ (MAX) + $^{t}JIT_{DTY}$ (MAX)	ps	
	Absolute CK low-level width		$^{t}CL_{abs}$	$^{t}CK_{AVG}$ (MIN) * $^{t}CL_{AVG}$ (MIN) + $^{t}JIT_{DTY}$ (MIN)	$^{t}CK_{AVG}$ (MAX) * $^{t}CL_{AVG}$ (MAX) + $^{t}JIT_{DTY}$ (MAX)	$^{t}CK_{AVG}$ (MIN) * $^{t}CL_{AVG}$ (MIN) + $^{t}JIT_{DTY}$ (MIN)	$^{t}CK_{AVG}$ (MAX) * $^{t}CL_{AVG}$ (MAX) + $^{t}JIT_{DTY}$ (MAX)	$^{t}CK_{AVG}$ (MIN) * $^{t}CL_{AVG}$ (MIN) + $^{t}JIT_{DTY}$ (MIN)	$^{t}CK_{AVG}$ (MAX) * $^{t}CL_{AVG}$ (MAX) + $^{t}JIT_{DTY}$ (MAX)	$^{t}CK_{AVG}$ (MIN) * $^{t}CL_{AVG}$ (MIN) + $^{t}JIT_{DTY}$ (MIN)	$^{t}CK_{AVG}$ (MAX) * $^{t}CL_{AVG}$ (MAX) + $^{t}JIT_{DTY}$ (MAX)	ps	
Clock Jitter	Clock jitter – period		$^{t}JIT_{PER}$	-125	125	-125	125	-125	125	-125	125	ps	39
	Clock jitter – half period		$^{t}JIT_{DUTY}$	-125	125	-125	125	-125	125	-150	150	ps	40
	Clock jitter – cycle to cycle		$^{t}JIT_{CC}$	250		250		250		250		ps	41
	Cumulative jitter error, 2 cycles		$^{t}ERR_{2per}$	-175	175	-175	175	-175	175	-175	175	ps	42
	Cumulative jitter error, 3 cycles		$^{t}ERR_{3per}$	-225	225	-225	225	-225	225	-225	225	ps	42
	Cumulative jitter error, 4 cycles		$^{t}ERR_{4per}$	-250	250	-250	250	-250	250	-250	250	ps	42
	Cumulative jitter error, 5 cycles		$^{t}ERR_{5per}$	-250	250	-250	250	-250	250	-250	250	ps	42, 48
	Cumulative jitter error, 6–10 cycles		$^{t}ERR_{6-10per}$	-350	350	-350	350	-350	350	-350	350	ps	42, 48
	Cumulative jitter error, 11–50 cycles		$^{t}ERR_{11-50per}$	-450	450	-450	450	-450	450	-450	450	ps	42

Table 48: AC Operating Conditions for -3E, -3, -37E and -5E Speeds (Sheet 2 of 6)

Notes: 1–5; notes appear on page 125; $V_{DD}Q$ = +1.8V ±0.1V, V_{DD} = +1.8V ±0.1V

AC Characteristics			-3E		-3		-37E		-5E		Units	Notes
	Parameter	Symbol	Min	Max	Min	Max	Min	Max	Min	Max		
Data	DQ hold skew factor	^tQHS	–	340	–	340	–	400	–	450	ps	47
	DQ output access time from CK/CK#	^tAC	-450	+450	-450	+450	-500	+500	-600	+600	ps	43
	Data-out high-impedance window from CK/CK#	^tHZ		^tAC (MAX)		^tAC (MAX)		^tAC (MAX)		^tAC (MAX)	ps	8, 9, 43
	DQS low-impedance window from CK/CK#	$^tLZ_1$	^tAC (MIN)	^tAC (MAX)	^tAC (MIN)	^tAC (MAX)	^tAC (MIN)	^tAC (MAX)	^tAC (MIN)	^tAC (MAX)	ps	8, 10, 43
	DQ low-impedance window from CK/CK#	$^tLZ_2$	2 * ^tAC (MIN)	^tAC (MAX)	2 * ^tAC (MIN)	^tAC (MAX)	2 * ^tAC (MIN)	^tAC (MAX)	2 * ^tAC (MIN)	^tAC (MAX)	ps	8, 10, 43
	DQ and DM input setup time relative to DQS	^tDS_a	300		300		350		400		ps	7, 15, 19
	DQ and DM input hold time relative to DQS	^tDH_a	300		300		350		400		ps	7, 15, 19
	DQ and DM input setup time relative to DQS	^tDS_b	100		100		100		150		ps	7, 15, 19
	DQ and DM input hold time relative to DQS	^tDH_b	175		175		225		275		ps	7, 15, 19
	DQ and DM input pulse width (for each input)	^tDIPW	0.35		0.35		0.35		0.35		^tCK	37
	Data hold skew factor	^tQHS		340		340		400		450	ps	47
	DQ–DQS hold, DQS to first DQ to go nonvalid, per access	^tQH	^tHP - ^tQHS		^tHP - ^tQHS		^tHP - ^tQHS		^tHP - ^tQHS		ps	15, 17, 47
	Data valid output window (DVW)	^tDVW	^tQH - ^tDQSQ		^tQH - ^tDQSQ		^tQH - ^tDQSQ		^tQH - ^tDQSQ		ns	15, 17

Table 48: AC Operating Conditions for -3E, -3, -37E and -5E Speeds (Sheet 3 of 6)

Notes: 1–5; notes appear on page 125; V_{DDQ} = +1.8V ±0.1V, V_{DD} = +1.8V ±0.1V

AC Characteristics			-3E		-3		-37E		-5E		Units	Notes
	Parameter	Symbol	Min	Max	Min	Max	Min	Max	Min	Max		
Data Strobe	DQS input-high pulse width	^{t}DQSH	0.35		0.35		0.35		0.35		^{t}CK	37
	DQS input-low pulse width	^{t}DQSL	0.35		0.35		0.35		0.35		^{t}CK	37
	DQS output access time from CK/CK#	^{t}DQSCK	-400	+400	-400	+400	-450	+450	-500	+500	ps	40
	DQS falling edge to CK rising – setup time	^{t}DSS	0.2		0.2		0.2		0.2		^{t}CK	37
	DQS falling edge from CK rising – hold time	^{t}DSH	0.2		0.2		0.2		0.2		^{t}CK	37
	DQS–DQ skew, DQS to last DQ valid, per group, per access	^{t}DQSQ		240		240		300		350	ps	15, 17
	DQS read preamble	^{t}RPRE	0.9	1.1	0.9	1.1	0.9	1.1	0.9	1.1	^{t}CK	33, 37, 43
	DQS read postamble	^{t}RPST	0.4	0.6	0.4	0.6	0.4	0.6	0.4	0.6	^{t}CK	33, 34, 37, 43
	DQS write preamble setup time	^{t}WPRES	0		0		0		0		ps	12, 13
	DQS write preamble	^{t}WPRE	0.35		0.35		0.25		0.25		^{t}CK	37
	DQS write postamble	^{t}WPST	0.4	0.6	0.4	0.6	0.4	0.6	0.4	0.6	^{t}CK	11, 37
	Positive DQS latching edge to associated clock edge	^{t}DQSS	-0.25	0.25	-0.25	0.25	-0.25	0.25	-0.25	0.25	^{t}CK	37
	WRITE command to first DQS latching transition		WL - ^{t}DQSS	WL + ^{t}DQSS	WL - ^{t}DQSS	WL + ^{t}DQSS	WL - ^{t}DQSS	WL + ^{t}DQSS	WL - ^{t}DQSS	WL + ^{t}DQSS	^{t}CK	

Table 48: AC Operating Conditions for -3E, -3, -37E and -5E Speeds (Sheet 4 of 6)
Notes: 1–5; notes appear on page 125; VDDQ = +1.8V ±0.1V, VDD = +1.8V ±0.1V

AC Characteristics			-3E		-3		-37E		-5E		Units	Notes
	Parameter	Symbol	Min	Max	Min	Max	Min	Max	Min	Max		
Command and Address	Address and control input pulse width for each input	^{t}IPW	0.6		0.6		0.6		0.6		^{t}CK	37
	Address and control input setup time	$^{t}IS_a$	400		400		500		600		ps	6, 19
	Address and control input hold time	$^{t}IH_a$	400		400		500		600		ps	6, 19
	Address and control input setup time	$^{t}IS_b$	200		200		250		350		ps	6, 19
	Address and control input hold time	$^{t}IH_b$	275		275		375		475		ps	6, 19
	CAS# to CAS# command delay	^{t}CCD	2		2		2		2		^{t}CK	37
	ACTIVE-to-ACTIVE (same bank) command	^{t}RC	54		55		55		55		ns	31, 37
	ACTIVE bank *a* to ACTIVE bank *b* command	^{t}RRD (x4, x8)	7.5		7.5		7.5		7.5		ns	25, 37
		^{t}RRD (x16)	10		10		10		10		ns	25, 37
	ACTIVE-to-READ or WRITE delay	^{t}RCD	12		15		15		15		ns	37
	4-Bank activate period	^{t}FAW (x4, x8)	37.5		37.5		37.5		37.5		ns	28, 37
	4-Bank activate period	^{t}FAW (x16)	50		50		50		50		ns	28, 37
	ACTIVE-to-PRECHARGE command	^{t}RAS	40	70,000	40	70,000	40	70,000	40	70,000	ns	18, 31, 37
	Internal READ to PRECHARGE command delay	^{t}RTP	7.5		7.5		7.5		7.5		ns	21, 25, 37
	Write recovery time	^{t}WR	15		15		15		15		ns	25, 37
	Auto precharge write recovery + precharge time	^{t}DAL	^{t}WR + ^{t}RP		^{t}WR + ^{t}RP		^{t}WR + ^{t}RP		^{t}WR + ^{t}RP		ns	20
	Internal WRITE-to-READ command delay	^{t}WTR	7.5		7.5		7.5		10		ns	25, 37
	PRECHARGE command period	^{t}RP	12		15		15		15		ns	29, 37
	PRECHARGE ALL command period	^{t}RPA	^{t}RP + ^{t}CK		^{t}RP + ^{t}CK		^{t}RP + ^{t}CK		^{t}RP + ^{t}CK		ns	29
	LOAD MODE command cycle time	^{t}MRD	2		2		2		2		^{t}CK	37

Table 48: AC Operating Conditions for -3E, -3, -37E and -5E Speeds (Sheet 5 of 6)

Notes: 1–5; notes appear on page 125; $V_{DD}Q$ = +1.8V ±0.1V, V_{DD} = +1.8V ±0.1V

AC Characteristics			-3E		-3		-37E		-5E		Units	Notes
	Parameter	Symbol	Min	Max	Min	Max	Min	Max	Min	Max		
Refresh	CKE LOW to CK, CK# uncertainty	^{t}DELAY	^{t}IS + ^{t}CK + ^{t}IH		^{t}IS + ^{t}CK + ^{t}IH		^{t}IS + ^{t}CK + ^{t}IH		^{t}IS + ^{t}CK + ^{t}IH		ns	26
	REFRESH to ACTIVE or REFRESH to REFRESH command interval	^{t}RFC	75	70,000	75	70,000	75	70,000	75	70,000	ns	14, 37
	Average periodic refresh interval (commercial)	^{t}REFI		7.8		7.8		7.8		7.8	µs	14, 37
	Average periodic refresh interval (industrial)	^{t}REFI$_{IT}$		3.9		3.9		3.9		3.9	µs	14, 37
Self Refresh	Exit SELF REFRESH to non-READ command	^{t}XSNR	^{t}RFC (MIN) + 10		^{t}RFC (MIN) + 10		^{t}RFC (MIN) + 10		^{t}RFC (MIN) + 10		ns	
	Exit SELF REFRESH to READ command	^{t}XSRD	200		200		200		200		^{t}CK	37
	Exit SELF REFRESH timing reference	^{t}ISXR	^{t}IS		^{t}IS		^{t}IS		^{t}IS		ps	6, 27
ODT	ODT turn-on delay	^{t}AOND	2	2	2	2	2	2	2	2	^{t}CK	37
	ODT turn-on	^{t}AON	^{t}AC (MIN)	^{t}AC (MAX) + 700	^{t}AC (MIN)	^{t}AC (MAX) + 700	^{t}AC (MIN)	^{t}AC (MAX) + 1,000	^{t}AC (MIN)	^{t}AC (MAX) + 1000	ps	23, 43
	ODT turn-off delay	^{t}AOFD	2.5	2.5	2.5	2.5	2.5	2.5	2.5	2.5	^{t}CK	35, 37
	ODT turn-off	^{t}AOF	^{t}AC (MIN)	^{t}AC (MAX) + 600	^{t}AC (MIN)	^{t}AC (MAX) + 600	^{t}AC (MIN)	^{t}AC (MAX) + 600	^{t}AC (MIN)	^{t}AC (MAX) + 600	ps	24, 44
	ODT turn-on (power-down mode)	^{t}AONPD	^{t}AC (MIN) + 2,000	2 x ^{t}CK + ^{t}AC (MAX) + 1,000	^{t}AC (MIN) + 2,000	2 x ^{t}CK + ^{t}AC (MAX) + 1,000	^{t}AC (MIN) + 2000	2 x ^{t}CK + ^{t}AC (MAX) + 1,000	^{t}AC (MIN) + 2,000	2 x ^{t}CK + ^{t}AC (MAX) + 1000	ps	
	ODT turn-off (power-down mode)	^{t}AOFPD	^{t}AC (MIN) + 2,000	2.5 x ^{t}CK + ^{t}AC (MAX) + 1,000	^{t}AC (MIN) + 2,000	2.5 x ^{t}CK + ^{t}AC (MAX) + 1,000	^{t}AC (MIN) + 2,000	2.5 x ^{t}CK + ^{t}AC (MAX) + 1,000	^{t}AC (MIN) + 2,000	2.5 x ^{t}CK + ^{t}AC (MAX) + 1,000	ps	
	ODT to power-down entry latency	^{t}ANPD	3		3		3		3		^{t}CK	37
	ODT power-down exit latency	^{t}AXPD	8		8		8		8		^{t}CK	37
	ODT enable from MRS command	^{t}MOD	12		12		12		12		ns	37, 49

Table 48: AC Operating Conditions for -3E, -3, -37E and -5E Speeds (Sheet 6 of 6)

Notes: 1–5; notes appear on page 125; $V_{DD}Q$ = +1.8V ±0.1V, V_{DD} = +1.8V ±0.1V

AC Characteristics			-3E		-3		-37E		-5E		Units	Notes
	Parameter	Symbol	Min	Max	Min	Max	Min	Max	Min	Max		
Power-Down	Exit active power-down to READ command, MR[12] = 0	^{t}XARD	2		2		2		2		^{t}CK	37
	Exit active power-down to READ command, MR[12] = 1	^{t}XARDS	7 - AL		7 - AL		6 - AL		6 - AL		^{t}CK	37
	Exit precharge power-down to any non-READ command	^{t}XP	2		2		2		2		^{t}CK	37
	CKE MIN HIGH/LOW time	^{t}CKE	3		3		3		3		^{t}CK	32, 37

Table 49: AC Operating Conditions for -25E (Sheet 1 of 3)

Notes: 1–5; notes appear on page 125; $V_{DD}Q$ = +1.8V ±0.1V, V_{DD} = +1.8V ±0.1V

AC Characteristics				-25E		Units	Notes
	Parameter		Symbol	Min	Max		
Clock	Clock cycle time	CL = 6	$^tCK_{AVG}(6)$	N/A	N/A	ps	16, 22, 36, 38
		CL = 5	$^tCK_{AVG}(5)$	2,500	8,000	ps	
		CL = 4	$^tCK_{AVG}(4)$	3,750	8,000	ps	
	CK high-level width		$^tCH_{AVG}$	0.48	0.52	^tCK	45
	CK low-level width		$^tCL_{AVG}$	0.48	0.52	^tCK	45
	Half clock period		^tHP	MIN (^tCH, ^tCL)		ps	46
	Absolute ^tCK		$^tCK_{abs}$	$^tCK_{AVG(MIN)}$ + $^tJIT_{PER(MIN)}$	$^tCK_{AVG(MAX)}$ + $^tJIT_{PER(MAX)}$	ps	
	Absolute CK high-level width		$^tCH_{ABS}$	$^tCK_{AVG(MIN)}$ * $^tCH_{AVG(MIN)}$ + $^tJIT_{DTY(MIN)}$	$^tCK_{AVG(MAX)}$ * $^tCH_{AVG(MAX)}$ + $^tJIT_{DTY(MAX)}$	ps	
	Absolute CK low-level width		$^tCL_{ABS}$	$^tCK_{AVG(MIN)}$ * $^tCL_{AVG(MIN)}$ + $^tJIT_{DTY(MIN)}$	$^tCK_{AVG(MAX)}$ * $^tCL_{AVG(MAX)}$ + $^tJIT_{DTY(MAX)}$	ps	
Clock Jitter	Clock jitter – period		$^tJIT_{PER}$	-100	100	ps	
	Clock jitter –half period		$^tJIT_{DUTY}$	-100	100	ps	40
	Clock jitter– cycle to cycle		$^tJIT_{CC}$	200		ps	41
	Cumulative jitter error, 2 cycles		$^tERR_{2per}$	-150	150	ps	42
	Cumulative jitter error, 3 cycles		$^tERR_{3per}$	-175	175	ps	42
	Cumulative jitter error, 4 cycles		$^tERR_{4per}$	-200	200	ps	42
	Cumulative jitter error, 5 cycles		$^tERR_{5per}$	-200	200	ps	42, 48
	Cumulative jitter error,6–10 cycles		$^tERR_{6-10per}$	-300	300	ps	42, 48
	Cumulative jitter error, 11–50 cycles		$^tERR_{11-50per}$	-450	450	ps	42, 48
Data	DQ output access time from CK/CK#		^tAC	-400	+400	ps	43
	Data-out high-impedance window from CK/CK#		^tHZ		^tAC (MAX)	ps	8, 9, 43
	DQS low-impedance window from CK/CK#		$^tLZ_1$	^tAC (MIN)	^tAC (MAX)	ps	8, 10, 43
	DQ low-impedance window from CK/CK#		$^tLZ_2$	2 * ^tAC (MIN)	^tAC (MAX)	ps	8, 10, 43
	DQ and DM input setup time relative to DQS		^tDS_a	250		ps	7, 15, 19
	DQ and DM input hold time relative to DQS		^tDH_a	250		ps	7, 15, 19
	DQ and DM input setup time relative to DQS		^tDS_b	50		ps	7, 15, 19
	DQ and DM input hold time relative to DQS		^tDH_b	125		ps	7, 15, 19
	DQ and DM input pulse width (for each input)		^tDIPW	0.35		^tCK	37
	Data hold skew factor		^tQHS		300	ps	47
	DQ–DQS output hold from DQS		^tQH	^tHP - ^tQHS		ps	15, 17, 47
	Data valid output window (DVW)		^tDVW	^tQH - ^tDQSQ		ns	15, 17, 19

Table 49: AC Operating Conditions for -25E (Sheet 2 of 3)

Notes: 1–5; notes appear on page 125; VDDQ = +1.8V ±0.1V, VDD = +1.8V ±0.1V

AC Characteristics			-25E		Units	Notes
	Parameter	Symbol	Min	Max		
Data Strobe	DQS input-high pulse width	^{t}DQSH	0.35		^{t}CK	37
	DQS input-low pulse width	^{t}DQSL	0.35		^{t}CK	37
	DQS output access time from CK/CK#	^{t}DQSCK	-350	+350	ps	40
	DQS falling edge to CK rising – setup time	^{t}DSS	0.2		^{t}CK	37
	DQS falling edge from CK rising – hold time	^{t}DSH	0.2		^{t}CK	37
	DQS–DQ skew, DQS to last DQ valid, per group, per access	^{t}DQSQ		200	ps	15, 17,
	DQS read preamble	^{t}RPRE	0.9	1.1	^{t}CK	33, 37, 43
	DQS read postamble	^{t}RPST	0.4	0.6	^{t}CK	33, 34, 37, 43
	DQS write preamble setup time	^{t}WPRES	0		ps	12, 13
	DQS write preamble	^{t}WPRE	0.35		^{t}CK	37
	DQS write postamble	^{t}WPST	0.4	0.6	^{t}CK	11, 37
	Positive DQS latching edge to associated clock edge	^{t}DQSS	-0.25	+0.25	^{t}CK	37
	WRITE command to first DQS latching transition		WL - ^{t}DQSS	WL + ^{t}DQSS	^{t}CK	
Command and Address	Address and control input pulse width for each input	^{t}IPW	0.6		^{t}CK	37
	Address and control input setup time	$^{t}IS_a$	400		ps	6, 19
	Address and control input hold time	$^{t}IH_a$	400		ps	6, 19
	Address and control input setup time	$^{t}IS_b$	200		ps	6, 19
	Address and control input hold time	$^{t}IH_b$	275		ps	6, 19
	CAS# to CAS# command delay	^{t}CCD	2		^{t}CK	37
	ACTIVE to ACTIVE (same bank) command	^{t}RC	55		ns	31, 37
	ACTIVE bank *a* to ACTIVE bank *b* command	^{t}RRD (x4, x8)	7.5		ns	25, 37
		^{t}RRD (x16)	10		ns	25, 37
	ACTIVE to READ or WRITE delay	^{t}RCD	12		ns	37
	4-bank activate period	^{t}FAW (1K page)	37.5		ns	28, 37
	4-bank activate period	^{t}FAW (2K page)	50		ns	28, 37
	ACTIVE-to-PRECHARGE command	^{t}RAS	40	70,000	ns	18, 34, 37
	Internal READ to PRECHARGE command delay	^{t}RTP	7.5		ns	21, 25, 37
	Write recovery time	^{t}WR	15		ns	25, 37
	Auto precharge write recovery + precharge time	^{t}DAL	^{t}WR + ^{t}RP		ns	20
	Internal WRITE-to-READ command delay	^{t}WTR	7.5		ns	25, 37
	PRECHARGE command period	^{t}RP	12.5		ns	32, 37
	PRECHARGE ALL command period	^{t}RPA	^{t}RP + ^{t}CK		ns	32
	LOAD MODE command cycle time	^{t}MRD	2		^{t}CK	37

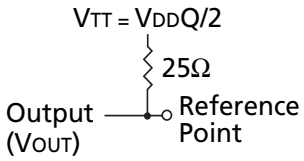
Table 49: AC Operating Conditions for -25E (Sheet 3 of 3)

Notes: 1–5; notes appear on page 125; $V_{DD}Q$ = +1.8V ±0.1V, V_{DD} = +1.8V ±0.1V

AC Characteristics			-25E		Units	Notes
	Parameter	Symbol	Min	Max		
Refresh	CKE low to CK, CK# uncertainty	^{t}DELAY	^{t}IS + ^{t}CK + ^{t}IH		ns	26
	REFRESH-to-ACTIVE or REFRESH-to-REFRESH command interval	^{t}RFC	75	70,000	ns	14, 37
	Average periodic refresh interval	^{t}REFI		7.8	µs	14, 37
	Average periodic refresh interval (industrial)	^{t}REFI$_{IT}$		3.9	µs	14, 37
Self Refresh	Exit self refresh to non-READ command	^{t}XSNR	^{t}RFC (MIN) + 10		ns	
	Exit self refresh to READ command	^{t}XSRD	200		^{t}CK	37
	Exit self refresh timing reference	^{t}ISXR	^{t}IS		ps	6, 30
ODT	ODT turn-on delay	^{t}AOND	2	2	^{t}CK	37
	ODT turn-on	^{t}AON	^{t}AC (MIN)	^{t}AC (MAX) + 700	ps	23, 43
	ODT turn-off delay	^{t}AOFD	2.5	2.5	^{t}CK	35, 37
	ODT turn-off	^{t}AOF	^{t}AC (MIN)	^{t}AC (MAX) + 600	ps	24, 44
	ODT turn-on (power-down mode)	^{t}AONPD	^{t}AC (MIN) + 2,000	2 x ^{t}CK + ^{t}AC (MAX) + 1,000	ps	
	ODT turn-off (power-down mode)	^{t}AOFPD	^{t}AC (MIN) + 2,000	2.5 x ^{t}CK + ^{t}AC (MAX) + 1,000	ps	
	ODT to power-down entry latency	^{t}ANPD	3		^{t}CK	37
	ODT power-down exit latency	^{t}AXPD	10		^{t}CK	37
	ODT enable from MRS command	^{t}MOD	12		ns	37, 49
Power-Down	Exit active power-down to READ command, MR[12} = 0	^{t}XARD	2		^{t}CK	37
	Exit active power-down to READ command, MR[12]= 1	^{t}XARDS	8 - AL		^{t}CK	37
	Exit precharge power-down to any non-READ command.	^{t}XP	2		^{t}CK	37
	CKE MIN HIGH/LOW time	^{t}CKE	3		^{t}CK	32, 37

Notes

1. All voltages are referenced to V_{SS}.
2. Tests for AC timing, I_{DD}, and electrical AC and DC characteristics may be conducted at nominal reference/supply voltage levels, but the related specifications and device operation are guaranteed for the full voltage range specified. ODT is disabled for all measurements that are not ODT-specific.
3. Outputs measured with equivalent load:



4. AC timing and I_{DD} tests may use a V_{IL}-to-V_{IH} swing of up to 1.0V in the test environment and parameter specifications are guaranteed for the specified AC input levels under normal use conditions. The slew rate for the input signals used to test the device is 1.0 V/ns for signals in the range between $V_{IL(AC)}$ and $V_{IH(AC)}$. Slew rates other than 1.0 V/ns may require the timing parameters to be derated as specified.
5. The AC and DC input level specifications are as defined in the SSTL_18 standard (i.e., the receiver will effectively switch as a result of the signal crossing the AC input level and will remain in that state as long as the signal does not ring back above [below] the DC input LOW [HIGH] level).
6. There are two sets of values listed for Command/Address : ${}^{t}IS_a$, ${}^{t}IH_a$ and ${}^{t}IS_b$, ${}^{t}IH_b$. The ${}^{t}IS_a$, ${}^{t}IH_a$ values (for reference only) are equivalent to the baseline values of ${}^{t}IS_b$, ${}^{t}IH_b$ at V_{REF} when the slew rate is 1 V/ns. The baseline values, ${}^{t}IS_b$, ${}^{t}IH_b$, are the JEDEC-defined values, referenced from the logic trip points. ${}^{t}IS_b$ is referenced from $V_{IH(AC)}$ for a rising signal and $V_{IL(AC)}$ for a falling signal, while ${}^{t}IH_b$ is referenced from $V_{IL(DC)}$ for a rising signal and $V_{IH(DC)}$ for a falling signal. If the Command/Address slew rate is not equal to 1 V/ns, then the baseline values must be derated by adding the values from Tables 26 and Table 27.
7. The values listed are for the differential DQS strobe (DQS and DQS#) with a differential slew rate of 2 V/ns (1 V/ns for each signal). There are two sets of values listed: ${}^{t}DS_a$, ${}^{t}DH_a$ and ${}^{t}DS_b$, ${}^{t}DH_b$. The ${}^{t}DS_a$, ${}^{t}DH_a$ values (for reference only) are equivalent to the baseline values of ${}^{t}DS_b$, ${}^{t}DH_b$ at V_{REF} when the slew rate is 2 V/ns, differentially. The baseline values, ${}^{t}DS_b$, ${}^{t}DH_b$, are the JEDEC-defined values, referenced from the logic trip points. ${}^{t}DS_b$ is referenced from $V_{IH(AC)}$ for a rising signal and $V_{IL(AC)}$ for a falling signal, while ${}^{t}DH_b$ is referenced from $V_{IL(DC)}$ for a rising signal and $V_{IH(DC)}$ for a falling signal. If the differential DQS slew rate is not equal to 2 V/ns, then the baseline values must be derated by adding the values from Tables 28 and 29. If the DQS differential strobe feature is not enabled, then the DQS strobe is single-ended, the baseline values not applicable, and timing is not referenced to the logic trip points. Single-ended DQS data timing is referenced to DQS crossing V_{REF}. The correct timing values for a single-ended DQS strobe are listed in Tables 30– Table 33; listed values are already derated for slew rate variations and can be used directly from the table.
8. ${}^{t}HZ$ and ${}^{t}LZ$ transitions occur in the same access time windows as valid data transitions. These parameters are not referenced to a specific voltage level, but specify when the device output is no longer driving (${}^{t}HZ$) or begins driving (${}^{t}LZ$).
9. This maximum value is derived from the referenced test load. ${}^{t}HZ$ (MAX) will prevail over ${}^{t}DQSCK$ (MAX) + ${}^{t}RPST$ (MAX) condition.
10. ${}^{t}LZ$ (MIN) will prevail over a ${}^{t}DQSCK$ (MIN) + ${}^{t}RPRE$ (MAX) condition.

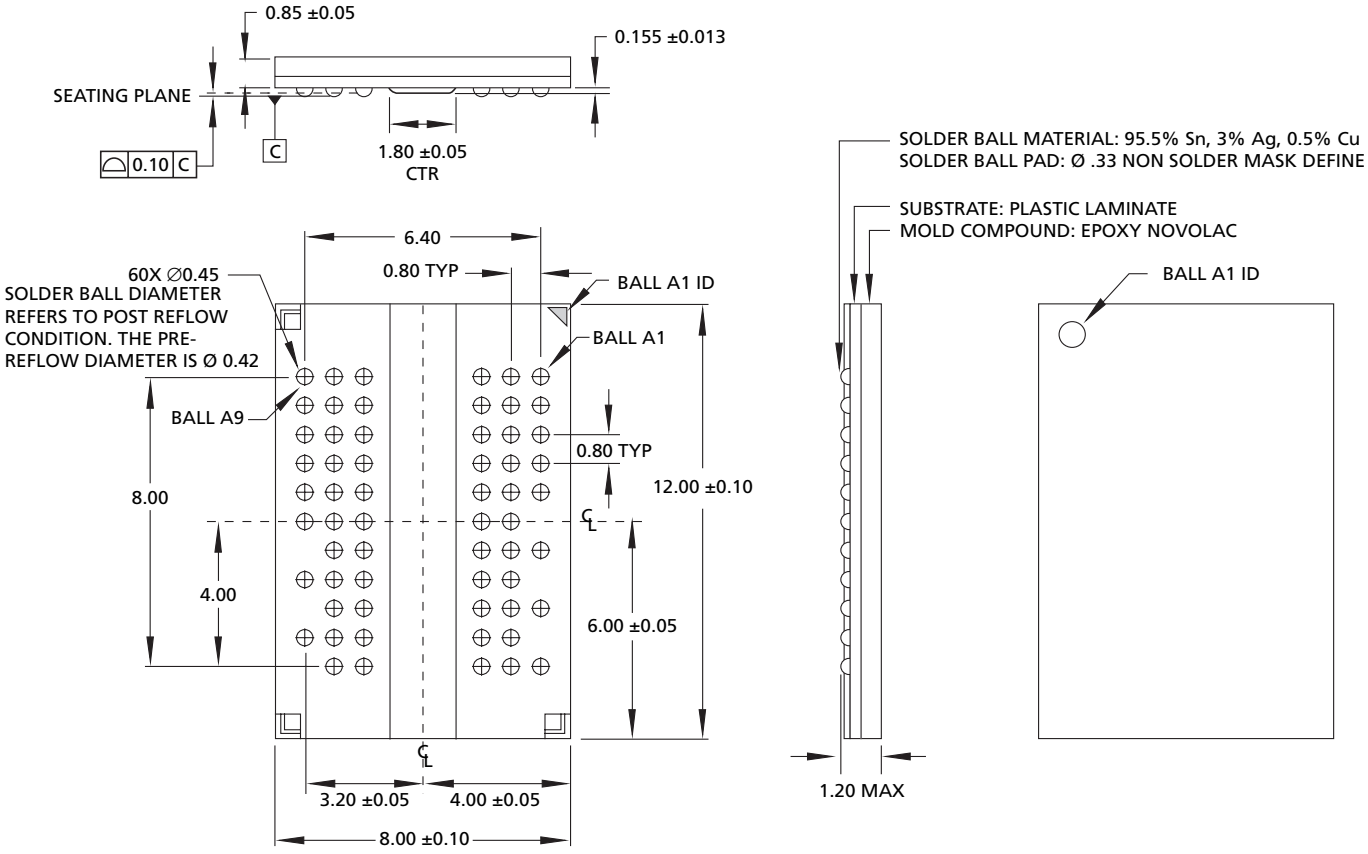
11. The intent of the "Don't Care" state after completion of the postamble is that the DQS-driven signal should either be HIGH, LOW or High-Z, and that any signal transition within the input switching region must follow valid input requirements. That is, if DQS transitions HIGH (above V_{IH}[DC] MIN), then it must not transition LOW (below V_{IH}[DC]) prior to ^{t}DQSH (MIN).
12. This is not a device limit. The device will operate with a negative value, but system performance could be degraded due to bus turnaround.
13. It is recommended that DQS be valid (HIGH or LOW) on or before the WRITE command. The case shown (DQS going from High-Z to logic LOW) applies when no WRITEs were previously in progress on the bus. If a previous WRITE was in progress, DQS could be HIGH during this time, depending on ^{t}DQSS.
14. The refresh period is 64ms (commercial) or 32ms (industrial). This equates to an average refresh rate of 7.8125µs (commercial) or 3.9607µs (industrial). However, a REFRESH command must be asserted at least once every 70.3µs or ^{t}RFC (MAX). To ensure all rows of all banks are properly refreshed, 8,192 REFRESH commands must be issued every 64ms (commercial) or 32ms (industrial).
15. Referenced to each output group: x4 = DQS with DQ0–DQ3; x8 = DQS with DQ0–DQ7; x16 = LDQS with DQ0–DQ7; and UDQS with DQ8–DQ15.
16. CK and CK# input slew rate is referenced at 1 V/ns (2 V/ns if measured differentially).
17. The data valid window is derived by achieving other specifications: ^{t}HP (^{t}CK/2), ^{t}DQSQ, and ^{t}QH (^{t}QH = ^{t}HP - ^{t}QHS). The data valid window derates in direct proportion to the clock duty cycle and a practical data valid window can be derived.
18. READs and WRITEs with auto precharge *are* allowed to be issued before ^{t}RAS (MIN) is satisfied since ^{t}RAS lockout feature is supported in DDR2 SDRAM.
19. V_{IL}/V_{IH} DDR2 overshoot/undershoot. See "AC Overshoot/Undershoot Specification" on page 24.
20. ^{t}DAL = (nWR) + (^{t}RP/^{t}CK). Each of these terms, if not already an integer, should be rounded up to the next integer. ^{t}CK refers to the application clock period; nWR refers to the ^{t}WR parameter stored in the MR[11,10,9]. For example, -37E at ^{t}CK = 3.75ns with ^{t}WR programmed to four clocks would have ^{t}DAL = 4 + (15ns/3.75ns) clocks = 4 + (4) clocks = 8 clocks.
21. The minimum internal READ to PRECHARGE time. This is the time from the last 4-bit prefetch begins to when the PRECHARGE command can be issued. A 4-bit prefetch is when the READ command internally latches the READ so that data will output CL later. This parameter is only applicable when ^{t}RTP / (2 x ^{t}CK) > 1, such as frequencies faster than 533 MHz when ^{t}RTP = 7.5ns. If ^{t}RTP / (2 x ^{t}CK) ≤ 1, then equation AL + BL/2 applies. ^{t}RAS (MIN) also has to be satisfied as well. The DDR2 SDRAM will automatically delay the internal PRECHARGE command until ^{t}RAS (MIN) has been satisfied.
22. Operating frequency is only allowed to change during self refresh mode (See "Self Refresh" on page 27), precharge power-down mode (See "Power-Down Mode" on page 30), and system reset condition (See "Reset Function" on page 7). SSC allows for small deviations in operating frequency, provided the SSC guidelines are satisfied.
23. ODT turn-on time ^{t}AON (MIN) is when the device leaves High-Z and ODT resistance begins to turn on. ODT turn-on time ^{t}AON (MAX) is when the ODT resistance is fully on. Both are measured from ^{t}AOND.
24. ODT turn-off time ^{t}AOF (MIN) is when the device starts to turn off ODT resistance. ODT turn off time ^{t}AOF (MAX) is when the bus is in High-Z. Both are measured from ^{t}AOFD.
25. This parameter has a two clock minimum requirement at any ^{t}CK.

26. ^{t}DELAY is calculated from ^{t}IS + ^{t}CK + ^{t}IH so that CKE registration LOW is guaranteed prior to CK, CK# being removed in a system RESET condition. See "Reset Function" on page 7.
27. ^{t}ISXR is equal to ^{t}IS and is used for CKE setup time during self refresh exit, as shown in Figure 66.
28. No more than four bank-ACTIVE commands may be issued in a given ^{t}FAW (MIN) period. ^{t}RRD (MIN) restriction still applies. The ^{t}FAW (MIN) parameter applies to all 8-bank DDR2 devices, regardless of the number of banks already open or closed.
29. ^{t}RPA timing applies when the PRECHARGE (ALL) command is issued, regardless of the number of banks already open or closed. If a single-bank PRECHARGE command is issued, ^{t}RP timing applies. ^{t}RPA (MIN) applies to all 8-bank DDR2 devices.
30. Value is minimum pulse width, not the number of clock registrations.
31. This is applicable to READ cycles only. WRITE cycles generally require additional time due to ^{t}WR during auto precharge.
32. ^{t}CKE (MIN) of three clocks means CKE must be registered on three consecutive positive clock edges. CKE must remain at the valid input level the entire time it takes to achieve the three clocks of registration. Thus, after any CKE transition, CKE may not transition from its valid level during the time period of ^{t}IS + 2 x ^{t}CK + ^{t}IH.
33. This parameter is not referenced to a specific voltage level, but specified when the device output is no longer driving (^{t}RPST) or beginning to drive (^{t}RPRE).
34. When DQS is used single-ended, the minimum limit is reduced by 100ps.
35. The half-clock of ^{t}AOFD's 2.5 ^{t}CK assumes a 50/50 clock duty cycle. This half-clock value must be derated by the amount of half-clock duty cycle error. For example, if the clock duty cycle was 47/53, ^{t}AOFD would actually be 2.5 - 0.03, or 2.47 for ^{t}AOF (MIN) and 2.5 + 0.03 or 2.53 for^{t}AOF (MAX).
36. The clock's $^{t}CK_{AVG}$ is the average clock over any 200 consecutive clocks and $^{t}CK_{AVG}$ (MIN) is the smallest clock rate allowed, except a deviation due to allowed clock jitter. Input clock jitter is allowed provided it does not exceed values specified. Also, the jitter must be of a random Gaussian distribution in nature.
37. The inputs to the DRAM must be aligned to the associated clock; that is, the actual clock that latches it in. However, the input timing (in ns) references to the $^{t}CK_{AVG}$ when determining the required number of clocks. The following input parameters are determined by taking the specified percentage times the $^{t}CK_{AVG}$ rather than ^{t}CK: ^{t}IPW, ^{t}DIPW, ^{t}DQSS, ^{t}DQSH, ^{t}DQSL, ^{t}DSS, ^{t}DSH, ^{t}WPST, and ^{t}WPRE.
38. Spread spectrum is not included in the jitter specification values. However, the input clock can accommodate spread spectrum at a sweep rate in the range 20–60 KHz with additional one percent of $^{t}CK_{AVG}$ as a long-term jitter component; however, the spread spectrum may not use a clock rate below $^{t}CK_{AVG(MIN)}$ or above $^{t}CK_{AVG(MAX)}$.
39. The period jitter ($^{t}JIT_{PER}$) is the maximum deviation in the clock period from the average or nominal clock allowed in either the positive or negative direction. JEDEC specifies tighter jitter numbers during DLL locking time. During DLL lock time, the jitter values should be 20 percent less than noted in the table (DLL locked).
40. The half-period jitter ($^{t}JIT_{DTY}$) applies to either the high pulse of clock or the low pulse of clock; however, the two cumulatively can not exceed $^{t}JIT_{PER}$.
41. The cycle-to-cycle jitter ($^{t}JIT_{CC}$) is the amount the clock period can deviate from one cycle to the following cycle. JEDEC specifies tighter jitter numbers during DLL locking time. During DLL lock time, the jitter values should be 20 percent less than noted in the table (DLL locked).

42. The cumulative jitter error ($^{t}ERR_{nPER}$), where n is 2, 3, 4, 5, 6–10, or 11–50, is the amount of clock time allowed to consecutively accumulate away from the average clock over any number of clock cycles.
43. The DRAM output timing is aligned to the nominal or average clock. Most output parameters must be derated by the actual jitter error when input clock jitter is present; this will result in each parameter becoming larger. The following parameters are required to be derated by subtracting $^{t}ERR_{5PER}$ (MAX): ^{t}AC (MIN), $^{t}DQSCK$ (MIN), $^{t}LZ_{DQS}$ (MIN), $^{t}LZ_{DQ}$ (MIN), ^{t}AON (MIN); while these following parameters are required to be derated by subtracting $^{t}ERR_{5PER}$ (MIN): ^{t}AC (MAX), $^{t}DQSCK$ (MAX), ^{t}HZ (MAX), $^{t}LZ_{DQS}$ (MAX), $^{t}LZ_{DQ}$ (MAX), ^{t}AON (MAX). The parameter $^{t}RPRE$ (MIN) is derated by subtracting $^{t}JIT_{PER}$ (MAX), while $^{t}RPRE$ (MAX), is derated by subtracting $^{t}JIT_{PER}$ (MIN). The parameter $^{t}RPST$ (MIN) is derated by subtracting $^{t}JIT_{DTY}$ (MAX), while $^{t}RPST$ (MAX), is derated by subtracting $^{t}JIT_{DTY}$ (MIN).
44. Half-clock output parameters must be derated by the actual $^{t}ERR_{5PER}$ and $^{t}JIT_{DTY}$ when input clock jitter is present; this will result in each parameter becoming larger. The parameter ^{t}AOF (MIN) is required to be derated by subtracting both $^{t}ERR_{5PER}$ (MAX) and $^{t}JIT_{DTY}$ (MAX). The parameter ^{t}AOF (MAX) is required to be derated by subtracting both $^{t}ERR_{5PER}$ (MIN) and $^{t}JIT_{DTY}$ (MIN).
45. MIN(^{t}CL, ^{t}CH) refers to the smaller of the actual clock LOW time and the actual clock HIGH time driven to the device. The clock's half period must also be of a Gaussian distribution; $^{t}CH_{AVG}$ and $^{t}CL_{AVG}$ must be met with or without clock jitter and with or without duty cycle jitter. $^{t}CH_{AVG}$ and $^{t}CL_{AVG}$ are the average of any 200 consecutive CK falling edges.
46. ^{t}HP (MIN) is the lesser of ^{t}CL and ^{t}CH actually applied to the device CK and CK# inputs; thus, ^{t}HP (MIN) ≥ the lesser of $^{t}CL_{ABS}$ (MIN) and $^{t}CH_{ABS}$ (MIN).
47. $^{t}QH = {}^{t}HP - {}^{t}QHS$; the worst case ^{t}QH would be the smaller of $^{t}CL_{ABS}$ (MAX) or $^{t}CH_{ABS}$ (MAX) times $^{t}CK_{ABS}$ (MIN) - ^{t}QHS. Minimizing the amount of $^{t}CH_{AVG}$ offset and value of $^{t}JIT_{DTY}$ will provide a larger ^{t}QH, which in turn will provide a larger valid data out window.
48. JEDEC specifies using $^{t}ERR_{6–10PER}$ when derating clock-related output timing (notes 43–44). Micron requires less derating by allowing $^{t}ERR_{5PER}$ to be used.
49. Requires 8 ^{t}CK for backward compatibility.

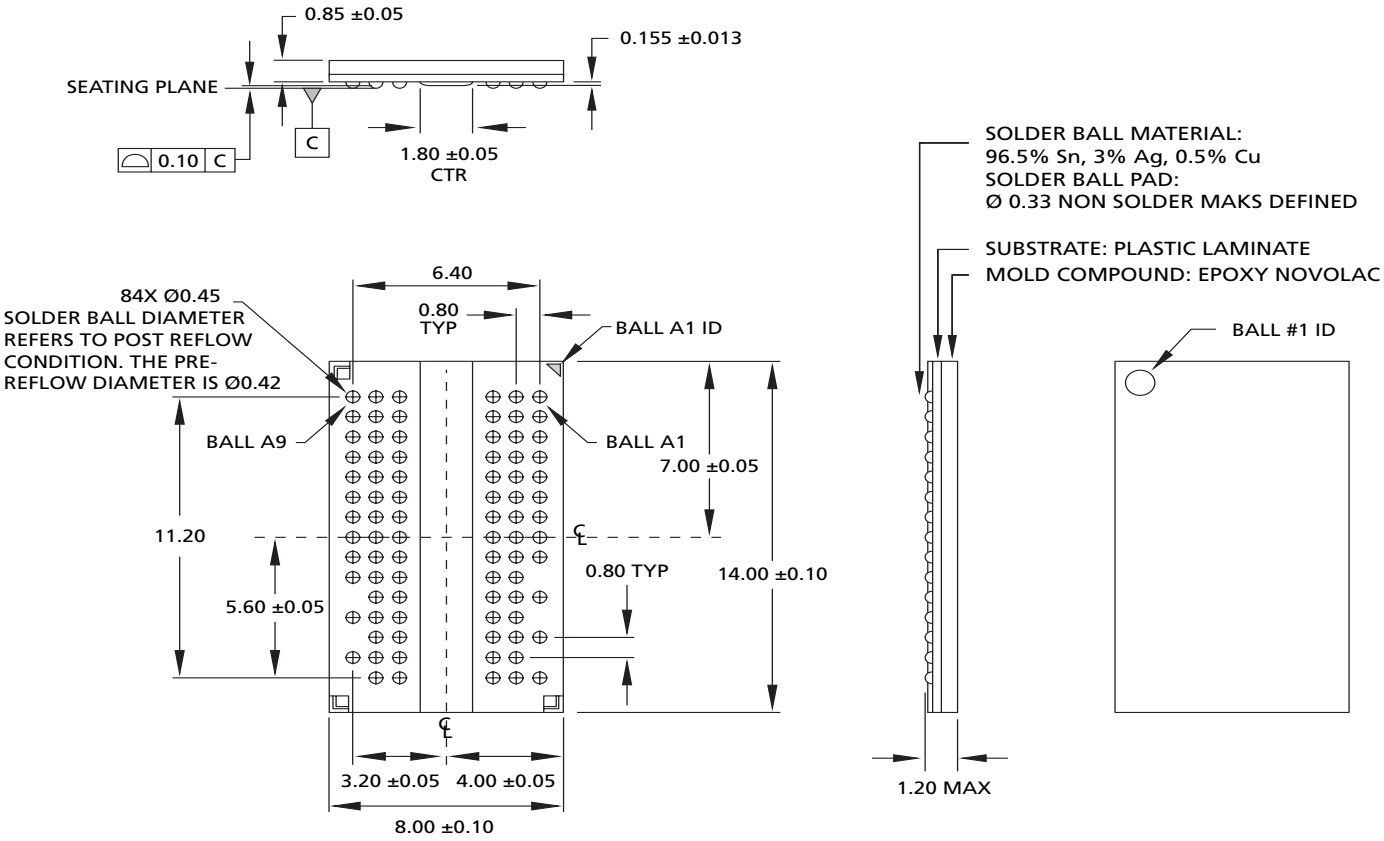
Package Dimensions

Figure 88: 60-Ball FBGA Package, 8mm x 12mm (x4, x8)



Note: All dimensions are in millimeters.

Figure 89: 84-Ball FBGA Package, 8mm x 14mm (x16)



Note: All dimensions are in millimeters.