MT8924

PCM Conference Circuit (PCC)

Preliminary Information

ISSUE 1 April 1994

Features

- Supports up to 10 independent conferences for up to 32 PCM Voice Channels
- ST-BUS compatible 2.048 Mb/s PCM Serial Interface (also supports 1.536 Mb/s and 1.544 Mb/s data rates)
- Per channel digital gain control (0/-3/-6 dB)
- Parallel microprocessor port for device control
- Programmable noise suppression
- External Tone Input
- Pin selectable A/µ-Law format
- Low power CMOS technology
- Available in 24 Pin PDIP and SOIC packages

Applications

- Digital PBX / KTS
- Conference bridges
- Digital C.O. switches

Ordering Information

MT8924AE	24 Pin Plastic DIP
MT8924AS	24 Pin SOIC

0°C to +70°C

Description

The MT8924 is designed to provide conference call capability in digital switching systems. It allows up to 10 independent conferences to be set for up to 32 PCM voice channels.

A/µ-Law companded data from the PCM input port is converted to linear format, processed by a dedicated arithmetic unit, re-converted to companded format and then sent to the PCM output port.The PCM output signal contains all the information of each channel connected in conference except its own.

Programmable attenuation and noise suppression are provided for channels connected in conference or transparent mode. Additionally, an input for an external tone is featured that can be used as a signal to indicate to connected parties that they are on a conference call.

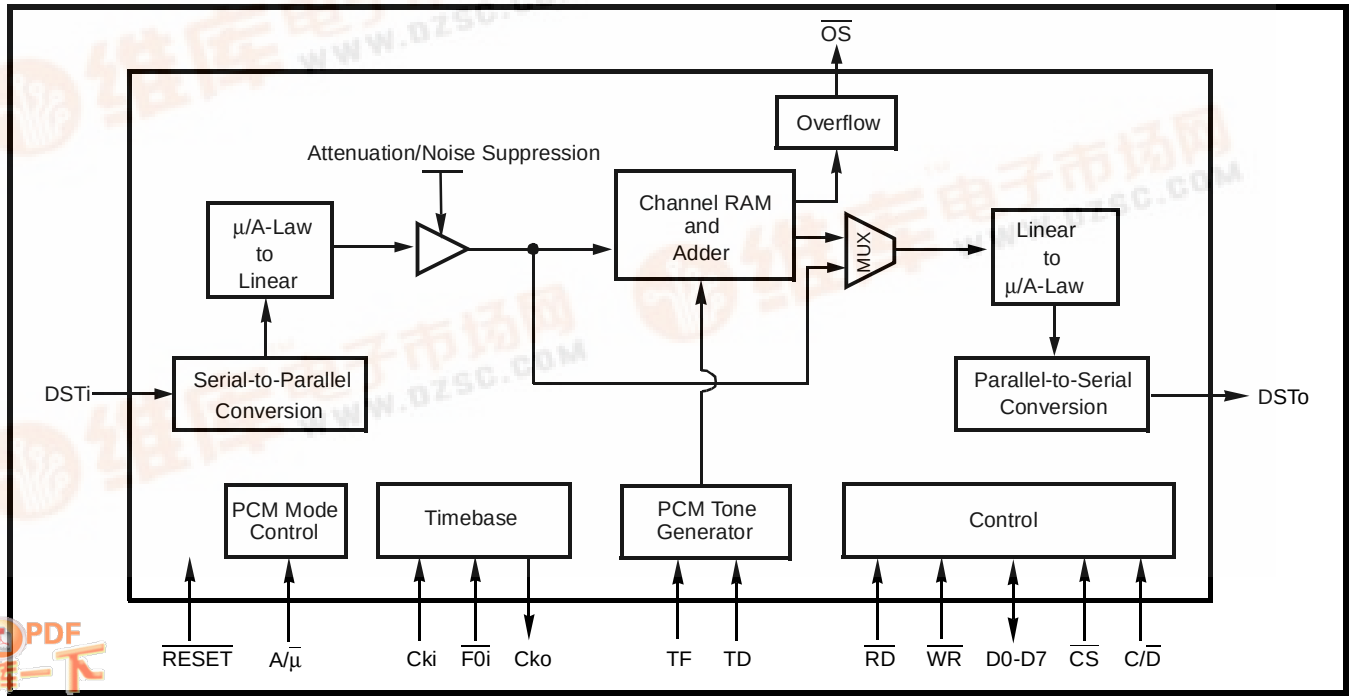

Figure 1 - Functional Block Diagram

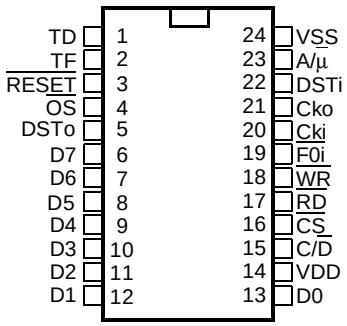

Figure 2 - Pin Connections

Pin Description

Pin #	Name	Description
1	TD	**Tone Duration (Input).** When TD is High, a PCM-coded tone is sent out to all channels of the enabled conferences instead of PCM data. TD is latched by frame pulse F0i so that all channels have the same tone during the same frame number. When TD is Low, normal operation is enabled.
2	TF	**Tone Frequency (Input).** This input is connected to an external squarewave generator. TF is strobed by frame pulse F0i so that all channels have the same tone frequency during the same number of frames. The PCM-coded tone level corresponds to 1/10th of the full scale value, and is activated when TD is High.
3	$\overline{\text{RESET}}$	**Master RESET (Input).** This input is used for system initialization after power up, or when the companding law format has been changed. The $\overline{\text{RESET}}$ pin is strobed by the rising edge of clock Cki. Complete circuit initialization takes two frame periods. Initialization disables the output drivers of the microprocessor interface and DSTo.
4	$\overline{\text{OS}}$	**Overflow Signalling (Output).** When $\overline{\text{OS}}$ is Low, a conference is in the overflow condition. This signal is delayed by half of a timeslot relative to the beginning of the output channel of the conference in overflow (see Figure 9).
5	DST_o	**ST-BUS Serial Output.** This pin is the output for the PCM signal. It is enabled upon channel selection, otherwise it is placed in a high impedance state. Maximum bit rate is 2.048 Mb/s.
6-13	D7 to D0	**Data Bus I/O Port.** These are bidirectional data pins over which data and instructions are transferred to and from the microprocessor (where D0 is the least significant bit). The bus is in a high impedance state when $\overline{\text{RESET}}$ is Low and/or $\overline{\text{CS}}$ is High.
14	V_{DD}	**Positive Supply Voltage.** Nominally 5 volts.
15	C/$\overline{\text{D}}$	**Control/Data Select (Input).** The signal on this input defines whether the information on the data bus should be interpreted as opcode or data. During a write operation a Low signal defines the bus content as data, while a High signal defines it as opcode. During a read operation this input differentiates overflow status between the first eight channels for C/D being LOW, and the last two channels for C/D being HIGH (see Instruction 4). This input also allows status monitoring (see Instruction 6) during a read operation.
16	$\overline{\text{CS}}$	**Chip Select (Input).** This active low input selects the device for microprocessor read/write operations. When $\overline{\text{CS}}$ is Low, data and instructions can be transferred to or from the microprocessor, and when $\overline{\text{CS}}$ is High, the data bus is in a high impedance state.
17	$\overline{\text{RD}}$	**Read (Input).** This active low input is for the read signal on the microprocessor interface. The data bus is updated on the falling edge of $\overline{\text{RD}}$.
18	$\overline{\text{WR}}$	**Write Input.** This active low input is for the write signal on the microprocessor interface. The data bus is strobed on the rising edge of $\overline{\text{WR}}$.

Pin Description (continued)

Pin #	Name	Description
19	$\overline{F0i}$	**Frame Pulse (Input).** This is an 8 kHz active low input used for frame synchronization of the PCM bit stream. The first falling edge of Cki following the falling edge of frame pulse $\overline{F0i}$ determines the start of a new frame and must correspond to the first bit of the first channel. When PCM frames of 1544 kbit/s are used, the rising edge of $\overline{F0i}$ must correspond to the Extra (193rd) bit.
20	Cki	**Clock (Input).** This signal is the timing reference used for all internal operations. The PCM bit cell boundaries lie on the alternate falling edges of this clock. The maximum allowable clock frequency is 4096 kHz.
21	Cko	**Clock (Output).** This pin provides the master clock for a digital crosspoint switch (e.g., MT898x series, or the MT9080, MT9085 combination). Normally the signal on this pin is identical to Cki. When Extra bit operating mode is selected (see Instruction 5), the first two cycles of the master clock are suppressed (see Figure 10). This feature allows the MT8924 to operate in 1544 kbit/s systems.
22	DST_i	**ST-BUS Serial Input.** This pin accepts the serial PCM input stream at a maximum allowable bit rate of 2048 kbit/s. In normal operation the first bit of the first channel is defined by the rising edge of Cki following the falling edge of frame pulse $\overline{F0i}$. When Extra bit operating mode is selected, the first bit of the first channel defines the extra bit.
23	A/$\overline{\mu}$	**A/$\overline{\mu}$ - Law Select Input.** When A/$\overline{\mu}$ is High, A-Law is selected, and when A/$\overline{\mu}$ is Low, μ-Law is selected. The companding law selection must be done before initializing the device using the $\overline{RESET}$ pin.
24	V_{SS}	**Negative Power Supply Voltage.** Nominally 0 Volts.

Functional Description

The MT8924 is a device designed to provide conferencing in a digital switching system in any combination for up to all 32 channels of a 2048 kbit/s ST-BUS stream (see Figure 3).

The information of channel N, frame M is first converted to Linear PCM and then added to the signal from other conferencees during the first half of channel N+1, frame M and subtracted during the second half of channel N-1, frame M+1. After Linear-to-PCM conversion the subtraction result goes to the parallel-to-serial converter, and appears at the output on the N+1 channel, M+1 frame with respect to the corresponding sending party information (see Figure 4).

To a microprocessor the MT8924 appears as a memory mapped peripheral device that can be controlled by a set of six instructions. These commands can be used to establish or cancel conferences between the PCM channels and also to transmit control messages on specific operating modes. The microprocessor can initiate and receive status messages or check conference connections that are currently in operation.

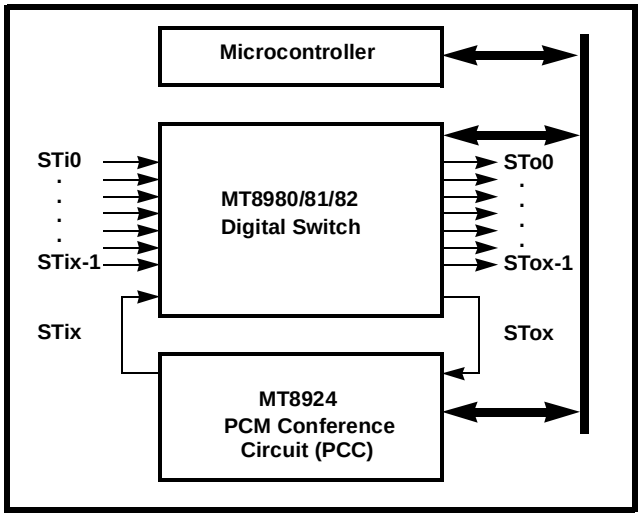

Figure 3 -Typical Conference Connection

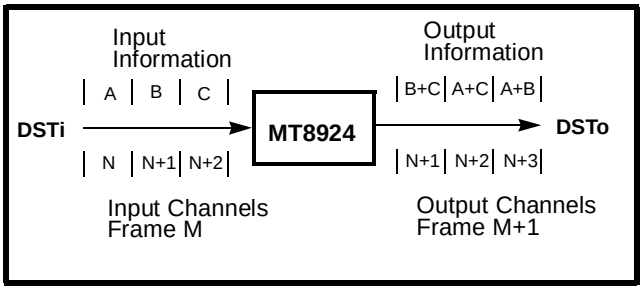

Figure 4 - Input/Output Channel Relationship

	Noise Threshold	PCM Byte	
		+ve input	-ve input
		B7 - B0	B7 - B0
A-Law	1/4096	1000 0000	0000 0000
	9/4096	1000 0100	0000 0100
	16/4096	1000 1000	0000 1000
	32/4096	1000 1111	0000 1111
μ-Law	1/8159	1111 1111	0111 1111
	9/8159	1111 1011	0111 1011
	16/8159	1111 0111	0111 0111
	32/8159	1111 0000	0111 0000

Table 1 - PCM Noise Suppression Threshold Levels

Overflow Detection / Input Channel Attenuation

If the sum of the channels involved in one conference exceeds the full scale value of the accumulator, an overflow condition is generated which can be monitored specifically by reading the status of the overflow register. If an overflow condition occurs, then each channel in a conference can be independently attenuated if desired.

Alternatively, a conference in the overflow condition can be detected using the $\overline{OS}$ signal in conjunction with frame pulse $\overline{F0i}$. $\overline{OS}$ will be low during the second half of a general output channel slot time N, if channel N belongs to a conference in overflow (see Figure 11). This information can be used to control input channel attenuation through software control.

F1	F0		B7	B6	B5	B4	B3	B2	B1	B0	Comments
0	0	+ Full Scale	1	1	1	1	1	1	1	1	No Inversion
		+ 0 Level	1	0	0	0	0	0	0	0	
		- 0 Level	0	0	0	0	0	0	0	0	
		- Full Scale	0	1	1	1	1	1	1	1	
0	1	+ Full Scale	1	0	1	0	1	0	1	0	Even Bit Inversion
		+ 0 Level	1	1	0	1	0	1	0	1	
		- 0 Level	0	1	0	1	0	1	0	1	
		- Full Scale	0	0	1	0	1	0	1	0	
1	0	+ Full Scale	1	1	0	1	0	1	0	1	Odd Bit Inversion
		+ 0 Level	1	0	1	0	1	0	1	0	
		- 0 Level	0	0	1	0	1	0	1	0	
		- Full Scale	0	1	0	1	0	1	0	1	
1	1	+ Full Scale	1	0	0	0	0	0	0	0	Bit Inversion
		+ 0 Level	1	1	1	1	1	1	1	1	
		- 0 Level	0	1	1	1	1	1	1	1	
		- Full Scale	0	0	0	0	0	0	0	0	

Table 2 - PCM Byte Format

B7 (sign bit) is the MSB and B0 is the LSB
F1-F0 corresponds to the D5-D4 bits of the control byte of Operating Mode Instruction 5

Noise Suppression

When noise suppression is enabled for a specific input channel then the PCM bytes for this channel, when below the selected threshold level, are converted to PCM bytes corresponding to the minimum PCM code level before being added to the conference sum.

The four threshold levels available correspond to the first, fifth, ninth and sixteenth step of the first segment. These are 1/4096, 9/4096, 16/4096, and 32/4096 with respect to full scale A-Law, and 1/8159, 9/8159, 16/8159, and 32/8159 with respect to full scale μ-Law (see Table 1).

PCM Format Selection

PCM digital code assignment is register programmable and achieved through the use of Instruction 5 (see Table 2). The available formats are CCITT G.711 A-Law or μ-Law, with true-sign Alternate Digit Inversion or true-sign/Inverted Magnitude coding.

Output clock Cko provides a reference time base for a digital time/space crosspoint switch. Normally this signal is identical to the master clock input Cki. When operating with the extra bit selection, through Instruction 5, Cko is low for two clock periods, which allows operation of the MT8924 with the 1.544 MHz PCM frame format (see Figure 10).

Transparent Mode

The MT8924 can operate in transparent mode. In this case the PCM input (DSTi) is passed unmodified through the MT8924 to the output (DSTo) with a delay of one frame and one channel. This feature allows attenuation of specific channels that are not connected to a conference.

Tone Insertion

The MT8924 provides for tone insertion into PCM output channels by using the two input pins TD and TF. An externally generated square wave tone applied to the TF input will generate a level corresponding to 1/10 of the full scale accumulator value when TD is High. Only channels connected in a conference with the insertion tone bit (IT) active will have the PCM coded tone at their output (see Instruction 1).

Testing and Diagnostic Feature

For testing and diagnostic purposes, a status instruction has been provided that indicates conference location and attenuation level for each channel requested. This data appears on the databus upon status request.

Programmable Control

Instruction 1 : Conference Mode Connection

This function connects a PCM channel to a conference. The control information from the microprocessor consists of two data bytes and one control byte. The first byte contains the conference number (bits D0-D3) and the Start bit S (D4). When S is High, the accumulator registers connected to a conference are initialized. S set to High is only required in Instruction 1 of the first channel connected to a new conference, otherwise S is set LOW to bring other channels into the conference. The second byte contains the number of the channel to be connected (D0-D4), and the Insert Tone Enable bit IT (D5). When IT and TD are both High all the channels belonging to that conference are enabled using the insert tone function. The third byte contains a four bit opcode (D0-D3) plus information about the attenuation level and noise suppression to be applied to the specific channel.

Instruction 2 : Transparent Mode Connection

This function sets up a PCM channel for transparent mode operation. The control information from the microprocessor consists of one data byte and one control byte.

The first byte contains the channel number, and the second byte contains a four bit opcode (D0-D3) and information about attenuation and noise suppression levels to be applied to the specific channel. PCM data on this channel is not added to any conference, but is transferred to the PCM output after a full frame pulse plus one channel delay. It is not affected by the tone control pins (TF, TD).

Instruction 3 : Disconnection

This function disconnects a PCM channel from a conference. The control information from the microprocessor consists of one data byte and one

control byte. The data byte contains the number of the channel to be disconnected. The second byte contains the opcode (D0-D3). One frame pulse must pass between disconnection and reconnection of the same channel.

Instruction 4 : Overflow Status Monitoring

This function extracts overflow status information on all existing conferences and transfers it to the microprocessor data bus. This instruction consists of two control bytes which are differentiated by the C/$\overline{D}$ control signal. C/$\overline{D}$ set Low reads the status of the first eight conferences, while C/$\overline{D}$ set High reads the status of the remaining two conferences. A conference is in overflow when the corresponding status bit is high.

Instruction 5 : PCM Mode Select

This function is used to set the PCM format. The control byte from the microprocessor consists of one data byte. It contains the Extra Bit E (D6), the Format Bits F1-F0 (D5, D4), and the opcode (D0-D3). The E bit must be high when the PCM frame contains an extra bit (i.e. 1.544 Mb/s). Normally E is Low. Bits F1-F0 are used to select the PCM byte format, according to Table 2. After $\overline{\text{RESET}}$ the default values correspond to F1 at Low and F0 at High if A-Law is selected, and F1 at High and F0 at High if μ-Law is selected. All channels must be disconnected when the PCM mode select instruction is sent. They must remain disconnected for at least two frame pulses after the instruction is sent. It is recommended that this instruction be used immediately following a system reset (see $\overline{\text{RESET}}$ pin description).

Instruction 6 : Status Monitoring

This function is a read operation which consists of a data byte, a control byte, and a status byte. It extracts information for test and diagnostic purposes and transfers it to the microprocessor bus. The first byte contains the channel number, while the second byte contains the opcode (D0-D3). The third byte contains the status information about the operating mode of the channel (D4-D7); the attenuation level (D2-D3); and the noise suppression level (D0-D1).

Instruction 1 : Channel Connection in Conference Mode

Control Signals				Data Bus								Comments
$\overline{CS}$	$\overline{RD}$	C/$\overline{D}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	
0	1	0	0	X	X	X	S	P3	P2	P1	P0	Conference Number
0	1	0	0	X	X	IT	C4	C3	C2	C1	C0	PCM Channel Number and Insertion Tone control
0	1	1	0	A1	A0	T1	T0	0	1	1	1	Opcode, Attenuation, and Noise Suppression control

S: Conference Start Bit
P3-P0: Conference Number (1-10)
IT: Insertion Tone Function Enable (IT=1)
C4-C0: Channel Number (0-31)
A1-A0: Channel Attenuation
00 = -0dB
01 = -3dB
10 = -6dB

T1-T0: Channel Noise Suppression

T1/T0	A-Law	μ-Law
00	no noise suppression	
01	9/4096	9/8159
10	16/4096	16/8159
11	32/4096	32/8159

Instruction 2 : Channel Connection in Transparent Mode

Control Signals				Data Bus								Comments
$\overline{CS}$	$\overline{RD}$	C/$\overline{D}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	
0	1	0	0	X	X	X	C4	C3	C2	C1	C0	PCM Channel Number
0	1	1	0	A1	A0	T1	T0	0	0	1	1	Opcode and Attenuation

T1-T0: see noise suppression description given for Instruction 1

Instruction 3 : Channel Disconnection

Control Signals				Data Bus								Comments
$\overline{CS}$	$\overline{RD}$	C/$\overline{D}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	
0	1	0	0	X	X	X	C4	C3	C2	C1	C0	PCM Channel Number
0	1	1	0	X	X	X	X	1	1	1	1	Opcode

Instruction 4: Overflow Status Monitoring

Control Signals				Data Bus								Comments
$\overline{CS}$	$\overline{RD}$	C/$\overline{D}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	
0	0	0	1	CF 8	CF 7	CF 6	CF 5	CF 4	CF 3	CF 2	CF 1	Conferences 1 to 8
0	0	1	1	X	X	X	X	X	X	CF 10	CF 9	Conferences 9 to 10

CF10 - CF1 : Conference is in overflow when bit is HIGH
Note : as long as $\overline{RD}$ remains LOW, the overflow status of the conference selected by C/$\overline{D}$ can be monitored in real time

Instruction 5 : PCM Operating Mode Selection

Control Signals				Data Bus								Comments
$\overline{CS}$	$\overline{RD}$	C/$\overline{D}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	
0	1	1	0	X	E	F1	F0	0	1	0	1	see Table 1

E: Extra bit insertion (active when E=1)
F1 - F0: PCM byte format selection (see Table 1)
00 = no bit inverted
01 = even bit (B0, B2, B4, B6) inverted
10 = odd bit (B1, B3, B5) inverted
11 = all bits (B0, B1, B2, B3, B4, B5, B6) inverted

Instruction 6 : Status Monitoring

Control Signals				Data Bus								Comments
$\overline{CS}$	$\overline{RD}$	C/$\overline{D}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	
0	1	0	0	X	X	X	C4	C3	C2	C1	C0	
0	1	1	0	X	X	X	X	0	1	1	0	
0	0	1	1	P3	P2	P1	P0	A1	A0	T1	T0	

P3 - P0: channel mode operation information
0000 = no connection
1111 = transparent mode
1010 - 0001 = conference mode
P3 - P0 provides conference number

A1 - A0: see channel attenuation description for Instruction 1

T1 - T0: see noise suppression description for Instruction 1

Note: Instruction 6 enables the data bus to read the status until reset by C/$\overline{D}$=0, $\overline{WR}$=1, and $\overline{CS}$=0

Absolute Maximum Ratings*

	Parameter	Symbol	Min	Max	Units
1	Supply Voltage	V_{DD} - V_{SS}	- 0.3	7	V
2	Voltage on any I/O pin	$V_{I/O}$	V_{SS} - 0.3	V_{DD} + 0.3	V
3	Current on any I/O pin	$I_{I/O}$		± 10	mA
4	Storage Temperature	T_{ST}	- 65	+ 150	°C
5	Power Dissipation (plastic package)	P_D		500	mW

* Exceeding these figures may cause permanent damage. Functional operation under these conditions is not guaranteed.

Recommended Operating Conditions

	Characteristics	Sym	Min	Typ*	Max	Units	Test Conditions
1	Supply Voltage	V_{DD}	4.75	5	5.25	V	
2	Ambient Operating Temp. Range	T_{OP}	0		+70	°C	
3	Input Voltage High	V_{IH}	2.4		V_{DD}	V	for 400mv noise margin
4	Input Voltage Low	V_{IL}	V_{SS}		0.8	V	

* Typical figures are at 25°C and are for design aid only; not guaranteed and not subject to production testing.

DC Characteristics: Clocked operation (T_{OP}=0 to 70°C; V_{DD}=5V±5%)

	Characteristics	Sym	Min	Typ	Max	Units	Test Conditions
1	Input Low Level	V_{IL}			0.8	V	Pins 1-3, 6-13, 15-20, 22-23
2	Input High Level	V_{IH}	2.0			V	Pins 1-3, 6-13, 15-20, 22-23
3	Output Low Level	V_{OL}			0.4	V	Pins 4, 6-13; I_{OL}=4 mA
4	Output High Level	V_{OH}	2.4			V	Pins 4, 6-13; I_{OL}=4 mA
5	Output Low Level	V_{OL}			0.4	V	Pins 5, 21; I_{OL}=8 mA
6	Input Leakage Current	I_{IL}			10	µA	Pins 1-3, 6-13, 15-20, 22-23; V_{IN}=0 to V_{DD}
7	Data Bus Leakage Current	I_{OL}			±10	µA	Pins 6-13; V_{IN}=0 to V_{DD}; $\overline{CS}$=V_{DD}
8	Supply Current	I_{DD}			10	mA	Pin 14; Cki=4.096 MHz

All DC characterisitics are valid 250µs after V_{DD} and C4i have been applied.

AC Electrical Characteristics - Capacitances

	Characteristics	Sym	Min	Typ	Max	Units	Test Conditions
1	Input Capacitance	C_I			5	pF	frequency=1MHz; T_{OP}=0 to 70°C; unused pins tied to V_{SS}; V_{DD}=5V±5%
2	I/O Capacitance (Bidirectional)	$C_{I/O}$			15	pF	
3	Output Capacitance	C_O			10	pF	

AC Electrical Characteristics - Clocked Timing* (T_{OP}=0 to 70°C; V_{DD}=5V±5%)

	Characteristics	Sym	Min	Typ	Max	Units	Test Conditions
1	Clock period	t_{CK}	230			ns	
2	Clock low level width	t_{WLCK}	100			ns	
3	Clock high level width	t_{WHCK}	100			ns	
4	Clock rise time	t_{RCK}			25	ns	
5	Clock fall time	t_{FCK}			25	ns	
6	Sync. low setup time	t_{SLSY}	50			ns	**
7	Sync. low level hold time	t_{HLSY}	40			ns	
8	Sync. high setup time	t_{SHSY}	80			ns	
9	Sync. high width	t_{WHSY}	t_{CK}			ns	
10	$\overline{OS}$ propagation delay from rising edge of Clock	t_{PDOS}			100	ns	C_L=50pF
11	Cko propagation delay to Clock edges	t_{PDEC}			80	ns	C_L=50pF
12	TD setup time	t_{STD}	80			ns	
13	TD hold time	t_{HTD}	40			ns	
14	TD setup time	t_{STF}	80			ns	
15	TD hold time	t_{HTD}	40			ns	

* All AC characteristics are valid 250µs after V_{DD} and the clock have been applied. C_L is the max. capacitive load and R_L is the test pull up resistor. With Extra Bit Insert operating mode these times are 80ns longer.

** With Extra Bit Insert operating mode this time becomes $3t_{CK}$.

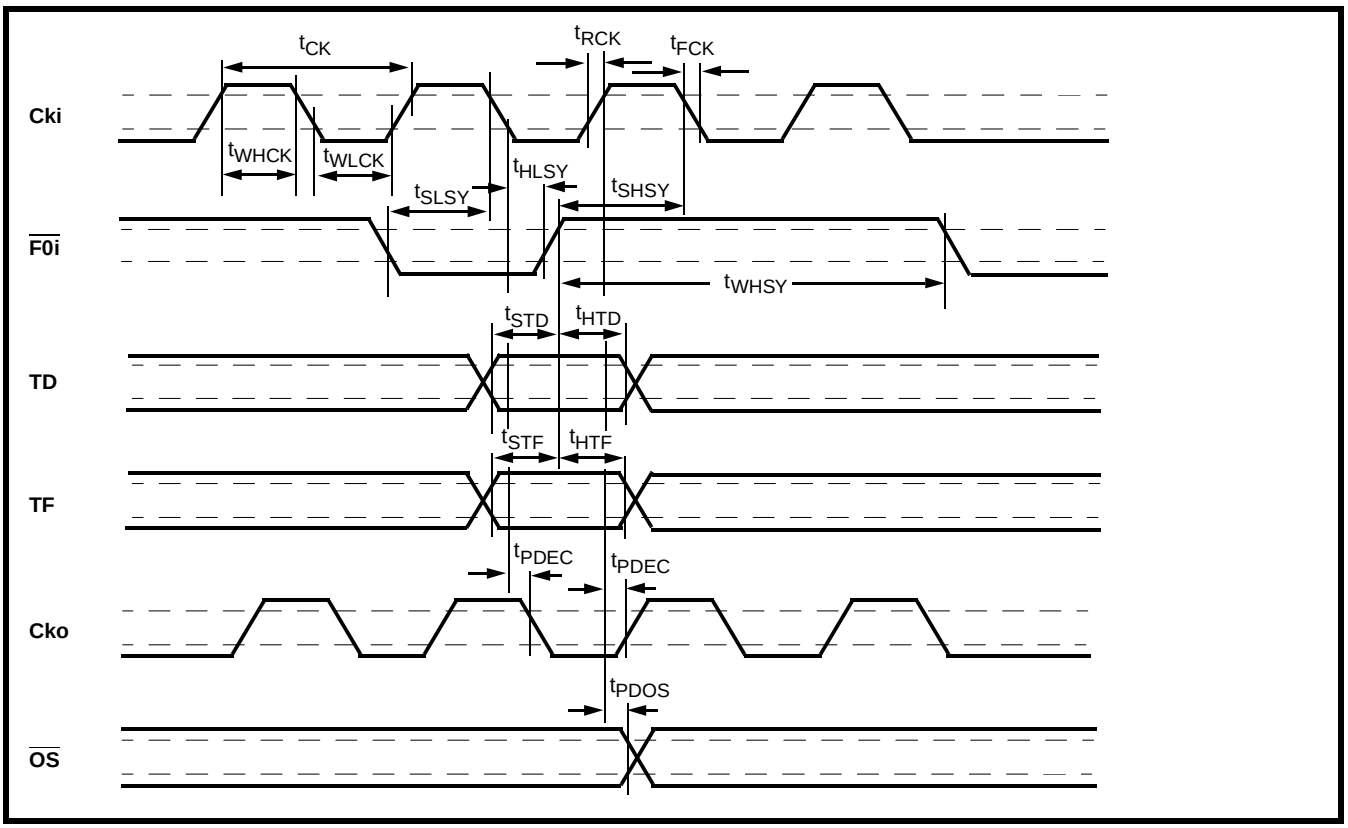

Figure 5 - Clock Timing

AC Electrical Characteristics - PCM Timing* (T_{OP}=0 to 70°C; V_{DD}=5V±5%)

	Characteristics	Sym	Min	Typ	Max	Units	Test Conditions
1	Input PCM setup time	t_{SPCM}	80			ns	
2	Input PCM hold time	t_{HPCM}	35			ns	
3	Output PCM propagation delay	t_{PD}	25		125	ns	C_L=150pF, R_L=1KΩ in 2.048MHz mode **

*All AC characteristics are valid 250µs after V_{DD} and the clock have been applied. C_L is the max. capacitive load and R_L is the test pull up resistor.

**With Extra Bit Insert operating mode these times are 80ns longer.

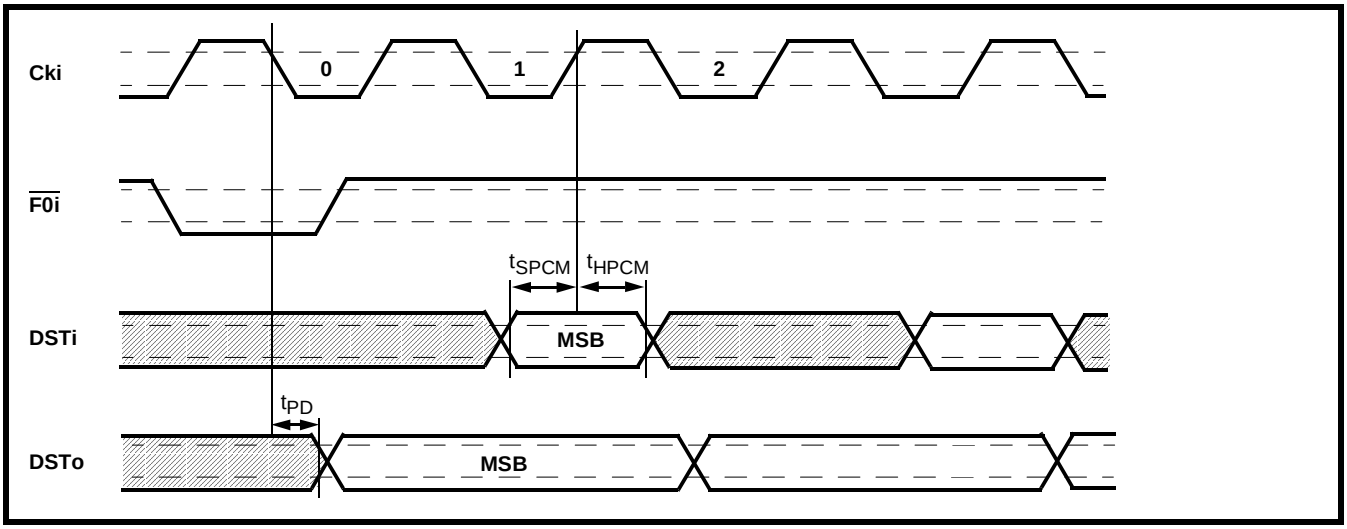

Figure 6 - PCM Timing

AC Electrical Characteristics - RESET Timing* (T_{OP}=0 to 70°C; V_{DD}=5V±5%)

	Characteristics	Sym	Min	Typ	Max	Units	Test Conditions
1	$\overline{\text{RESET}}$ low setup time	t_{SLRES}	100			ns	
2	$\overline{\text{RESET}}$ low hold time	t_{HLRES}	50			ns	
3	$\overline{\text{RESET}}$ high setup time	t_{SHRES}	90			ns	
4	$\overline{\text{RESET}}$ high level width	t_{WHRES}	t_{CK}			ns	

* All AC characteristics are valid 250µs after V_{DD} and the clock have been applied. C_L is the max. capacitive load and R_L is the test pull up resistor.

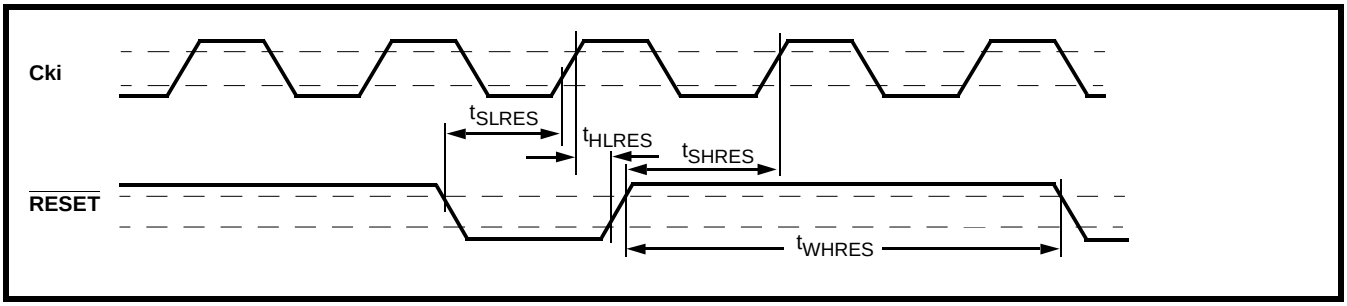

Figure 7 - Reset Timing

AC Electrical Characteristics - Write Timing (T_{OP}=0 to 70°C; V_{DD}=5V±5%)

	Characteristics	Sym	Min	Typ	Max	Units	Test Conditions
1	Write Pulse low width	t_{WLWR}	150			ns	
2	Write Pulse high width	t_{WHWR}	200			ns	
3	Repetition Interval between active Write Pulses	t_{REPWR}	500			ns	
4	Read high setup time to active Write Pulse	t_{SHRD}	0			ns	
5	Read high hold time from active Write Pulse	t_{HHRD}	20			ns	
6	Write Pulse rise time	t_{RWR}	60			ns	
7	Write Pulse fall time	t_{FWR}	60			ns	
8	$\overline{CS}$ low setup time to $\overline{WR}$ falling edge	t_{SLCSWR}	0			ns	Active case
9	$\overline{CS}$ low hold time from $\overline{WR}$ falling edge	t_{HLCSWR}	0			ns	Active case
10	$\overline{CS}$ high setup time to $\overline{WR}$ rising edge	t_{SHCSWR}	0			ns	
11	$\overline{CS}$ high hold time from $\overline{WR}$ rising edge	t_{HHCSWR}	0			ns	
12	C/$\overline{D}$ setup time to Write Pulse end	$t_{SC/DWR}$	130			ns	
13	C/$\overline{D}$ hold time from Write Pulse end	t_{HCDWR}	25			ns	
14	Input setup time to Write Pulse end	t_{SDWR}	130			ns	
15	Input hold time from Bus Write Pulse end	t_{HDWR}	25			ns	

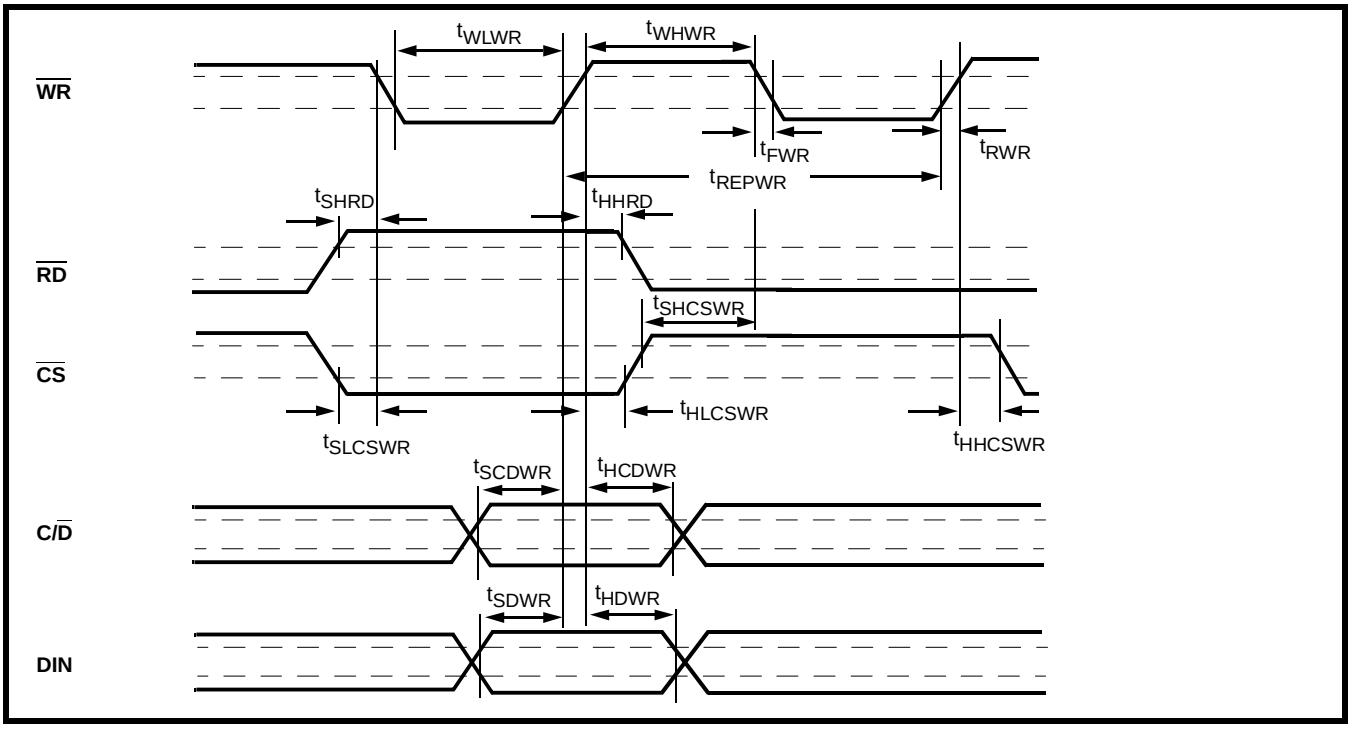

Figure 8 - Write Timing Characteristics

AC Electrical Characteristics - Read Timing (T_{OP}=0 to 70°C; V_{DD}=5V±5%)

	Characteristics	Sym	Min	Typ	Max	Units	Test Conditions
1	Read Pulse low width	t_{WLRD}	180			ns	
2	Read Pulse high width	t_{WHRD}	200			ns	
3	Repetition Interval between active Read Pulses	t_{REPRD}	500			ns	
4	Write high setup time to active Read Pulse	t_{SHWR}	0			ns	
5	Write high hold time from active Read Pulse	t_{HHWR}	20			ns	
6	Read Pulse rise time	t_{RRD}			60	ns	
7	Read Pulse fall time	t_{FRD}			60	ns	
8	Low setup time to $\overline{RD}$ falling edge	t_{SLCSRD}	0			ns	Active case
9	Low hold time from $\overline{RD}$ falling edge	t_{HLCSRD}	0			ns	Active case
10	High setup time to $\overline{RD}$ falling edge	t_{SHCSRD}	0			ns	Active case
11	High hold time from $\overline{RD}$ rising edge	t_{HHCSRD}	0			ns	Active case
12	C/$\overline{D}$ setup time to $\overline{RD}$ Pulse start	t_{SCDRD}	20			ns	
13	Hold time from Read Pulse end	t_{HCDRD}	25			ns	
14	Propagation delay from falling edge of Read Pulse	t_{PDD}			120	ns	Read; C_L=200pF
15	Propagation delay from rising edge of Read Pulse to high impedance state	t_{HZ}			80	ns	Write; C_L=200pF

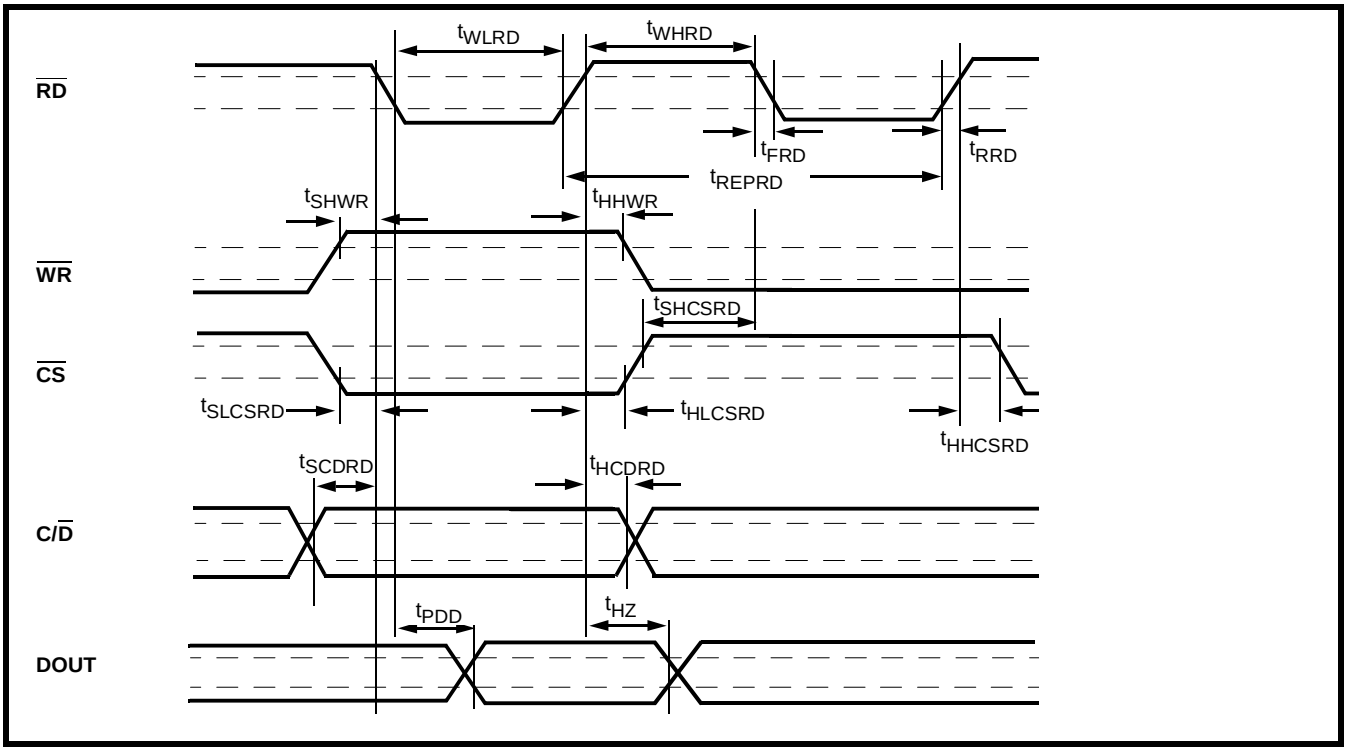

Figure 9 - Read Timing Characteristics

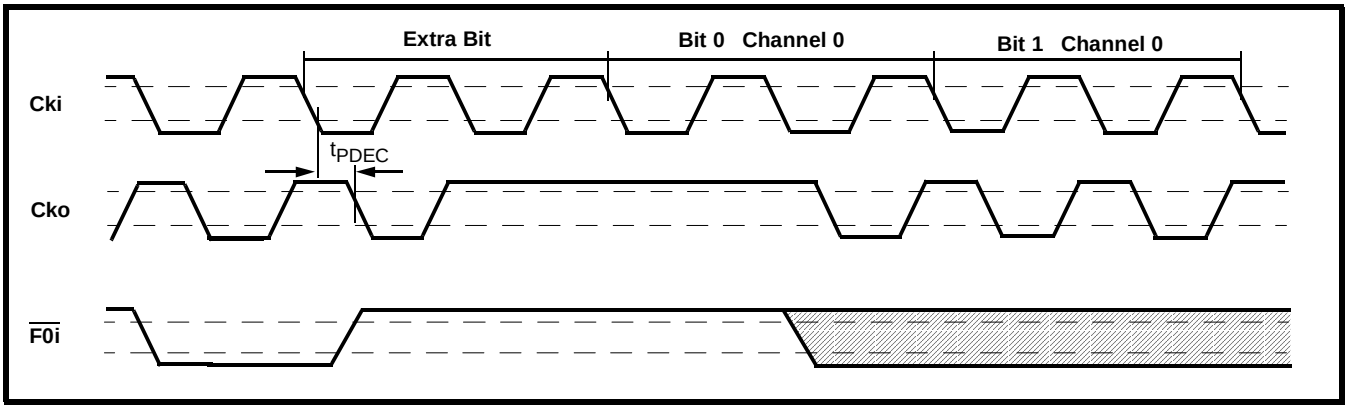

Figure 10 - CKo Timing with Extra Bit Insertion Mode

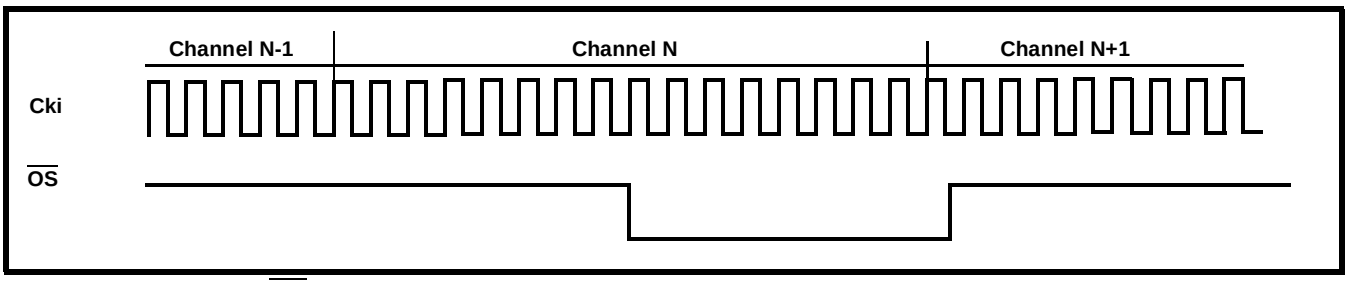

Figure 11 - $\overline{OS}$ Timing with Output PCM Channel belonging to a Conference in Overflow