PRELIMINARY‡

1/2-INCH 3-MEGAPIXEL CMOS ACTIVE-PIXEL DIGITAL IMAGE SENSOR

PART NUMBER: MT9T001P12STC

Features

- DigitalClarity™ Image Sensor Technology
- High frame rate
- Global Reset Release
- Horizontal and vertical binning
- Column and row skip modes
- Superior low-light performance
- Low dark current
- Simple two-wire serial interface
- Programmable Controls: Gain, frame rate, frame size, exposure
- Pin-for-Pin Compatible with Micron's 1.3-Megapixel MT9M001 and 2-Megapixel MT9D001

Applications

- Digital still cameras
- Digital video cameras
- Converged DSCs/camcorders

Description

The Micron® Imaging MT9T001 is a QXGA-format 1/2-inch CMOS active-pixel digital image sensor with an active imaging pixel array of 2,048H x 1,536V. It incorporates sophisticated camera functions on-chip such as windowing, column and row skip mode, and snapshot mode. It is programmable through a simple two-wire serial interface.

The 3-megapixel CMOS image sensor features DigitalClarity—Micron's breakthrough low-noise CMOS imaging technology that achieves CCD image quality (based on signal-to-noise ratio and low-light sensitivity) while maintaining the inherent size, cost, and integration advantages of CMOS.

The sensor can be operated in its default mode or programmed by the user for frame size, exposure, gain setting, and other parameters. The default mode outputs a QXGA image at 12 frames per second (fps). An on-chip analog-to-digital converter (ADC) provides 10 bits per pixel. FRAME_VALID and LINE_VALID signals are output on dedicated pins, along with a pixel clock that is synchronous with valid data.

Table 1: Key Performance Parameters

PARAMETER		TYPICAL VALUE
Optical Format		1/2-inch (4:3)
Active Imager Size		6.55mm(H) x 4.92mm(V) 8.19 (Diagonal)
Active Pixels		2,048H x 1,536V
Pixel Size		3.2um x 3.2um
Color Filter Array		RGB Bayer Pattern
Shutter Type		Global Reset Release, Electronic Rolling Shutter (ERS)
Maximum Data Rate/ Master Clock		48 MPS/48 MHz
Frame Rate	QXGA (2,048 x 1,536)	Programmable up to 12 fps
	UXGA (1,600 x 1,200)	Programmable up to 20 fps
	SXGA (1,280 x 1,024)	Programmable up to 27 fps
	XGA (1,024 x 768)	Programmable up to 43 fps
	VGA (640 x 480)	Programmable up to 93 fps
ADC Resolution		10-bit, on-chip
Responsivity		>1.0 V/lux-sec (550nm)
Dynamic Range		61dB
SNR_{MAX}		43dB
Supply Voltage		3.0V—0 3.6V (3.3V nominal)
Power Consumption		240mW (nominal); 250uW (standby)
Operating Temperature		0°C to +60°C
Packaging		48-pin PLCC

Our MT9T001 produces extraordinarily clear, sharp digital pictures, and its ability to capture both continuous video and single frames makes it the perfect choice for a wide range of consumer and industrial applications, including digital still cameras, digital video cameras, and PC cameras.

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Figure 1: Block Diagram

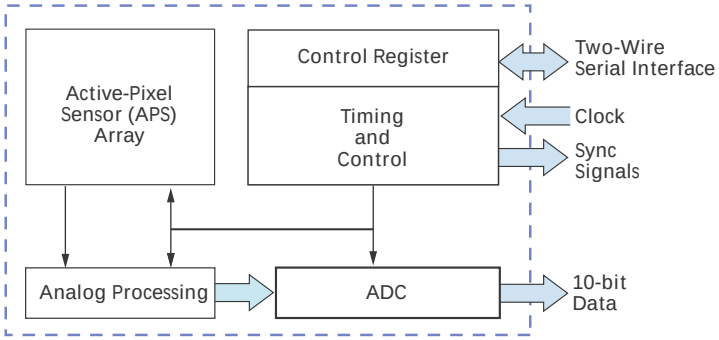
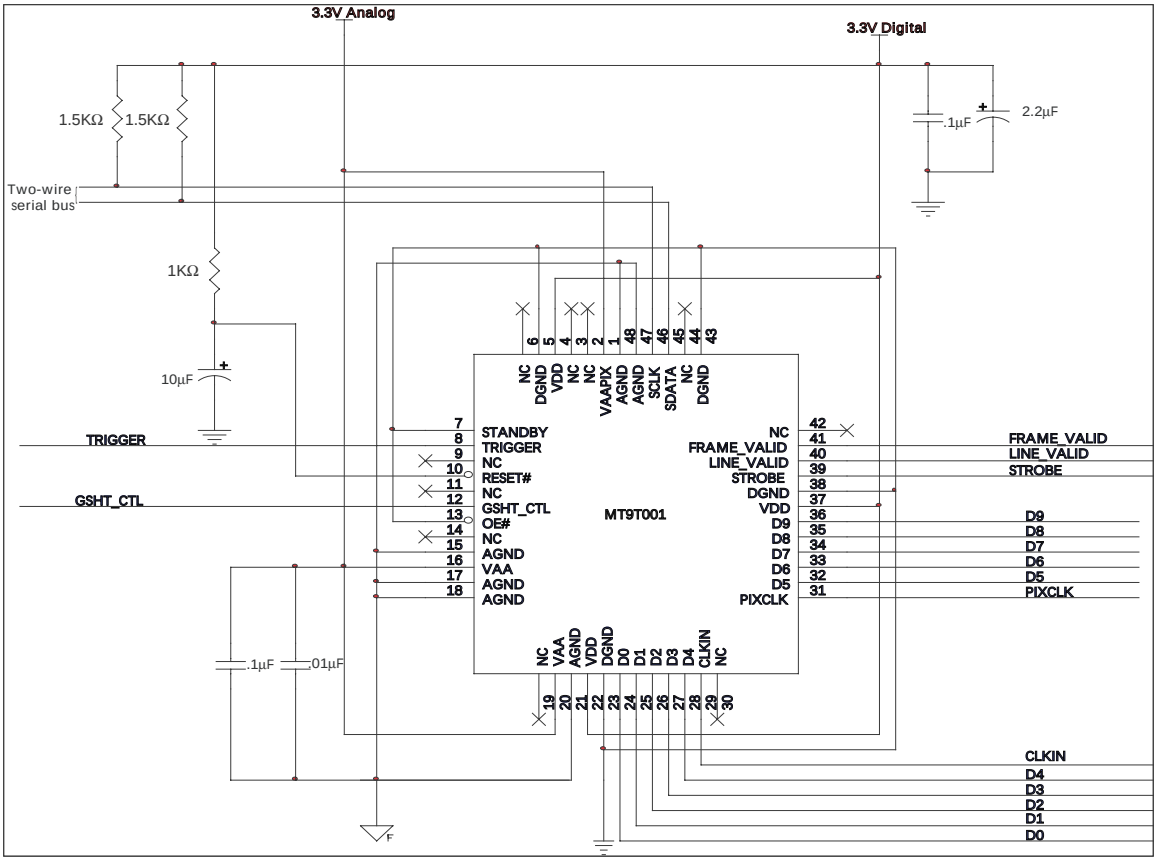


Figure 2: Typical Configuration (Connection)



NOTE:

Resistor value 1.5KΩ is recommended, but may be greater for slower two-wire speed.

Figure 3: Pinout–48-Pin PLCC

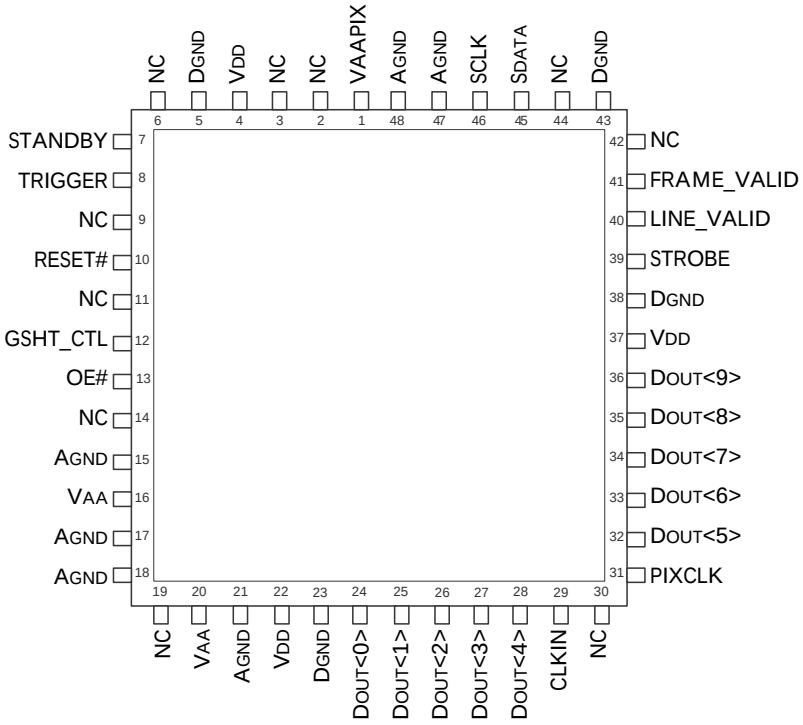


Table 2: Pin Descriptions

PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION
7	STANDBY	Input	Standby: Activates (HIGH) standby mode, disables analog bias circuitry for power saving mode.
8	TRIGGER	Input	Trigger: Activates (HIGH) snapshot sequence.
10	RESET#	Input	Reset: Activates (LOW) asynchronous reset of sensor. All registers assume factory defaults.
13	OE#	Input	Output Enable: OE# when HIGH, places outputs DOUT<0-9>, FRAME_VALID, LINE_VALID, PIXCLK, and STROBE into a tri-state configuration.
29	CLKIN	Input	Clock In: Master clock into sensor (48 MHz maximum).
46	SCLK	Input	Serial Clock: Clock for serial interface.
12	GSHT_CTL	Input	Global shutter control.
45	SDATA	I/O	Serial Data: Serial data bus, requires 1.5KΩ resistor to 3.3V for pull-up.
24, 25, 26, 27, 28, 32, 33, 34, 35, 36	DOUT<0-9>	Output	Data Out: Pixel data output bit 0, DOUT<9> (MSB), DOUT<0> (LSB).
31	PIXCLK	Output	Pixel Clock: Pixel data outputs are valid during falling edge of this clock. Frequency = (master clock).
39	STROBE	Output	Strobe: Output is pulsed HIGH to indicate sensor reset operation of pixel array has completed.
40	LINE_VALID	Output	Line Valid: Output is pulsed HIGH during line of selectable valid pixel data (see Reg0x20 for options).
41	FRAME_VALID	Output	Frame Valid: Output is pulsed HIGH during frame of valid pixel data.

Table 2: Pin Descriptions (continued)

PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION
1	VAAPIX	Supply	Analog Pixel Power: Provide power supply for pixel array, 3.3V ±0.3V.
4, 22, 37	VDD	Supply	Digital Power: Provide power supply for digital block, 3.3V ±0.3V.
5, 23, 38, 43	DGND	Supply	Digital Ground: Provide isolated ground for digital block.
16, 20	VAA	Supply	Analog Power: Provide power supply for analog block, 3.3V ±0.3V.
15, 17, 18, 21, 47, 48	AGND	Supply	Analog Ground: Provide isolated ground for analog block and pixel array.
2, 3, 6, 9, 11,14,19, 30 42, 44	NC	–	No Connect: These pins must be left unconnected.

Pixel Data Format

Pixel Array Structure

The MT9T001 pixel array is configured as 2,112 columns by 1,568 rows, as shown in Figure 4. Columns from 0 through 27 and from 2,085 through 2,111, and also rows from 0 through 15 and from 1,561 through 1,567 are optically black. These optical black columns and rows can be used to monitor the black level. The black row data is used internally for the automatic black level adjustment. However, the black rows and columns can also be read out by setting Reg0x20 (11) and Reg0x1E (7), respectively. There are 2,057 columns by 1,545 rows of optically active pixels, which provides a four-pixel boundary around the QXGA (2,048 x 1,536) image to avoid boundary effects during color interpolation and correction.

The MT9T001 uses a Bayer color pattern, as shown in Figure 5. The even-numbered rows contain green and red color pixels, and odd-numbered rows contain blue and green color pixels. The even-numbered columns contain green and blue color pixels; odd-numbered columns contain red and green color pixels.

Figure 4: Pixel Array Description

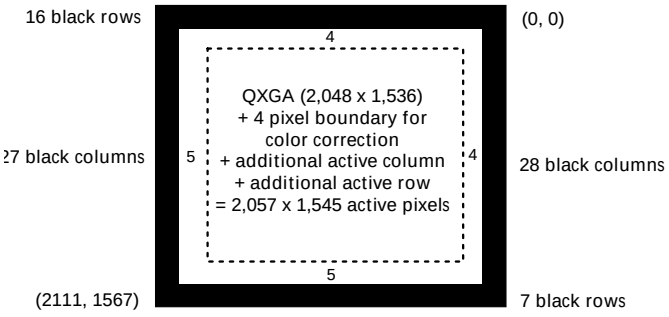
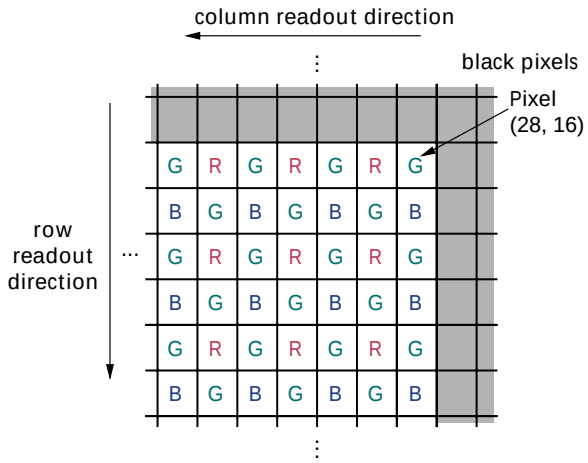


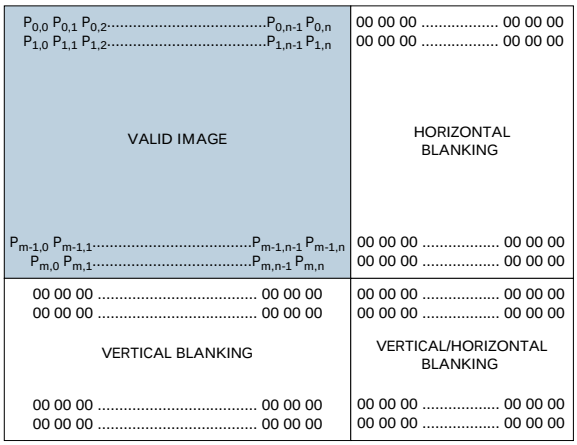
Figure 5: Pixel Color Pattern Detail (Top Right Corner)



Output Data Format

The MT9T001 image data is read out in a progressive scan. Valid image data is surrounded by horizontal blanking and vertical blanking, as shown in Figure 6. The amount of horizontal blanking and vertical blanking is programmable through Reg0x05 and Reg0x06, respectively. LINE_VALID is HIGH during the shaded region of the figure. FRAME_VALID timing is described in "Output Data Timing" on page 10.

Figure 6: Spatial Illustration of Image Readout



Output Data Timing

The data output of the MT9T001 is synchronized with the PIXCLK output. When LINE_VALID is HIGH, one 10-bit pixel datum is output every PIXCLK period.

The PIXCLK can be used as a clock to latch the data. DOUT data is valid on the falling edge of PIXCLK in default mode. The PIXCLK is HIGH while master clock is HIGH and then LOW while master clock is LOW. It is continuously enabled, even during the blanking period. The parameters in P, A, and Q shown in Figure 8 are defined in Table 3.

Figure 7: Timing Example of Pixel Data

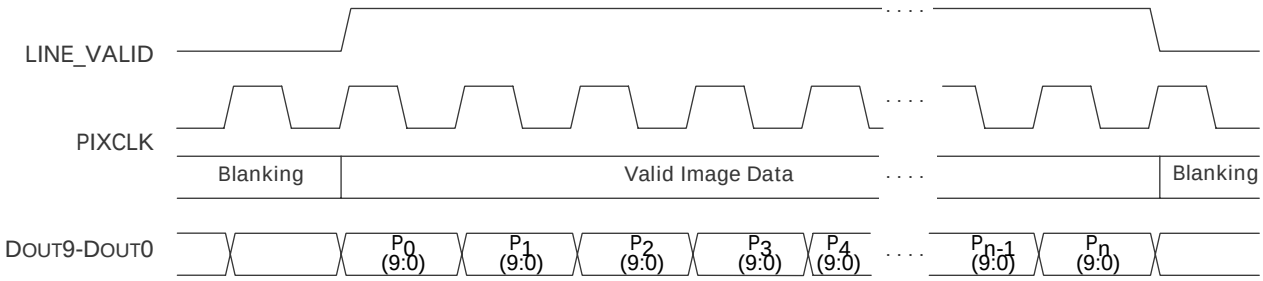
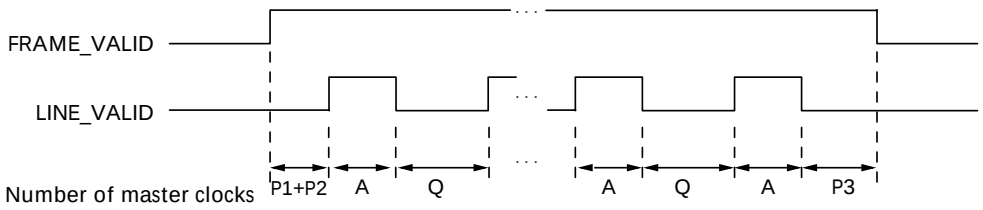


Figure 8: Row Timing and FRAME_VALID/LINE_VALID Signals



Frame Timing Formulas

Table 3: Frame Timing

PARAMETER	NAME	EQUATION (PIXEL CLOCKS = MASTER CLOCK)	DEFAULT TIMING
R	Active Rows	((Reg0x03 + 1)/((Reg0x22[2-0] + 1))) (rounded up to next even number)	1,536 pixel clocks = 32.0µs
A	Active Columns	((Reg0x04 + 1)/((Reg0x23[2-0] + 1))) (rounded up to next even number)	2,048 pixel clocks = 42.67µs
P1	Frame Start Blanking 1	331 if Reg0x22[5-4] = 0, normal 673 if Reg0x22[5-4] = 1, Bin 2x 999 if Reg0x22[5-4] = 2, Bin 3x	331pixel clocks = 6.89µs
P2	Frame Start Blanking 2	38 if Reg0x23[5-4] = 0, normal 22if Reg0x23[5-4] = 1, Bin 2x 14 if Reg0x23[5-4] = 2, Bin 3x	38 pixel clocks = 0.79µs
P3	Frame End Blanking 3	Reg0x05 (minimum Reg0x05 value = 21)	142 pixel clocks = 2.96µs
Q	Horizontal Blanking	P1 + P2 + P3	511 pixel clocks = 10.65µs
P4	Shutter Overhead	Reg0x0C + 316 x (Reg0x23[5-4] +1)	316 pixel clocks = 6.58µs
t_{ROW}	RowTime	The greater of: (A + Q) or (P1+ P4)	2,559 pixel clocks = 53.31µs
V	Vertical Blanking	(Reg0x06 + 1) x t_{ROW}	66,534 pixel clocks = 1.39ms
t_{FV}	Frame Valid Time	R x t_{ROW}	3,930,624 pixel clocks = 81.89ms
t_{FRAME}	Total Frame Time	The greater of: ((65536 x Reg0x08 + Reg0x09) x t_{ROW}) or (t_{FV} + V)	3,997,158 pixel clocks = 83.27ms

Table 4: Register List and Default Values

REGISTER # (HEX)	DESCRIPTION	DATA FORMAT (BINARY)	DEFAULT VALUE (HEX)
0x00	Chip Version	0001 0110 0000 0001	0x1611
0x01	Row Start	0000 00dd dddd ddd0	0x0014
0x02	Column Start	0000 0ddd dddd ddd0	0x0020
0x03	Row Size (Window Height)	0000 00dd dddd ddd1	0x05FF
0x04	Col Size (Window Width)	0000 0ddd dddd ddd1	0x07FF
0x05	Horizontal Blanking	0000 00dd dddd dddd	0x008E
0x06	Vertical Blanking	0000 00dd dddd dddd	0x0019
0x07	Output Control	0d00 0000 d0dd 00dd	0x0002
0x08	Shutter Width Upper	0000 0000 0000 dddd	0x0000
0x09	Shutter Width	dddd dddd dddd dddd	0x0619
0x0A	Pixel Clock Control	dddd dddd dddd dddd	0x0000
0x0B	Restart	0000 0000 0000 000d	0x0000
0x0C	Shutter Delay	0000 00dd dddd dddd	0x0000
0x0D	Reset	0000 0000 0000 000d	0x0000
0x1E	Read Mode 1	dddd dddd dd00 0000	0xC040
0x20	Read Mode 2	ddd0 ddd0 0000 00dd	0x0000
0x21	Read Mode 3	0000 0000 0000 00dd	0x0000
0x22	Row Address Mode	0ddd 0ddd 0ddd 0ddd	0x0000
0x23	Column Address Mode	0000 0ddd 00dd 0ddd	0x0000
0x2B	Green1 Gain	0ddd dddd 0d0d dddd	0x0008
0x2C	Blue Gain	0ddd dddd 0d0d dddd	0x0008
0x2D	Red Gain	0ddd dddd 0d0d dddd	0x0008
0x2E	Green2 Gain	0ddd dddd 0d0d dddd	0x0008
0x35	Global Gain	dddd dddd dddd dddd	0x0008
0x49	Black Level	0000 0ddd dddd dddd	0x00A8
0x4B	Row Black Default Offset	0000 0ddd dddd dddd	0x0028
0x5D	BLC Delta Thresholds	0ddd dddd 0ddd dddd	0x2D13
0x5F	Cal Threshold	dddd dddd dddd dddd	0x231D
0x60	Green1 Offset	0000 000d dddd dddd	0x0020
0x61	Green2 Offset	0000 000d dddd dddd	0x0020
0x62	Black Level Calibration	dddd d000 0000 00dd	0x0000
0x63	Red Offset	0000 0ddd dddd dddd	0x0020
0x64	Blue Offset	0000 0ddd dddd dddd	0x0020
0xF8	Chip Enable/Synchronize	0000 0000 0000 00dd	0x0001
0xFF	Chip Version	0001 0110 0000 0001	0x1611

NOTE:

1 = always 1
0 = always 0
d = programmable
? = read only

Table 5: Reserved Register List and Default Values

REGISTER # (HEX)	DESCRIPTION	DEFAULT VALUE (HEX)
0x27	Reserved	0x0001
0x29	Reserved	0x0401
0x30	Reserved	0x0000
0x32	Reserved	0x0008
0x3C	Reserved	0x0010
0x3D	Reserved	0x0005
0x3E	Reserved	0x0003
0x3F	Reserved	0x0002
0x40	Reserved	0x0005
0x41	Reserved	0x0003
0x42	Reserved	0x0003
0x43	Reserved	0x0003
0x44	Reserved	0x0003
0x45	Reserved	0x0010
0x46	Reserved	0x0010
0x47	Reserved	0x0010
0x48	Reserved	0x0010
0x4A	Reserved	0x0010
0x4C	Reserved	0x0030
0x4D	Reserved	0x0020
0x4E	Reserved	0x0010
0x4F	Reserved	0x0028
0x50	Reserved	0x8004
0x51	Reserved	0x0002
0x52	Reserved	0x8004
0x53	Reserved	0x0002
0x54	Reserved	0x0010
0x55	Reserved	0x0010
0x56	Reserved	0x0020
0x5B	Reserved	0x0007
0x5C	Reserved	0x071C
0x5E	Reserved	0x5364
0x65	Reserved	0x0000
0x67	Reserved	0x3FFF
0x68	Reserved	0x0000
0x69	Reserved	0x0000
0x6A	Reserved	0x0000
0x6B	Reserved	0x0000
0x6C	Reserved	0x0000
0x6D	Reserved	0x0000
0x6E	Reserved	0x0000
0x70	Reserved	0x00A3
0x71	Reserved	0xA204
0x72	Reserved	0xA006
0x73	Reserved	0x260A
0x74	Reserved	0x280C

Table 5: Reserved Register List and Default Values (continued)

REGISTER # (HEX)	DESCRIPTION	DEFAULT VALUE (HEX)
0x75	Reserved	0x520D
0x76	Reserved	0x7054
0x77	Reserved	0x0000
0x78	Reserved	0x9C57
0x79	Reserved	0x9E02
0x7A	Reserved	0x9E04
0x7B	Reserved	0x9E06
0x7C	Reserved	0xA006
0x7D	Reserved	0x5308
0x7E	Reserved	0x3208
0x7F	Reserved	0x7C52
0x80	Reserved	0x004E
0x81	Reserved	0x4E00
0x82	Reserved	0x4C02
0x83	Reserved	0x480C
0x84	Reserved	0x4A0E
0x86	Reserved	0x2E0C
0x87	Reserved	0x0000
0x89	Reserved	0x4C02
0x8A	Reserved	0x0000
0x8B	Reserved	0x4F0A
0x8C	Reserved	0x3A0A
0x90	Reserved	0x061F
0x91	Reserved	0x0000
0x92	Reserved	0x0001
0xF1	Reserved	0x0000
0xFA	Reserved	0x0000
0xFB	Reserved	0x0000
0xFC	Reserved	0x0000
0xFD	Reserved	0x0000

NOTE:
Even reading some of these registers will cause this part to go into an unknown state.

Register Description

Table 6: Register Descriptions

REGISTER	BIT	DESCRIPTION
Chip ID		
0x00	15:0	This register is read-only and gives the chip identification number: 0x1611.
Row Start		
0x01	10:0	First row to be read out—default = 0x0014 (20), register value must be an even number.
Column Start		
0x02	11:0	First column to be read out—default = 0x0020 (32), register value must be an even number. Note: If column bin is enabled, the value must be a multiple of Reg0x23 [5:4] + 1.
Row Size		
0x03	10:0	Window height (number of rows - 1)—default = 0x5FF (1535), register value must be an odd number. Minimum value for 0x03 = 0x0001.
Column Size		
0x04	10:0	Window width (number of columns - 1)—default = 0x7FF (2047), register value must be an odd number. Minimum value for 0x04 = 0x0001.
Horizontal Blank		
0x05	10:0	Horizontal Blank—default = 0x008E (142 pixels). Minimum value = 0x0015 (21).
Vertical Blank		
0x06	10:0	Vertical Blank—default = 0x0019 (25 rows). Minimum value = 0x0003 (3).
Output Control This register controls various features of the output format for the sensor.		
0x07	0	Synchronize changes. 0 = normal operation, update changes to registers that affect image brightness (integration time, shutter delay, gain, horizontal and vertical blank, window size, row/column skip, or row mirror) at the next frame boundary. 1 = do not update any changes to these settings until this bit is returned to “0.”
	1	Chip Enable. 1 = normal operation. 0 = sensor readout is stopped and analog control signals are put in a state which draws minimal power.
	6	Override pixel data. 0 = normal operation. 1 = output programmed test data (see Reg0x32). First valid columns will output contents of test data register; second columns will output inverted data. Third columns will output non-inverted data, fourth inverted, etc.
Shutter Width Upper		
0x08	15:0	The most significant bits of the shutter width, which are combined with Shutter Width (Reg0x09). The total shutter width is therefore: (((Shutter_Width_Upper) x 65536) + Shutter_Width). This should allow a shutter width from about 50us to about 50s at default row time.
Shutter Width		
0x09	15:0	Number of rows of integration, the exposure time; the time between when the rolling shutter resets a row and that row is read out, in rows. Default = 0x0619 (1561). Minimum value = 0x0001 (1).

Table 6: Register Descriptions (continued)

REGISTER	BIT	DESCRIPTION
Pixel Clock Control		
0x0A	15	Invert Pixel Clock—default = 0x00 (0) When set, line_valid, frame_valid, and data10_out will be set up to the rising edge of PIXCLK. When clear, they are set up to the falling edge. This is accomplished by inverting the PIXCLK output.
	10:8	Shift Pixel Clock—default = 0x00 (0) Two's compliment value representing how far to shift the PIXCLK output pin relative to DOUT, in CLKIN cycles. Positive values shift PIXCLK later in time relative to DOUT (and thus relative to the internal array/datapath clock. No effect unless PIXCLK is divided by Divide Pixel Clock.
	6:0	Divide Pixel Clock —default = 0x00 (0) Produces a PIXCLK that is divided by the value times two. The value must be a power of 2. This will slow down the internal clock in the array control and datapath blocks, including pixel readout. It will not affect the two-wire serial interface clock. A value of 0 corresponds to a PIXCLK with the same frequency as CLK_IN. A value of 1 means f_PIXCLK = (f_CLK_IN / 2); 2 means f_PIXCLK = (f_CLK_IN / 4); 64 means f_PIXCLK = (f_CLK_IN / 128); etc.
Frame Restart		
0x0B	0	Setting bit 0 to “1” of Reg0x0B will cause the sensor to abandon the readout of the current frame and restart from the first row. This register automatically resets itself to 0x0000 after the frame restart. The first frame after this event is considered to be a "bad frame" (see description for Reg0x20, bit 0).
Shutter Delay		
0x0C	10:0	Shutter delay—default = 0x0000 (0). This is the number of pixel clocks that the timing and control logic waits before asserting the reset for a given row.
Reset		
0x0D	0	Setting this bit will put the sensor into reset mode, which will set the sensor to its default power-up state. Clearing this bit will resume normal operation.
Read Mode 1		
0x1E	8	Snapshot Mode—default is 0 (continuous mode). 1 = enable Snapshot trigger signal can come from outside signal (trigger pin 8 on the sensor) or from serial interface register restart, i.e. programming a “1” to bit 0 of Reg0x0B.
	9	Strobe Enable—default is 0 (no strobe signal). 1 = enable strobe (signal output from the sensor during the time all rows are integrating). See strobe width for more information.
	10	Strobe Width—default is 0 (strobe signal width at minimum length, one row of integration time, prior to Line_Valid going high). 1 = extend strobe width (strobe signal width extends to entire time all rows are integrating; shutter width must be >= row size + vertical blanking).
	11	Strobe Override—default is 0 (strobe signal created by digital logic). 1 = override strobe signal (strobe signal is set high when this bit is set, low when this bit is set low. It is assumed that strobe enable is set to “0” if strobe override is being used).
Read Mode 2		
0x20	0	No bad frames—1 = output all frames (including bad frames). 0 = default, only output good frames. A bad frame is defined as the first frame following a change to: window size or position, horizontal blanking, row or column skip, or mirroring.
	9	1 = "Continuous" LINE_VALID (continue producing Line_Valid during vertical blanking). 0 = Normal Line_Valid (default, no Line_Valid during vertical blank).
	10	1 = LINE_VALID = "Continuous" LINE_VALID XOR FRAME_VALID. 0 = LINE_VALID determined by bit 9 (default).

Table 6: Register Descriptions (continued)

REGISTER	BIT	DESCRIPTION
Read Mode 3		
0x21	0	Global Reset—default = 0x0000—when set, snapshot mode will make use of the global reset — that is, the entire array will be released from reset simultaneously. Ineffective unless Snapshot (Reg0x1E[8]) is set.
	1	Use GSHT_CTL—default = 0x0000. When set, the leading edge of the GSHT_CTL pad signal will be used to start the shutter sequence in snapshot mode, and the trailing edge will start the read sequence. When clear, the leading edge of the TRIGGER pad signal will be used to initiate the shutter sequence, the trailing edge of GSHT_CTL will start the exposure, and the trailing edge of the TRIGGER pad signal will be used to start the strobe and readout. Ineffective unless Snapshot (Reg0x1E[8]) and Global Reset are set.
Row Address Mode		
0x22	2:0	Row Skip—the number of row-pairs to skip for every row read. For example, “0” means read every row pair. “1” is skip 2x; 2 is skip 3x, etc. If Row Bin is non-zero, this should be set to the interval between the first rows in each bin. For full binning, Row Skip equals Row Bin.
	5:4	Row Bin—the number of rows to be read per row output minus one. For normal read out, this should be “0.” For Bin 2x, it should be “1”; for Bin 3x, it should be “2.”
Column Address Mode		
0x23	2:0	Column Skip—the number of column-pairs to skip for every pair read. Zero means read every column. “1” means skip one pair for every pair read (Skip 2x); 2 means skip 2 pairs for every pair read (Skip 3x) etc.
	5:4	Column Bin—the number of columns to be addressed per column read out minus one. Zero will produce standard 1:1 read out. A value of “1” will produce Bin 2x; “2” would be Bin 3x. Note: Column start address value must be a multiple of Reg0x23 [5:4] + 1.
Green1 Gain		
0x2B	6:0	Green1 analog gain—default = 0x08 (8) = 1x gain.
	14:8	Green1 digital gain—default = 0x00 (0) = 1x gain.
Blue Gain		
0x2C	6:0	Blue analog gain—default = 0x08 (8) = 1x gain.
	14:8	Blue digital gain—default = 0x00 (0) = 1x gain.
Red Gain		
0x2D	6:0	Red analog gain—default = 0x08 (8) = 1x gain.
	14:8	Red digital gain—default = 0x00 (0) = 1x gain.
Green2 Gain		
0x2E	6:0	Green2 analog gain—default = 0x08 (8) = 1x gain.
	14:8	Green2 digital gain—default = 0x00 (0) = 1x gain.
Global Gain		
0x35	6:0	Global analog gain—default = 0x08 (8) = 1x gain.
	14:8	Global digital gain—default = 0x00 (0) = 1x gain. This register can be used to set all four gains at once. When read, it will return the value stored in Reg0x2B.
Black Level		
0x49	11:2	Desired black level in image.

Table 6: Register Descriptions (continued)

REGISTER	BIT	DESCRIPTION
Black Level Calibration Coarse Thresholds		
0x5D	6:0	Low Coarse Threshold—default = 0x13. This value should be less than Low Target Threshold. See High Coarse Threshold below.
	14:8	High Coarse Threshold—default = 0x2D. If the average black value for a color is higher than this value or lower than Low Coarse Threshold, the coarse mode will be activated (if enabled). Once the black level is between the High Coarse Threshold and the Low Coarse Threshold, the fine method will be used. This value should be set no lower than High Target Threshold.
Black Level Calibration Target Thresholds		
0x5F	6:0	Thres_lo: Lower threshold for black level in units of ADC LSBs—default = 29.
	14:8	Thres_hi: Upper threshold for black level in units of ADC LSBs—default = 35. When the black value for a color is within these thresholds, it will be considered to be on target.
Green1 Offset		
0x60	8:0	Cal Green1—Two's compliment representation of analog offset correction value for Green1.
Green2 Offset		
0x61	8:0	Cal Green2—Two's compliment representation of analog offset correction value for Green2.
Black Level Calibration		
0x62	0	Manual override of black level correction. 1 = override automatic black level correction with programmed values. 0 = normal operation (default).
	1	Force/disable black level calibration. 0 = Enable Offset Correction (default). 1 = disable Offset Correction Voltage (Offset Correction Voltage = 0.0V).
	12	Recalculate Black Level—1 = start a new running digitally filtered average for the black level (this is internally reset to “0” immediately), and do a rapid sweep to find the new starting point. 0 = normal operation (default).
	13	Lock Red/Blue Calibration—when set, only one calibration value will be used for both red and blue channels. Default is 0, set to “0” at all times. Note: Gain for Red and Blue channels must be equal for setting to be effective.
	14	Lock Green Calibration—when set, only one calibration value will be used for both Green1 and Green2 channels. Default is 0, set to “0” at all times. Note: Gain for Green1 and Green2 channels must be equal for setting to be effective.
Red Offset		
0x63	8:0	Cal Red. Two's compliment representation of analog offset correction value for Red.
Blue Offset		
0x64	8:0	Cal Blue. Two's compliment representation of analog offset correction value for Blue.
Chip Enable and Two-Wire Serial Interface Write Synchronize		
0xF8	0	Mirrors the functionality of Reg0x07 bit 1,(Chip Enable). 1 = normal operation. 0 = stop sensor read out. When this is returned to “1,” sensor read out restarts at the starting row in a new frame.
	1	Mirrors the functionality of Reg0x07 bit 0 (Synchronize changes). 0 = normal operation, update changes to registers that affect image brightness (integration time, integration delay, gain, horizontal and vertical blank, window size, row/column skip, or row/column mirror) at the next frame boundary. 1 = do not update any changes to these settings until this bit is returned to ”0.”

Feature Description

Window Control

Reg0x01, Reg0x02, Reg0x03, and Reg0x04 These registers control the size of the window.

Window Size

The default programmed window size is 2,048 columns by 1,536 rows (2,048H x 1,536V). The control logic allows the flexibility to change the window size by programming Reg0x03 and Reg0x04. Reg0x03 controls the window height (number of rows) and Reg0x04 controls the window width (number of columns). The value to be programmed in Reg0x03 is the desired number of rows -1. The value to be programmed in Reg0x04 is the desired number of columns -1.

The minimum value for Reg0x03 is 0x0001; for Reg0x04, 0x0001. Thus, the smallest window size is two columns by two rows (2H x 2V). Note that the value of Reg0x03 and Reg0x04 must be an odd number (there can only be even number of columns). It is also important to note that the user can program the window size to be any format desired. Table 7 shows examples of register settings to achieve various resolutions and frame rates.

Table 7: Standard Resolutions

RESOLUTION	FRAME RATE	COLUMN_SIZE (REG0x04)	ROW_SIZE (REG0x03)	SHUTTER WIDTH (REG0x09)
2,048 x 1,536 QXGA	12 fps	2,047	1,535	<1,552
1,600 x 1,200 UXGA	20 fps	1,599	1,199	<1,216
1,280 x 1,024 SXGA	27 fps	1,279	1,023	<1,040
1,024 x 768 XGA	43 fps	1,023	767	<784
800 x 600 SVGA	65 fps	799	599	<616
640 x 480 VGA	93 fps	639	479	<496

Table 8: Wide Screen (16:9) Resolutions

RESOLUTION	FRAME RATE	COLUMN_SIZE (REG0x04)	ROW_SIZE (REG0x03)	SHUTTER WIDTH (REG0x09)
1,920 x 1,080 HDTV	18 fps	1,919	1,079	<1,096
1,280 x 720 HDTV	39 fps	1,279	719	<736

NOTE:

For Table 7 and Table 8 above, the settings for Reg0x05 (horizontal blanking) and Reg0x06 (vertical blanking) are 21 and 15 respectively, while all of the registers are set to default.

Electronic Panning

In addition to changing the window size, the user has the flexibility to change the location of the readout window. Reg0x01 controls the first row to be read out and Reg0x02 controls the first column to be read out. The default values are 0x0014 (decimal 20) for Reg0x01 and 0x0020 (decimal 32) for Reg0x02. Note that the first column to be read out must be an even number.

Reg0x01 and Reg0x02, together with Reg0x03 and Reg0x04, allow the user to choose any segment of the imager array to be read out. This is especially beneficial when the user needs to zoom in on a small portion of the image and perform analysis on the image content.

Figure 9 shows some examples of the electronic panning/zoom-in and windowing capabilities of the sensor.

Blanking Control

Reg0x05 and Reg0x06 These registers control the blanking time in a row (called column fill-in or horizontal blanking) and between frames (vertical blanking). Horizontal blanking is specified in terms of pixel clocks. Vertical blanking is specified in terms of row readout times. The actual imager timing can be calculated using the equations given in Table 3 on page 11.

Reg0x05 controls the horizontal blanking time in a row. The value is specified in terms of pixel clocks. Default value of 0x008E for Reg0x05 results in a horizontal blanking time of 511 pixel clocks. Note that the minimum value for Reg0x05 is 21. Thus, the minimum horizontal blanking time is 390 pixel clocks.

Reg0x06 controls the vertical blanking time in a row. The value is specified in terms of the number of rows. Default value of 0x0019 for Reg0x06 results in a vertical blanking time of 26-row time.

Frame Time

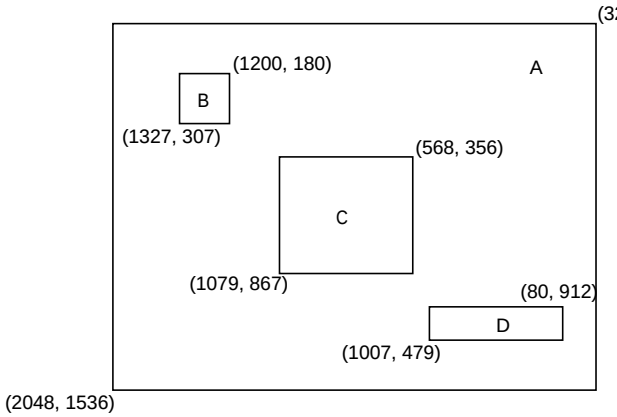
Reg0x03, Reg0x04, Reg0x05, and Reg0x06 Total frame time in terms of pixel clocks can be obtained using the formula given in Table 3 on page 11. The user can change the number of columns and rows read out, horizontal blanking and vertical blanking times to obtain different frame rates.

High Frame Rate Readout Modes

Reg0x01, Reg0x02, Reg0x03, Reg0x04, Reg0x05, and Reg0x06 In addition to having the flexibility to read out smaller standard formats, the sensor gives the user the option of reading out nonstandard formats. This is particularly useful if the user needs to zoom in on a particular segment of the image to perform high-speed mathematical calculations (e.g., high-speed viewfinder or auto-focus applications).

In applications such as the auto-focus mode, the user may need more horizontal resolution than vertical. Thus, the user can window down to the mid-section of the imager array by programming Reg0x01 and Reg0x03 to change the row start address and the window height. Figure 10 is an example of how the user may want to window down to 2,048H x 512V from the default of 2,048H x 1,536V. See also Table 9 for other auto-focus mode resolutions.

Figure 9: Windowing Capabilities

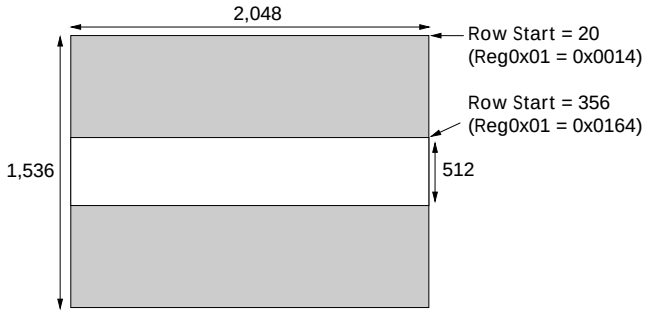


	Window Size	Reg0x01	Reg0x02	Reg0x03	Reg0x04
Window A	2,048 x 1,536	0x0014	0x0020	0x05FF	0x07FF
Window B	128 x 128	0x00B4	0x04B0	0x007F	0x007F
Window C	512 x 512	0x0164	0x0238	0x01FF	0x01FF
Window D	400 x 96	0x0390	0x0050	0x018F	0x005F

Table 9: Auto-Focus Modes

RESOLUTION	FRAME RATE	COLUMN_SIZE (REG0x04)	ROW_SIZE (REG 0x03)	HORIZONTAL_BLANK (REG0x05)	VERTICAL_BLANK (REG0x06)	ROW (REG 0x22)	ROW_SKIP (REG 0x22)	COLUMN_BIN (REG0x23)	COLUMN_SKIP (REG0x23)
2,048 x 512	30 fps	2,047	1,535	22	1	2	2	0	0
2,048 x 256	60 fps	2,047	1,535	22	0	2	5	0	0
2,048 x 128	120 fps	2,047	1,023	34	14	1	7	0	0

Figure 10: Windowing



The user can change Reg0x05 and Reg0x06 to obtain the desired frame rate. Also, the user may want to perform row skip modes to obtain larger field of view if high-frequency vertical resolution is not critical.

Pixel Integration Time Control

Reg0x09 and Reg0x0C The integration time of the pixel is the amount of time the pixels are set to collect charge generated from light. The user can change the integration time of the sensor by programming Reg0x09. The value of Reg0x09 sets the number of row time for integration. The sensor also supports sub-row integration time for fine control of pixel integration time.

The formula for calculating the pixel integration time is (reference Table 3 on page 11 for P1 description):

$^{t}INT = (65536 \times Reg0x08 + Reg0x09) \times {}^{t}ROW - Reg0x0C - P1 + 132$

Typically, the value of Reg0x09 is limited to the number of rows per frame (which includes vertical blanking rows), such that the frame rate is not affected by the integration time. However, if Reg0x09 is increased beyond the total number of rows per frame, then additional blanking rows are added as needed.

While the user can adjust the integration time to the desired value according to the aforementioned formula, not all integration times may be desired under certain lighting conditions. If the light source has a flicker component, then the integration time needs to be set properly to avoid banding in the image.

Under 60Hz flicker, the integration time must be a multiple of 1/120 of a second to avoid flicker. Under 50Hz flicker, the integration time must be a multiple of 1/100 of a second to avoid flicker.

Snapshot Mode and Flash Control

Reg0x1E, STROBE pin and TRIGGER pin

Setting up for Snapshot Mode

Snapshot mode must be enabled before use by setting bit 8 = “1” of Reg0x1E. There are two important signals used for snapshot mode: TRIGGER and STROBE. The TRIGGER signal initiates the start of a single frame capture and STROBE is an output pulse that may be used to turn on a flash and/or activate a mechanical shutter.

Triggering A Snapshot

The TRIGGER signal required for starting a frame capture may be generated in the following two ways:

a. External TRIGGER Pulse
   Pin 8 is a digital input that may be used to supply an external trigger signal input. The snap-

shot operation begins after the TRIGGER pulse transitions from a HIGH to LOW state.

b. TRIGGER from Register Setting
A second method for triggering a snapshot is by setting bit 0 = 1 of Reg0x0B (Restart). This register automatically returns bit 0 to "0" after the TRIGGER is initiated. This bit does not need to be reset by the user after use.

Strobe Pulse Output

The STROBE pulse must be enabled before use by setting Reg0x1E [bit 9] = 1. The STROBE signal has two options for pulse length and may be selected using Reg0x1E [bit 10] as shown in Table 10.

Table 10: STROBE Pulse Output

REG 0x1E BIT 10	STROBE PULSE WIDTH
0	1 row time (default)
1	((655326 x Reg0x08 + Reg0x09 - R) -16) x ^{t}ROW - V

After the TRIGGER pulse has signaled a snapshot operation, each row of the imager array is reset in sequence to clear out any accumulated signal. Once each row of the imager is reset, the STROBE pulse is output from the imager with a length dependent upon the characteristics described above. After the STROBE pulse goes low, the imager waits 16 additional rows and then each row from the pixel array is read out. Note that no STROBE will be generated unless the shutter width is greater than the output image height plus vertical blanking.

Global Shutter Release Snapshot Mode

Reg0x1E and Reg0x21

In addition to the standard snapshot mode, the MT9T001 has a global shutter release mode which may be combined with a mechanical shutter to achieve simultaneous exposure of all rows in the image.

Two global shutter modes are available: programmed exposure and bulb mode. In programmed exposure mode, the exposure time is dictated by {Reg0x08, Reg0x09} (Shutter Width). In bulb mode, the TRIGGER and GSHT_CTL pins are used to achieve an arbitrary exposure time.

Programmed Exposure Mode

To use programmed exposure mode:

1. Set up snapshot mode as normal (including any STROBE preferences).
2. Set Reg0x21 (Read Mode 3) to 0x0003.
3. Assert (transition LOW to HIGH) the GSHT_CTL pin to reset the array. This pin must remain HIGH for 18820 PIXCLKs.
4. Negate (transition HIGH to LOW) the GSHT_CTL pin to begin the exposure. The exposure starts 1000 PIXCLKs after the falling edge of GSHT_CTL. NOTE: Unlike normal snapshot mode, Reg0x0B (Restart) may not be used to initiate the exposure in global shutter modes.
5. Row readout will begin automatically. The mechanical shutter should be closed before row read out begins. The trailing edge of STROBE (if enabled) will occur ((65536 x Reg0x08 + Reg0x09) x ^{t}ROW + 2000) PIXCLKs after the falling edge of GSHT_CTL. Readout of the active window will start the lesser of 16 x ^{t}ROW or (Reg0x06 + 1) x ^{t}ROW later.

Bulb Mode

To use bulb mode:

1. Set up snapshot mode as normal (including any STROBE preferences).
2. Set Reg0x21 (Read Mode 3) to 0x0001.
3. Assert (transition LOW to HIGH) the GSHT_CTL pin.
4. Assert (transition LOW to HIGH) the TRIGGER pin to reset the array. This pin must remain HIGH for at least 18,820 PIXCLKs.
5. Negate (transition HIGH to LOW) the GSHT_CTL pin to begin the exposure. The exposure starts 1,000 PIXCLKs after the falling edge of GSHT_CTL. NOTE: Unlike normal snapshot mode, Reg0x0B (Restart) may not be used to initiate the exposure in global shutter modes.
6. Negate (transition HIGH to LOW) the TRIGGER pin to begin row read out. The mechanical shutter should be closed before row read out begins. The trailing edge of STROBE (if enabled) will occur ((65536 x Reg0x08 + Reg0x09) x ^{t}ROW) PIXCLKs after the falling edge of TRIGGER. Read out of the active window will start the lesser of 16 x ^{t}ROW or (Reg0x06 + 1) x ^{t}ROW later. In this mode, the shutter width (Reg0x08, Reg0x09) would normally be set to a low number, allowing row readout to start immediately after the trailing edge of TRIGGER.

Skip and Bin Modes

Row and column skip modes use subsampling to reduce the output resolution without reducing field-of-view. The MT9T001 also has row and column binning modes, which can reduce the impact of aliasing introduced by the use of skip modes. This is achieved by the averaging of two or three adjacent rows and columns (adjacent same-color pixels). Both 2x and 3x binning modes are supported. Rows and columns can be binned independently.

Table 11: Bin and Skip Mode Resolution

RESOLUTION	FRAME RATE	COLUMN_SIZE (REG0x04)	ROW_SIZE (REG 0x03)	HORIZONTAL_BLANK (REG0x05)	VERTICAL_BLANK (REG0x06)	ROW_BIN (REG 0x22)	ROW_SKIP (REG 0x22)	COLUMN_BIN (REG0x23)	COLUMN_SKIP (REG0x23)
1,024 x 768 XGA	34 fps	2,047	1,535	22	40	1	1	1	1
800 x 600 SVGA	50 fps	1,599	1,199	22	30	1	1	1	1
640 x 480 VGA	48 fps	1,919	1,439	21	31	2	2	2	2

NOTE:

Column start address value must be a multiple of Reg0x23 [5-4] + 1.

To use binning mode, set Reg0x22[5–4] (row bin) or Reg0x23[5–4] (column bin) to the desired reduction minus 1, as would be done for skip mode. Additionally, Reg0x22[2–0] (column skip) must be set no less than Reg0x22[5–4], and Reg0x23[2–0] (row skip) must be set no less than Reg0x23[5–4]. Row and column skip modes may be set higher than the corresponding binning modes to achieve greater reductions, but binning must be done. The different skip modes supported are between 2x and 8x in both column and row directions. The different binning modes supported are 2x and 3x. See Table 12 for register bits controlling the different bin and skip modes.

Table 12: Skip and Bin Modes

REGISTER BIT	SKIP/BIN MODES	READOUTS
Reg0x23		
Bit[2-0]	No column skip	col0, col1, col2, col3, col4, col5, etc.
	Column skip 2x	col0, col1, col4, col5, col8, col9, etc.
	Column skip 3x	col0, col1, col16, col7, col12, col13 etc.
	Column skip 4x	col0, col1, col8, col9, col16, col17, etc.
	Column skip 8x	col0, col1, col16, col17, col32, col33, etc.
Bit[5-4]	Column Bin 2x	Binning of 2 adjacent same-color pixels in a 4x4 window
	Column Bin 3x	Binning of 3 pixel of each color plane in a 6x6 window
Reg0x22		
Bit[2-0]	No row skip	row0, row1, row2, row3, row4, row5, etc.
	Row skip 2x	row0, row1, row4, row5, row8, row9, etc.
	Row skip 3x	row0, row1, row6, row7, row12, row13, etc.
	Row skip 4x	row0, row1, row8, row9, row16, row17, etc.
	Row skip 8x	row0, row1, row16, row17, row32, row33, etc.
Bit[5-4]	Row bin 2x	Binning of 2 pixel of each color plane in a 4x4 window
	Row bin 3x	Binning of 3 pixel of each color plane in a 6x6 window

NOTE:

Column and row skip modes 1x through 8x are available on the MT9T001. Also, the read outs shown assume column start and row start addresses are both “0”.

Figure 11: Column Skip 2x; Row Skip 2X Enabled

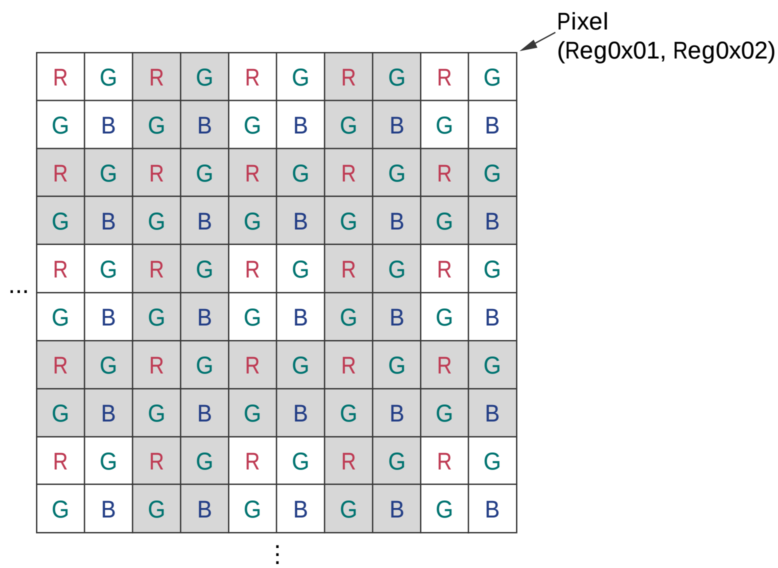


Figure 12: Column Skip 3x; Row Skip 3X Enabled

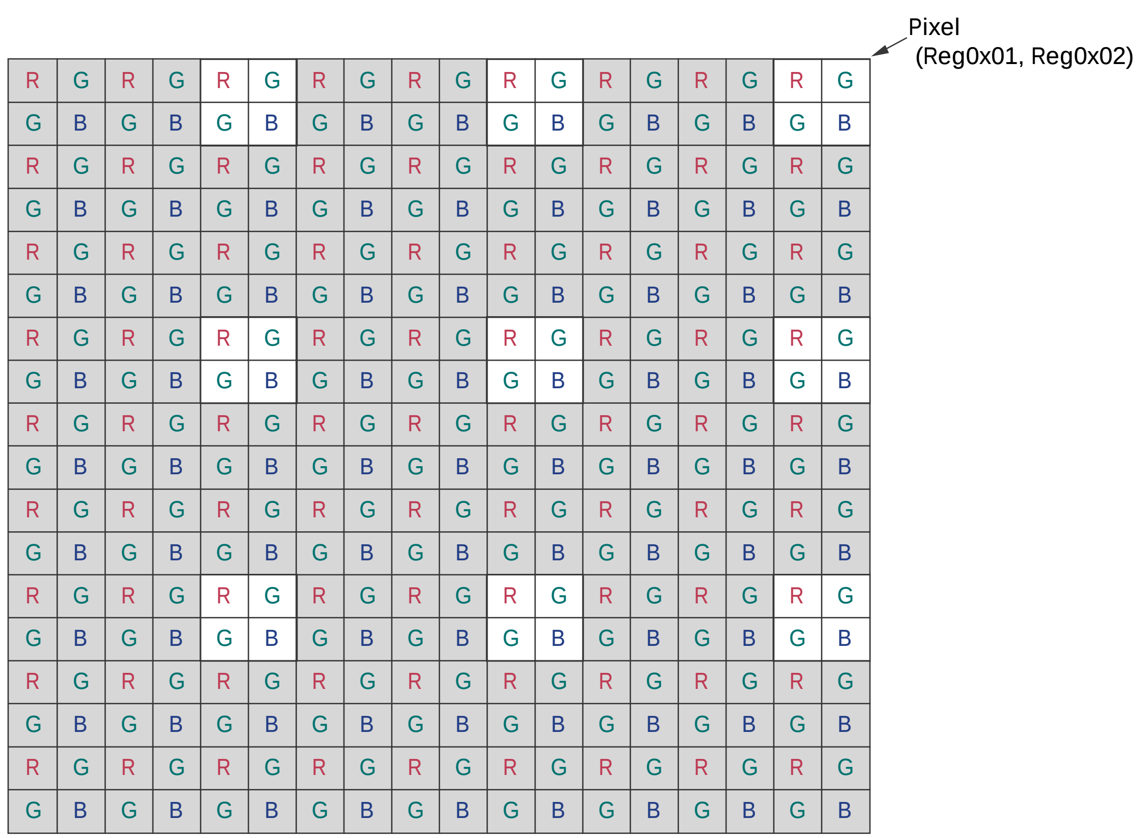


Figure 13: Column Skip 4x; Row Skip 4X Enabled

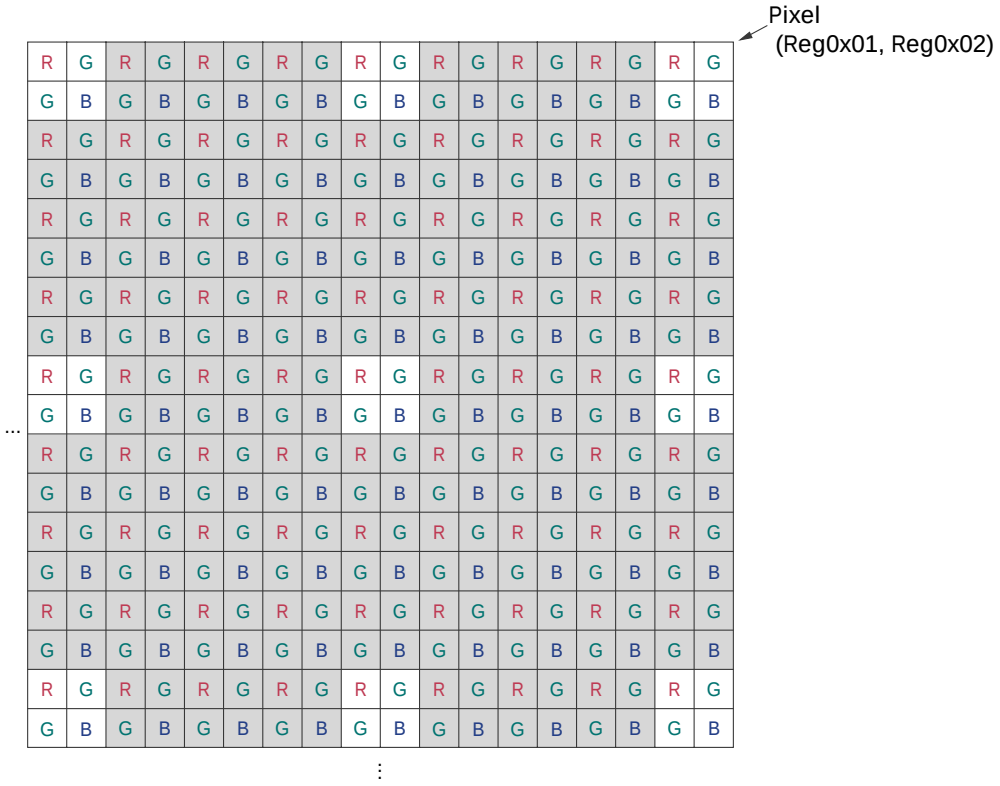


Figure 14: Column Skip 8x; Row Skip 8X Enabled

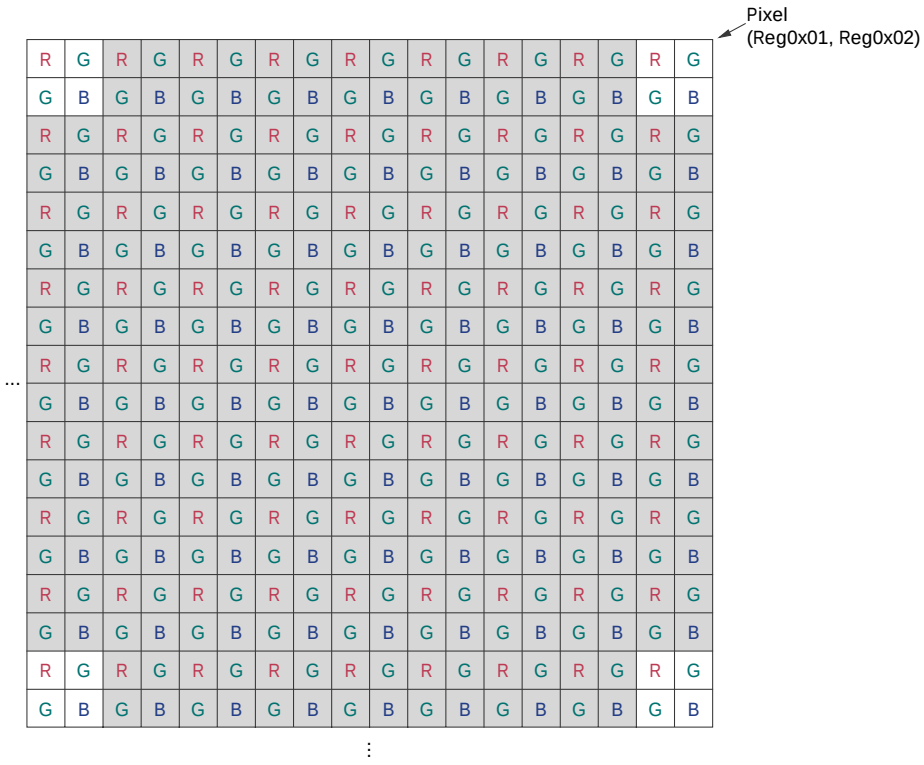
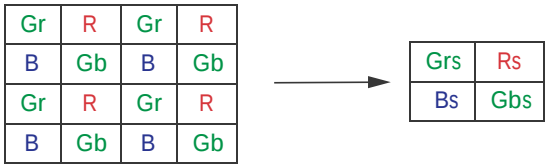
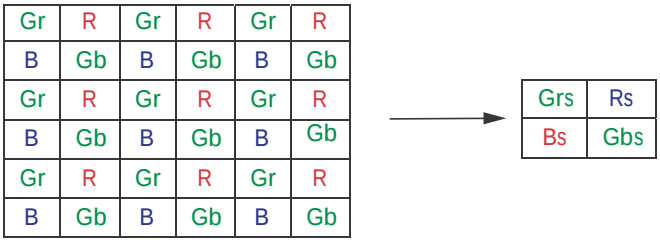


Figure 15: Bin 2-to-1: 2,048H x 1,536V (QXGA) to 1,024H x 768V (XGA)



NOTE:
Grs = binning of 4 Gr[s] in a 4 x 4 window; Gbs = binning of 4 Gb[s] in a 4 x 4 window.
Rs = binning of 4 R[s] in a 4 x 4 window; B[s] = binning of 4 B[s] in a 4 x 4 window.

Figure 16: Bin 3-to-1: 2,048H x 1,536V (QXGA) to 640H x 480V (VGA)



NOTE:
Grs = binning of 9 Gr[s] in a 6 x 6 window; Gbs = binning of 9 Gb[s] in a 6 x 6 window.
Rs = binning of 9 R[s] in a 6 x 6 window; Bs = binning of B[s] in a 6 x 6 window.

Smaller Format Resolution

Reg0x01, Reg0x02, Reg0x03, Reg0x04, Reg0x05, Reg0x06, Reg0x22, and Reg0x23 With the aforementioned flexible windowing capability of the sensor, the user is able to read out different resolution formats from default of QXGA to UXGA, SXGA, XGA, SVGA, VGA, CIF, QVGA, QCIF, etc. Below are some examples of programmable register settings to obtain the estimated frame rates for the desired formats.

The user can change the values of Reg0x05 and Reg0x06 to obtain different frame rates. Note that the field of view of the image will be reduced since the programmed settings effectively reduce the read out window to the specified settings without skipping any rows or columns.

If the user only changes the register settings mentioned above without changing the row and column start address, the read out window would start from that coordinate. To read out the center of the image or any portion that is desired, the user would need to program Reg0x01 and Reg0x02, thus performing electronic panning.

To maintain the same field of view while reducing the read out resolution, the user would need to perform row and column skip. For example, if the desired read out resolution needs to be XGA (1,024H x 7,68V) instead of QXGA (2,048H x 1,536V). To maintain the same field of view, the user can select column skip 2x and row skip 2x modes. This effectively reduces the horizontal and vertical resolution by 2x for a factor of 4x reduction in overall number of pixels that are read out. To perform this read out mode, the user would need to set the following:

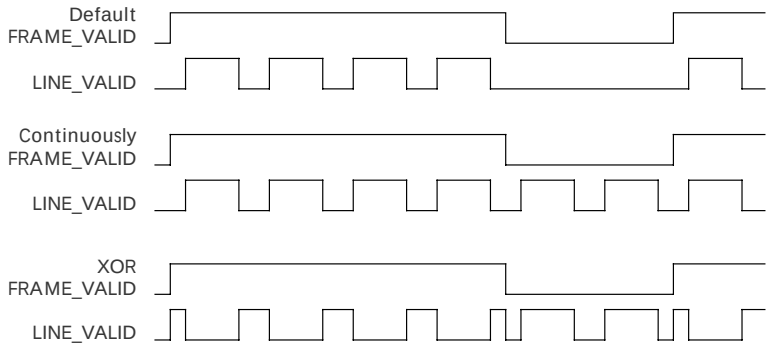
Reg0x03 = 0x05FF	1,536V rows
Reg0x04 = 0x07FF	2,048H columns
Reg0x23 Bit[2:0]=1	Column skip 2x—> 1,024H columns read out
Reg0x22 Bit[2:0] = 1	Row skip 2x —> 768 rows read out

Note that if the user sets Reg0x03 = 0x02FF (768V rows), Reg0x04 = 0x03FF (1,024H columns), and then enable column skip 2x and row skip 2x, the effective readout resolution will be 512H x 384V.

Line_Valid Formats

Reg0x20 is used to control many aspects of the readout of the sensor. By setting Bit 9 and 10 of Reg0x20 the LINE_VALID signal can get three different output formats. The formats are shown in Figure 17 when reading out four rows and two vertical blanking rows. In the last format the LINE_VALID signal is the XOR between the continuously LINE_VALID signal and the FRAME_VALID signal.

Figure 17: Different LINE_VALID Formats



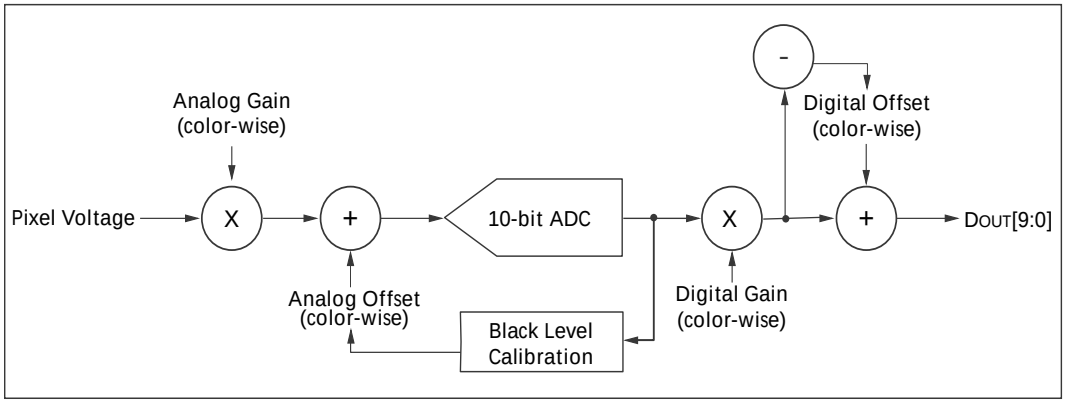
Signal Path

The MT9T001 sensor analog signal path consists of the pixel array, the column sample and hold (S/H) circuitry, the programmable gain stage, the analog offset correction and the analog-to-digital converter (ADC).

The reset and signal voltages from the pixel are sampled onto the column sample and hold circuitry on a row-wise basis. After signal sampling is complete, the differential signal (reset - signal) is transferred to the programmable gain stage.

After the gain stage, the differential signal goes through the analog offset correction circuitry. The user can decide if a positive or negative offset or no offset needs to be added to the differential signal. The signal is then sampled onto the sample and hold circuitry of the ADC before being digitized.

Figure 18: Signal Path



Gain Settings

Reg0x2B, Reg0x2C, Reg0x2D, Reg0x2E, and Reg0x35

The analog programmable gain stage consists of two stages of gain circuitry that operate in a pipelined manner. The first stage of gain has programmable gain of 1 or 2 while the second stage of gain has programmable gain of 1 to 4 with steps of 0.125 for a maximum analog gain of 8. The gain settings can be independently adjusted for the colors of Green1, Blue, Red, and Green2 and are programmed through Reg0x2B, Reg0x2C, Reg0x2D, and Reg0x2E, respectively. The gain may also be adjusted globally through Reg0x35. The first stage of gain is set by Bit(6), while the second stage gain is set by Bit(5-0). The gain is individually controllable for each color in the Bayer pattern as follows:

Analog Gain < = 8:
Gain = (Bit[6] + 1) x (Bit[5:0] x 0.125)
Digital Gain = 1 + Bit[14:8]/8
Total Gain = Analog Gain x Digital Gain

Since Bit[6] of the gain registers are multiplicative factors for the gain settings, there are alternative ways of achieving certain gains. Some settings offer superior noise performance to others, despite the same overall gain, as shown in Table 13.

Table 13: Gain Increment Settings

NOMINAL GAIN	INCREMENTS	RECOMMENDED SETTINGS
1 to 4.000	0.125	0x0008 to 0x0020
4.25 to 8.00	0.25	0x0051 to 0x0060
9.0 to 128.0	1.0	0x0160 to 0x7860

Black Level Calibration

Reg0x5D, and Reg0x5F The digitized black level of the MT9T001 sensor will potentially vary with temperature or gain setting changes. The MT9T001 sensor allows the user the flexibility of automatic black level calibration or manual black level control.

Manual Black Level Calibration

Reg0x60, Reg0x61, Reg0x62, Reg0x63, and Reg0x64

The programmable analog offset stage corrects for analog offset that might be present in the analog signal. The user would need to program Reg0x62 appropriately to enable the analog offset correction. The analog offset settings can be independently adjusted for the colors of Green1, Green2, Red and Blue and are programmed through Reg0x60, Reg0x61, Reg0x63 and Reg0x64 respectively. Note that Bit[8] of Reg0x60, Reg0x61, Reg0x63 and Reg0x64 (these registers have two's complement representation) determines the sign of the analog offset. Bit[8] = 1 makes the analog correction negative instead of positive.

The lower 8 bits (Bit[7:0]) determine the absolute value of the analog offset to be corrected and Bit[8] determines the sign of the correction. When Bit[8] is "1", the sign of the correction is negative and vice versa. The analog value of the correction relative to the analog gain stage can be determined from the following formula:

Analog offset = Bit[8:0] x 1 LSB

Note that the 1 LSB value in the formula is an estimate amount. It will deviate from 1 LSB with process variation.

Black Level

Reg0x49 Digital offset will be applied such that the average black level of a frame in a resulting image equals the value of this register. This adjustment happens after black level calibration.

Reset

This register is used to reset the sensor registers to their default, power-up state. To reset the MT9T001, first write a "1" into bit 0 of this register to put the MT9T001 in reset mode, then write a "0" into bit 0 to resume operation.

Another way to reset the sensor is through the RESET# pin (pin 10) - by pulling the RESET# signal to 0V.

The reset operation is an asynchronous reset and the sensor will remain in reset as long as RESET# signal = 0V. In both methods of reset, the sensor register settings will return to their default states.

Standby Control and Chip Enable

There are two steps required to put the sensor in standby mode:

1. Through the two-wire serial interface program Reg0x07 Bit[1] = 0. This stops the sensor readout and powers down analog circuitry of the sensor. The sensor will stay in standby mode until the user reprograms Reg0x07 Bit[1] = 1.
2. Set STANDBY (pin 7) to HIGH.

Serial Bus Description

Registers are written to and read from the MT9T001 through the two-wire serial interface bus. The MT9T001 is a serial interface slave and is controlled by the serial clock (SCLK), which is driven by the serial interface master. Data is transferred into and out of the MT9T001 through the serial data (SDATA) line. The SDATA line is pulled up to 3.3V off-chip by a 1.5KΩ resistor. Either the slave or master device can pull the SDATA line down—the serial interface protocol determines which device is allowed to pull the SDATA line down at any given time.

Protocol

The two-wire serial defines several different transmission codes, as follows:

- a start bit
- the slave device 8-bit address
- a(n) (no) acknowledge bit
- an 8-bit message
- a stop bit

Sequence

A typical read or write sequence begins by the master sending a start bit. After the start bit, the master sends the slave device's 8-bit address. The last bit of the address determines if the request will be a read or a write, where a “0” indicates a write and a “1” indicates a read. The slave device acknowledges its address by sending an acknowledge bit back to the master.

If the request was a write, the master then transfers the 8-bit register address to which a write should take place. The slave sends an acknowledge bit to indicate that the register address has been received. The master then transfers the data eight bits at a time, with the slave sending an acknowledge bit after each eight bits. The MT9T001 uses 16-bit data for its internal registers, thus requiring two 8-bit transfers to write to one register. After 16 bits are transferred, the register address is automatically incremented, so that the next 16 bits are written to the next register address. The master stops writing by sending a start or stop bit.

A typical read sequence is executed as follows. First the master sends the write-mode slave address and 8-bit register address, just as in the write request. The master then sends a start bit and the read-mode slave address. The master then clocks out the register data eight bits at a time. The master sends an acknowledge bit after each 8-bit transfer. The register address is auto-incremented after every 16 bits is transferred. The data transfer is stopped when the master sends a no-acknowledge bit.

Bus Idle State

The bus is idle when both the data and clock lines are HIGH. Control of the bus is initiated with a start bit, and the bus is released with a stop bit. Only the master can generate the start and stop bits.

Start Bit

The start bit is defined as a HIGH-to-LOW transition of the data line while the clock line is HIGH.

Stop Bit

The stop bit is defined as a LOW-to-HIGH transition of the data line while the clock line is HIGH.

Slave Address

The eight-bit address of a two-wire serial interface device consists of seven bits of address and 1 bit of direction. A “0” (0xBA) in the LSB (least significant bit) of the address indicates write mode, and a “1” (0xBB) indicates read mode.

Data Bit Transfer

One data bit is transferred during each clock pulse. The serial interface clock pulse is provided by the master. The data must be stable during the HIGH period of the two-wire serial interface clock—it can only change when the serial clock is LOW. Data is transferred eight bits at a time, followed by an acknowledge bit.

Acknowledge Bit

The master generates the acknowledge clock pulse. The transmitter (which is the master when writing, or the slave when reading) releases the data line, and the receiver indicates an acknowledge bit by pulling the data line LOW during the acknowledge clock pulse.

No-Acknowledge Bit

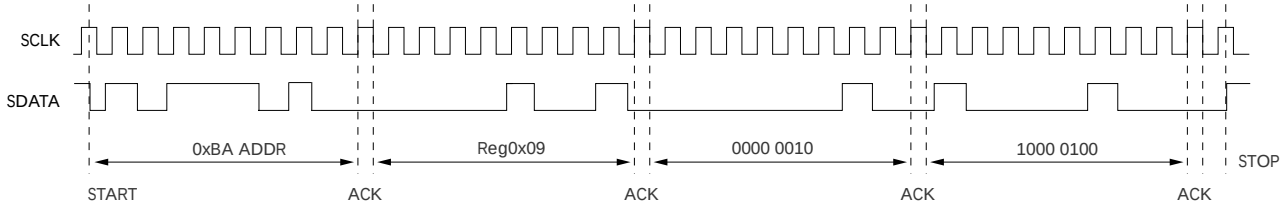
The no-acknowledge bit is generated when the data line is not pulled down by the receiver during the acknowledge clock pulse. A no-acknowledge bit is used to terminate a read sequence.

Two-Wire Serial Interface Sample Write and Read Sequences

16-Bit Write Sequence

A typical write sequence for writing 16 bits to a register is shown in Figure 19. A start bit given by the master, followed by the write address, starts the sequence. The image sensor will then give an acknowledge bit and expects the register address to come first, followed by the 16-bit data. After each eight-bit transfer, the image sensor will give an acknowledge bit. All 16 bits must be written before the register will be updated. After 16 bits are transferred, the register address is automatically incremented so that the next 16 bits are written to the next register. The master stops writing by sending a start or stop bit.

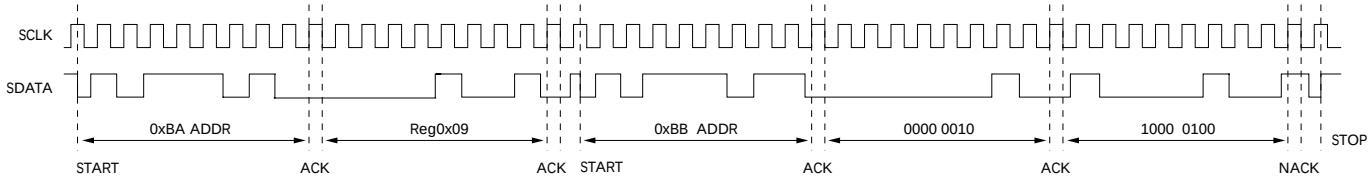
Figure 19: Timing Diagram Showing a Write to Reg0x09 with the Value 0x0284



16-Bit Read Sequence

A typical read sequence is shown in Figure 20. First the master has to write the register address, as in a write sequence. Then a start bit and the read address specifies that a read is about to happen from the register. The master then clocks out the register data eight bits at a time. The master sends an acknowledge bit after each eight-bit transfer. The register address should be incremented after every 16 bits is transferred. The data transfer is stopped when the master sends a no-acknowledge bit.

Figure 20: Timing Diagram Showing a Read from Reg0x09; Returned Value 0x0284



Electrical Specifications

Table 14: DC Electrical Characteristics

(V_{PWR} = 3.3 ±0.3V; T_A = 25°C)

SYMBOL	DEFINITION	CONDITION	MIN	TYP	MAX	UNITS
V_{IH}	Input High Voltage		V_{PWR} - 0.3		V_{PWR} + 0.3	V
V_{IL}	Input Low Voltage		-0.3		0.8	V
I_{IN}	Input Leakage Current	No Pull-up Resistor; V_{IN} = V_{PWR} or V_{GND}	-15		15	µA
V_{OH}	Output High Voltage		V_{PWR} - 0.2			V
V_{OL}	Output Low Voltage			0.0	0.2	V
I_{OZ}	Tri-state Output Leakage Current				15	µA
$I_{PWR}A$	Analog Quiescent Supply Current	Default settings	TBD	50	TBD	mA
$I_{PWR}D$	Digital Quiescent Supply Current	CLKIN = 48 MHz; default setting, C_{LOAD} = 10pF		22		mA
$I_{PWR}A$ Standby	Analog Standby Supply Current	STDBY = V_{DD}	TBD	TBD	TBD	µA
$I_{PWR}D$ Standby	Digital Standby Supply Current	STDBY = V_{DD}, CLKIN = 0 MHz	TBD	TBD	TBD	µA
$I_{PWR}D$ Standby ClkOn	Digital Standby Supply Current with Clock On	STDBY = V_{DD}, CLKIN = 48 MHz	TBD	TBD	TBD	µA

Table 15: AC Electrical Characteristics

(V_{PWR} = 3.3 ±0.3V; T_A = 25°C; CLKIN at 48 MHz)

SYMBOL	DEFINITION	CONDITION	MIN	TYP	MAX	UNITS
FCLK_IN	Input Clock Frequency Clock		1		48	MHz
	Duty Cycle		45		55	%
t_R	Input Clock Rise Time		TBD	TBD	TBD	ns
t_F	Input Clock Fall Time		TBD	TBD		ns
t_{PLHP}	CLKIN to PIXCLK propagation delay, LOW-to-HIGH	C_{LOAD} = 10pF	4	5	6	ns
t_{PHLP}	CLKIN to PIXCLK propagation delay, HIGH-to-LOW	C_{LOAD} = 10pF	6	7	8	ns
t_{PLHD}	CLKIN to D_{OUT}<9-0> propagation delay, LOW-to-HIGH	C_{LOAD} = 10pF		TBD		
t_{PHLD}	CLKIN to D_{OUT}<9-0> propagation delay, HIGH-to-LOW	C_{LOAD} = 10pF		TBD		
t_{OH}	Data Hold Time			TBD		
$t_{PLHF,L}$	CLKIN to FRAME_VALID and LINE_VALID propagation, LOW-to-HIGH		TBD	TBD	TBD	ns
$t_{PHLF,L}$	CLKIN to FRAME_VALID and LINE_VALID propagation, HIGH-to-LOW		TBD	TBD	TBD	ns

Propagation Delay for FRAME_VALID and LINE_VALID Signals

The FRAME_VALID and LINE_VALID signals change on the same falling master clock edge as the data output. The LINE_VALID goes HIGH on the same rising master clock edge as the output of the first valid pixel's data and returns LOW on the same master clock rising edge as the end of the output of the last valid pixel's data.

The typical output delay, relative to the master clock edge, is TBD. Note that the data outputs change on the rising edge of the master clock.

Figure 21: Propagation Delays for FRAME_VALID and LINE_VALID Signals

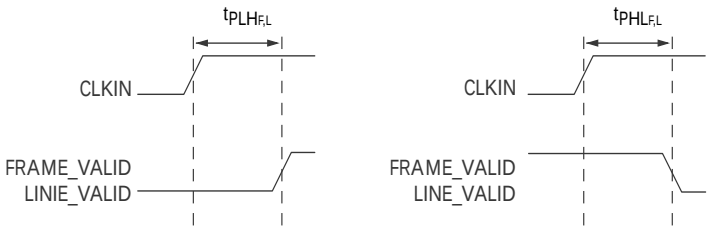
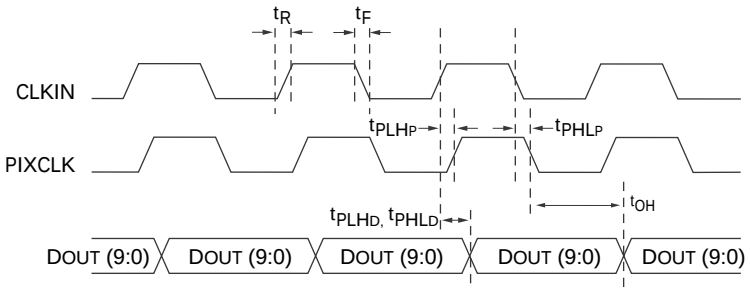


Figure 22: Propagation Delays for PIXCLK and Data Out Signals



Two-Wire Serial Bus Timing

The two-wire serial bus operation requires certain minimum master clock cycles between transitions. These are specified in the following diagrams in master clock cycles.

Figure 23: Serial Host Interface Start Condition Timing

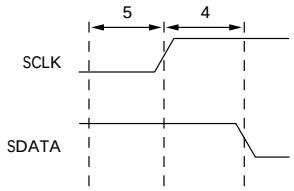
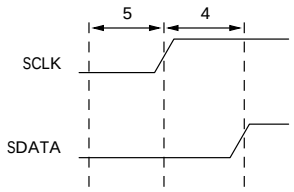
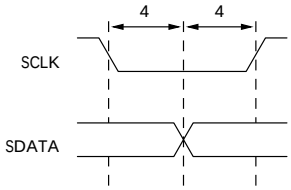


Figure 24: Serial Host Interface Stop Condition Timing



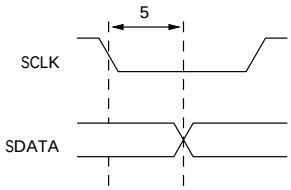
NOTE:
All timing are in units of master clock cycle.

Figure 25: Serial Host Interface Data Timing for Write



NOTE:
SDATA is driven by an off-chip transmitter.

Figure 26: Serial Host Interface Data Timing for Read



NOTE:
SDATA is pulled LOW by the sensor, or allowed to be pulled HIGH by a pull-up resistor off-chip.

Figure 27: Acknowledge Signal Timing After an 8-Bit Write to the Sensor

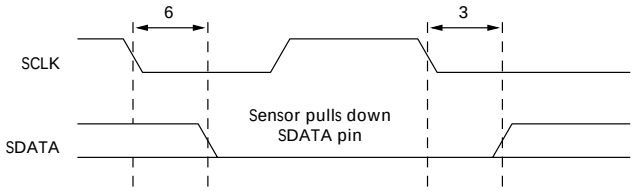
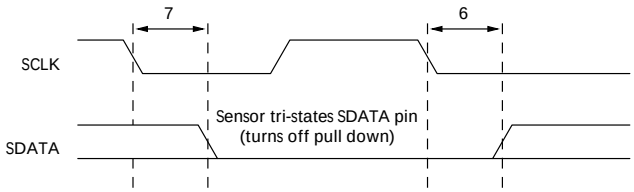
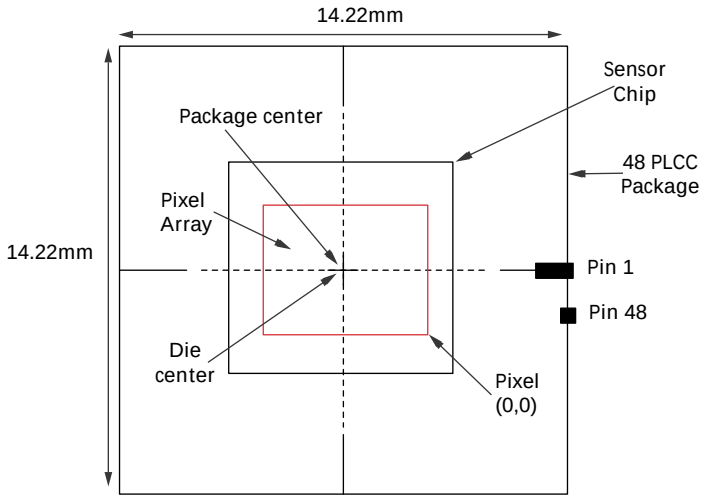


Figure 28: Acknowledge Signal Timing After an 8-Bit Read from the Sensor



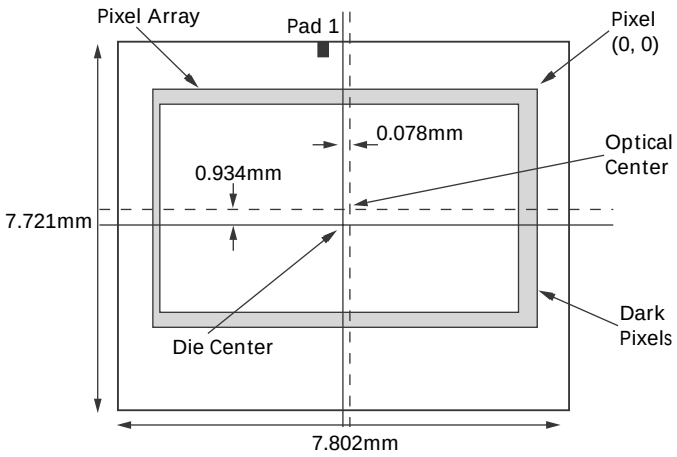
NOTE:
After a read, the master receiver must pull down SDATA to acknowledge receipt of data bits. When read sequence is complete, the master must generate a no acknowledge by leaving SDATA to float HIGH. On the following cycle, a start or stop bit may be used.

Figure 29: Die Placement



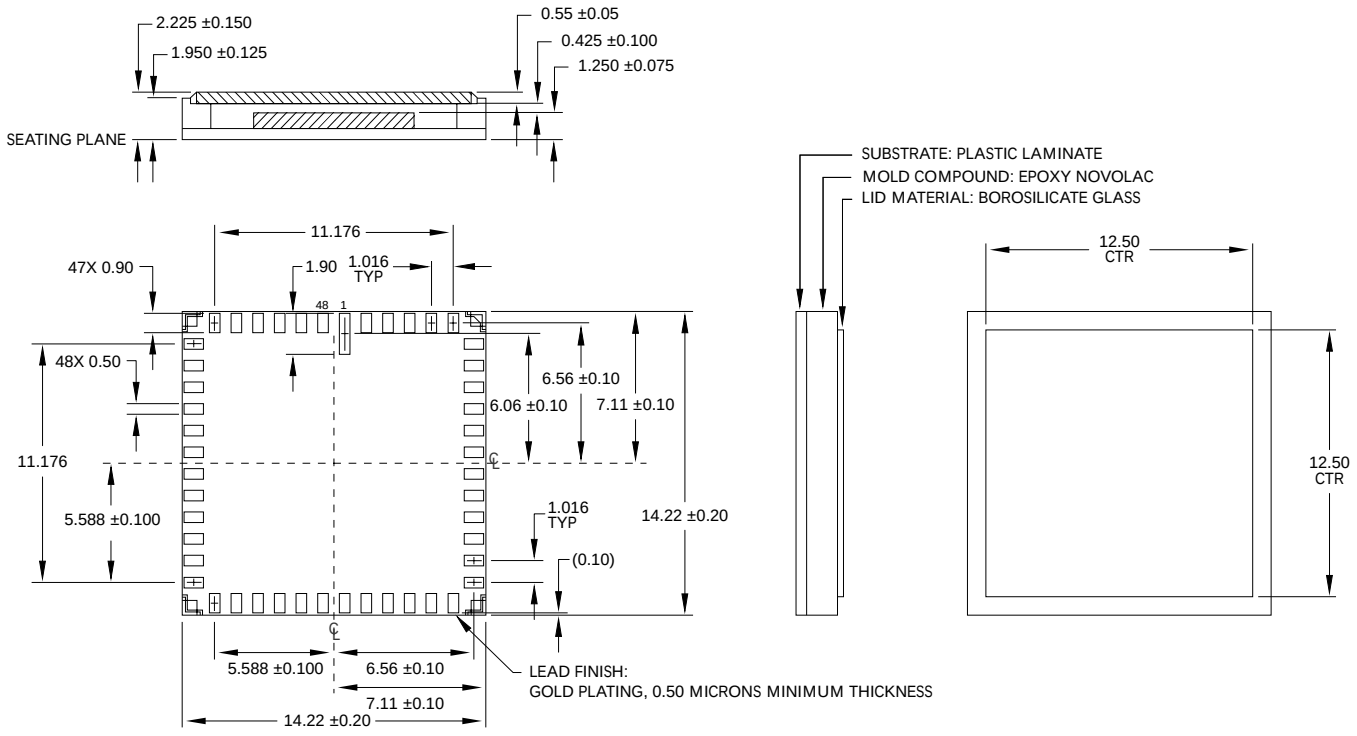
Package Center = Die Center

Figure 30: Image Center Offset



NOTE: Diagrams are not to scale.

Figure 31: 48-Pin PLCC



Data Sheet Designation

Preliminary: This data sheet contains initial characterization limits that are subject to change upon full characterization of production devices.

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Revision History

Rev C, Preliminary 9/04

- Added Applications
- Updated Image Center Offset, Figure 30

Rev B, Preliminary 3/04

- Updated Figure 29
- Added Table 1
- Updated Tables 2, 4, 5, and 6

Rev A, Version 1.0, Preliminary 12/03

- Initial Release of document