

# Synchronous DRAM Module

MT9LSDT872 – 64MB  
MT9LSDT1672 – 128MB  
MT9LSDT3272 – 256MB

For the latest data sheet, refer to Micron's Web site: [www.micron.com/products/modules](http://www.micron.com/products/modules)

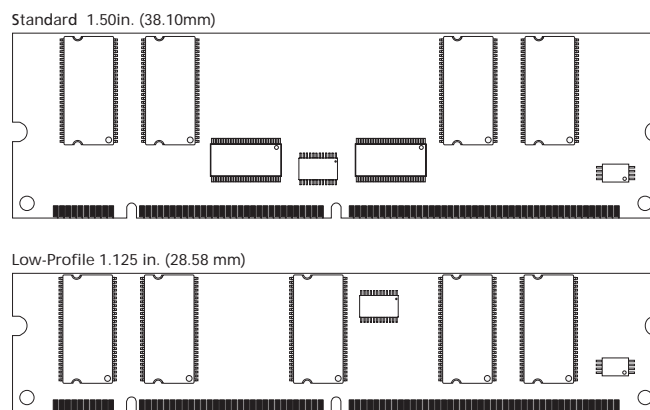
## Features

- 168-pin, dual in-line memory module (DIMM)
- PC133-compliant
- Registered inputs with one-clock delay
- Phase-lock loop (PLL) clock driver to reduce loading
- Utilizes 133 MHz SDRAM components
- Supports ECC error detection and correction
- 64MB (8 Meg x 72), 128MB (16 Meg x 72), and 256MB (32 Meg x 72)
- Single +3.3V power supply
- Fully synchronous; all signals registered on positive edge of PLL clock
- Internal pipelined operation; column address can be changed every clock cycle
- Internal SDRAM banks for hiding row access/precharge
- Programmable burst lengths: 1, 2, 4, 8, or full page
- Auto precharge, includes concurrent auto precharge; auto refresh mode
- Self refresh mode: 64ms, 4,096-cycle refresh (64MB, 128MB); 8,192 cycle refresh (256MB)
- LVTTL-compatible inputs and outputs
- Serial presence-detect (SPD)
- Gold edge contacts

**Table 1: Timing Parameters**  
CL = CAS (READ) latency

Module Marking	Clock Frequency	Access Time		Setup Time	Hold Time
		CL = 2	CL = 3		
-13E	133 MHz	5.4ns	–	1.5ns	0.8ns
-133	133 MHz	–	5.4ns	1.5ns	0.8ns

**Figure 1: 168-Pin DIMM (MO-161)**



## Options

- Package
  - 168-pin DIMM (standard) G
  - 168-pin DIMM (lead-free) Y<sup>1</sup>
- Frequency/CAS Latency<sup>2</sup>
  - 133 MHz (7.5ns) / CL = 2 -13E
  - 133 MHz (7.5ns) / CL = 3 -133
- PCB
  - Standard 1.50in. (38.10mm) See note page 2
  - Low-Profile 1.125in. (28.58mm) See note page 2

## Marking

- Notes:1. Contact Micron for product availability.  
2. Registered mode will add one clock cycle to CL.



## 64MB, 128MB, 256MB (x72, ECC, SR): 168-PIN SDRAM RDIMM Features

**Table 2: Address Table**

Parameter	64MB	128MB	256MB
Refresh count	4K	4K	8K
Device banks	4 (BA0, BA1)	4 (BA0, BA1)	4 (BA0, BA1)
Device configuration	64Mb (8 Meg x 8)	128Mb (16 Meg x 8)	256Mb (32 Meg x 8)
Device row addressing	4K (A0–A11)	4K (A0–A11)	8K (A0–A12)
Device column addressing	512 (A0–A8)	1K (A0–A9)	1K (A0–A9)
Module ranks	1 (S0#, S2#)	1 (S0#, S2#)	1 (S0#, S2#)

**Table 3: Part Numbers**

Part Number	Module Density	Configuration	System Bus Speed
MT9LSDT872G-13E__	64MB	8 Meg x 72	133 MHz
MT9LSDT872Y-13E__	64MB	8 Meg x 72	133 MHz
MT9LSDT872G-133__	64MB	8 Meg x 72	133 MHz
MT9LSDT872Y-133__	64MB	8 Meg x 72	133 MHz
MT9LSDT1672G-133__	128MB	16 Meg x 72	133 MHz
MT9LSDT1672Y-133__	128MB	16 Meg x 72	133 MHz
MT9LSDT1672G-13E__	128MB	16 Meg x 72	133 MHz
MT9LSDT1672Y-13E__	128MB	16 Meg x 72	133 MHz
MT9LSDT3272G-133__	256MB	32 Meg x 72	133 MHz
MT9LSDT3272Y-133__	256MB	32 Meg x 72	133 MHz
MT9LSDT3272G-13E__	256MB	32 Meg x 72	133 MHz
MT9LSDT3272Y-13E__	256MB	32 Meg x 72	133 MHz

Note: All part numbers end with a two-place code (not shown), designating component and PCB revisions. Consult factory for current revision codes. Example: MT9LSDT1672G-133B1.

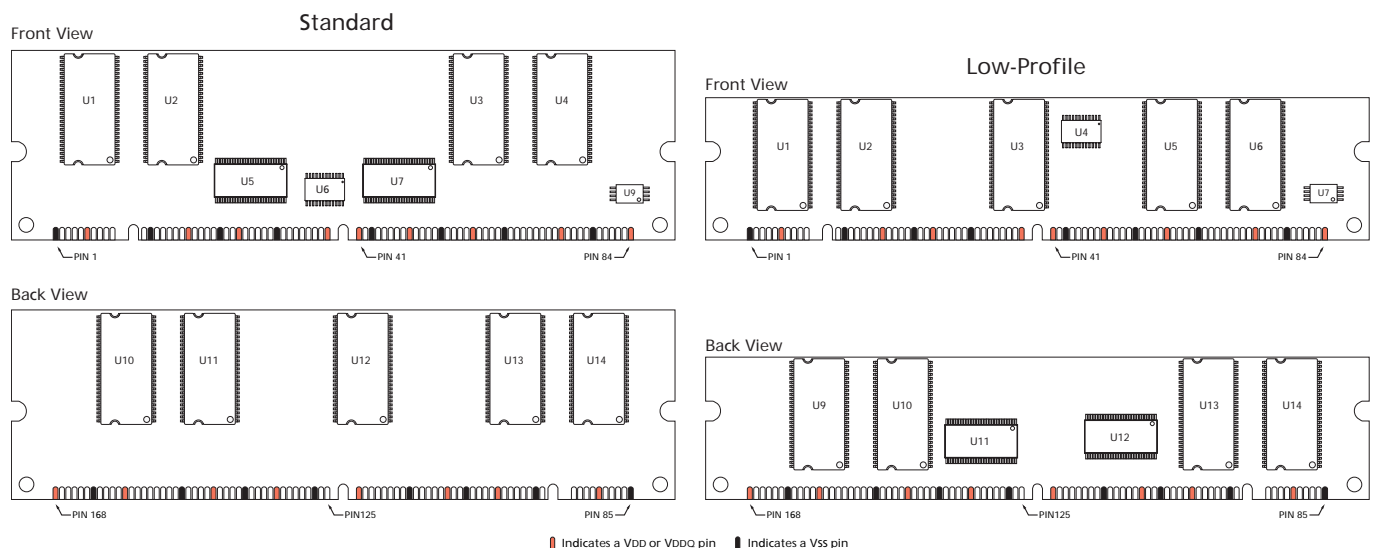
### Pin Assignments and Descriptions

**Table 4: Pin Assignments**

168-Pin DIMM (Front)								168-Pin DIMM (Back)							
Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
1	Vss	22	CB1	43	Vss	64	Vss	85	Vss	106	CB5	127	Vss	148	Vss
2	DQ0	23	Vss	44	DNU	65	DQ21	86	DQ32	107	Vss	128	CKE0	149	DQ53
3	DQ1	24	NC	45	S2#	66	DQ22	87	DQ33	108	NC	129	RFU (S3#)	150	DQ54
4	DQ2	25	NC	46	DQMB2	67	DQ23	88	DQ34	109	NC	130	DQMB6	151	DQ55
5	DQ3	26	VDD	47	DQMB3	68	Vss	89	DQ35	110	VDD	131	DQMB7	152	Vss
6	VDD	27	WE#	48	DNU	69	DQ24	90	VDD	111	CAS#	132	RFU (A13)	153	DQ56
7	DQ4	28	DQMB0	49	VDD	70	DQ25	91	DQ36	112	DQMB4	133	VDD	154	DQ57
8	DQ5	29	DQMB1	50	NC	71	DQ26	92	DQ37	113	DQMB5	134	NC	155	DQ58
9	DQ6	30	S0#	51	NC	72	DQ27	93	DQ38	114	NC	135	NC	156	DQ59
10	DQ7	31	DNU	52	CB2	73	VDD	94	DQ39	115	RAS#	136	CB6	157	VDD
11	DQ8	32	Vss	53	CB3	74	DQ28	95	DQ40	116	Vss	137	CB7	158	DQ60
12	Vss	33	A0	54	Vss	75	DQ29	96	Vss	117	A1	138	Vss	159	DQ61
13	DQ9	34	A2	55	DQ16	76	DQ30	97	DQ41	118	A3	139	DQ48	160	DQ62
14	DQ10	35	A4	56	DQ17	77	DQ31	98	DQ42	119	A5	140	DQ49	161	DQ63
15	DQ11	36	A6	57	DQ18	78	Vss	99	DQ43	120	A7	141	DQ50	162	Vss
16	DQ12	37	A8	58	DQ19	79	CK2	100	DQ44	121	A9	142	DQ51	163	CK3
17	DQ13	38	A10	59	VDD	80	NC	101	DQ45	122	BA0	143	VDD	164	NC
18	VDD	39	BA1	60	DQ20	81	WP	102	VDD	123	A11	144	DQ52	165	SA0
19	DQ14	40	VDD	61	NC	82	SDA	103	DQ46	124	VDD	145	NC	166	SA1
20	DQ15	41	VDD	62	NC	83	SCL	104	DQ47	125	CK1	146	NC	167	SA2
21	CB0	42	CK0	63	NC	84	VDD	105	CB4	126	NC/A12 <sup>1</sup>	147	REGE	168	VDD

Notes: 1. Pin 126 is NC (64MB and 128MB) or A12 (256MB).

**Figure 2: 168-Pin DIMM Pin Locations**



**Table 5: Pin Descriptions**

Pin numbers may not correlate with symbols; refer to Table 4 on page 3 for more information

Pin Numbers	Symbol	Type	Description
27, 111, 115	WE#, CAS#, RAS#	Input	Command inputs: RAS#, CAS#, and WE# (along with S#) define the command being entered.
42, 79, 125, 163	CK0–CK3	Input	Clock: CK is driven by the system clock. All SDRAM input signals are sampled on the positive edge of CK. CK also increments the internal burst counter and controls the output registers.
128	CKE0	Input	Clock enable: CKE activates (HIGH) and deactivates (LOW) the CK signal. Deactivating the clock provides PRECHARGE, POWER-DOWN, and SELF REFRESH operation (all device banks idle), ACTIVE POWER-DOWN (row ACTIVE in any device bank), or CLOCK SUSPEND operation (burst access in progress). CKE is synchronous except after the device enters power-down and self refresh modes, where CKE becomes asynchronous until after exiting the same mode. The input buffers, including CK, are disabled during power-down and self refresh modes, providing low standby power.
30, 45	S0#, S2#	Input	Chip select: S# enable (registered LOW) and disable (registered HIGH) the command decoder. All commands are masked when S# are registered HIGH. S# are considered part of the command code.
28-29, 46-47, 112-113, 130-131	DQMB0–DQMB7	Input	Input/Output mask: DQMB is an input mask signal for write accesses and an output enable signal for read accesses. Input data is masked when DQMB is sampled HIGH during a WRITE cycle. The output buffers are placed in a High-Z state (two-clock latency) when DQMB is sampled HIGH during a READ cycle.
39, 122	BA0, BA1	Input	Bank address: BA0 and BA1 define to which bank the ACTIVE, READ, WRITE or PRECHARGE command is being applied.
33, 34, 35, 36, 37, 38, 117, 118, 119, 120, 121, 123, 126 (256MB)	A0–A11 (64MB, 128MB) A0–A12 (256MB)	Input	Address inputs: Sampled during the ACTIVE command and READ/WRITE command, with A10 defining auto precharge) to select one location out of the memory array in the respective device bank. A10 is sampled during a PRECHARGE command to determine if both device banks are to be precharged (A10 HIGH). The address inputs also provide the op-code during a LOAD MODE REGISTER command.
83	SCL	Input	Serial clock for presence-detect: SCL is used to synchronize the presence-detect data transfer to and from the module.
165–167	SA0–SA2	Input	Presence-Detect address inputs: These pins are used to configure the presence-detect device.
147	REGE	Input	Register enable.
2–5, 7–11, 13–17, 19–20, 55–58, 60, 65–67, 69–72, 74–77, 86–89, 91–95, 97–101, 103–104, 139–142, 144, 149–151, 153–156, 158–161	DQ0–DQ63	Input/Output	Data I/Os: Data bus.
21–22, 52–53, 105–106, 136–137	CB0–CB7	Input/Output	Check bits.
8 2	SDA	Input/Output	Serial presence-detect data: SDA is a bidirectional pin used to transfer addresses and data into and data out of the presence-detect portion of the module.
6, 18, 26, 40–41, 49, 59, 73, 84, 90, 102, 110, 124, 133, 143, 157, 168	VDD	Supply	Power supply: +3.3V ±0.3V.



**Table 5: Pin Descriptions**

Pin numbers may not correlate with symbols; refer to Table 4 on page 3 for more information

Pin Numbers	Symbol	Type	Description
1, 12, 23, 32, 43, 54, 64, 68, 78, 85, 96, 107, 116, 127, 138, 148, 152, 162	VSS	Supply	Ground.
63, 81, 114, 126 (64MB, 128MB), 129, 132	NC	–	Reserved for future use: These pins are not connected on this module but are assigned pins on other SDRAM versions.
31, 44, 48	DNU	–	Do not use: These pins are not connected on this module but are assigned pins on the compatible DRAM version.

## Functional Block Diagrams

Per industry standard, Micron utilizes various component speed grades as referenced in the Module Part Numbering Guide at [www.micron.com/support/numbering.html](http://www.micron.com/support/numbering.html).

### Standard PCB

Standard modules use the following SDRAM devices: MT48LC8M8A2TG (64MB); MT48LC16M8A2TG (128MB); and MT46LC32M8A2TG (256MB).

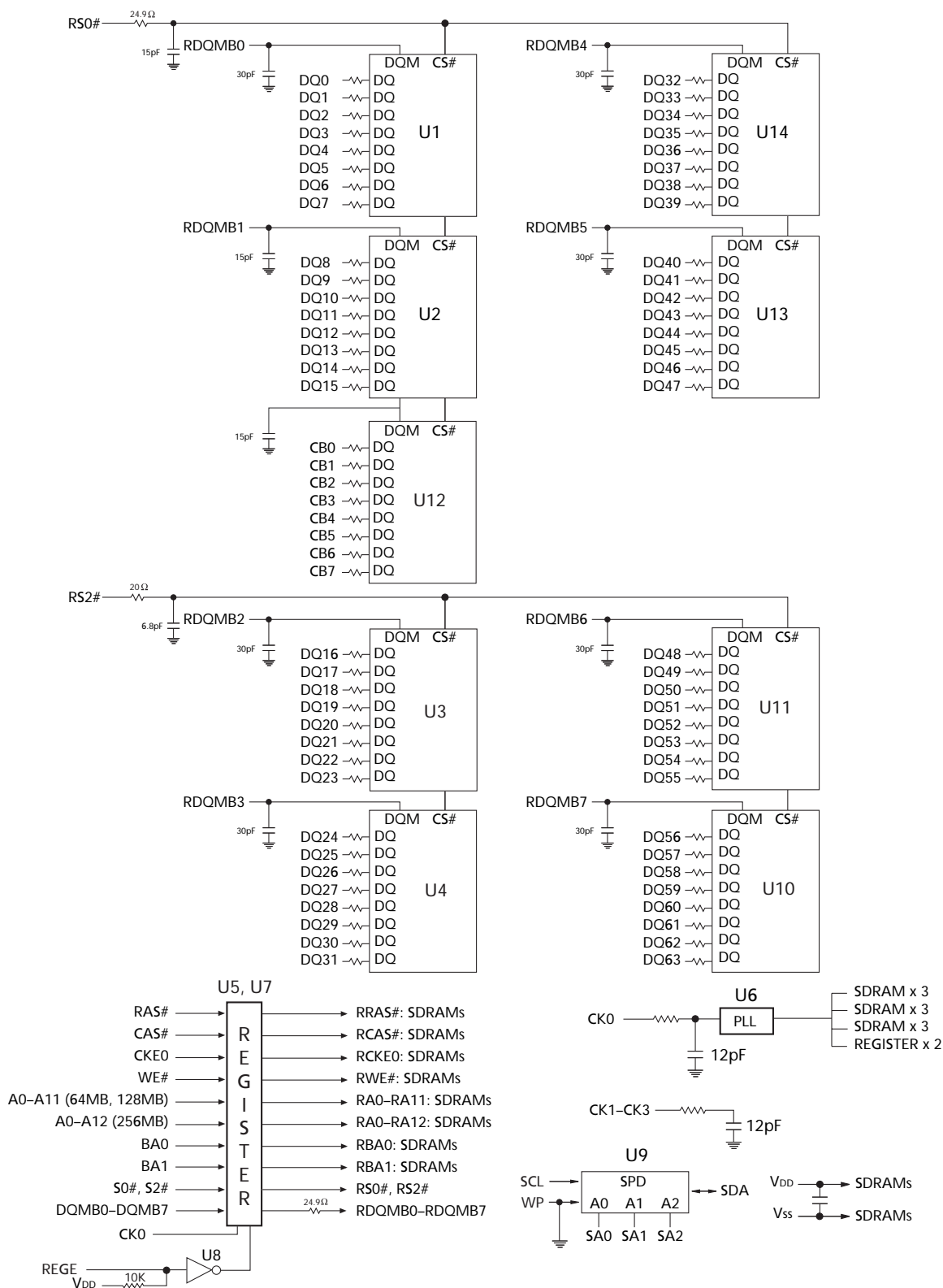
Lead-free modules use the following SDRAM devices: MT48LC8M8A2P (64MB); MT48LC16M8A2P (128MB); and MT46LC32M8A2P (256MB).

### Low-Profile PCB

Standard modules use the following SDRAM devices: MT48LC16M8A2TG (64MB); MT48LC32M8A2TG (128MB); and MT46LC64M8A2TG (256MB).

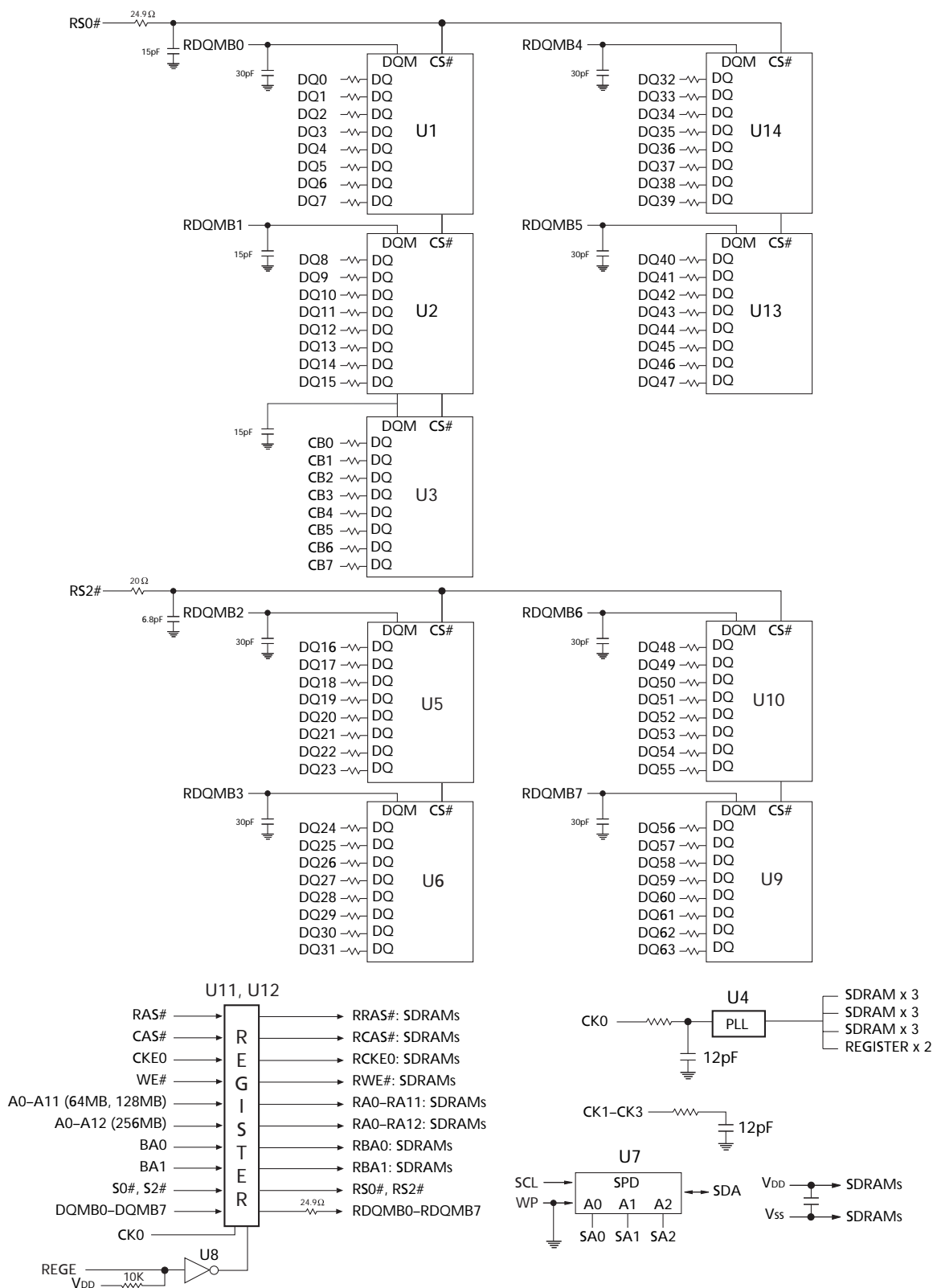
Lead-free modules use the following SDRAM devices: MT48LC16M8A2P (64MB); MT48LC32M8A2P (128MB); and MT46LC64M8A2P (256MB).

**Figure 3: Standard PCB**



Note: All resistor values are 10Ω unless otherwise specified.

**Figure 4: Low-Profile PCB**



Note: All resistor values are 10Ω unless otherwise specified.

## General Description

The Micron MT9LSDT872, MT9LSDT1672, and MT9LSDT3272 are high-speed CMOS, dynamic random-access, 64MB, 128MB, and 256MB modules organized in a x72 configuration. SDRAM modules use internally configured quad-bank SDRAM devices with a synchronous interface (all signals are registered on the positive edge of clock signals CK).

Read and write accesses to SDRAM modules are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an ACTIVE command, which is then followed by a READ or WRITE command. The address bits registered coincident with the ACTIVE command are used to select the bank and row to be accessed (BA0, BA1 select the bank, A0–A11 [64MB and 128MB] or A0–A12 [256MB] select the row). The address bits registered coincident with the READ or WRITE command are used to select the starting column location for the burst access.

SDRAM modules provide for programmable read or write BL of 1, 2, 4 or 8 locations, or full page, with a burst terminate option. An AUTO PRECHARGE function may be enabled to provide a self-timed row precharge that is initiated at the end of the burst sequence.

SDRAM modules use an internal pipelined architecture to achieve high-speed operation. This architecture is compatible with the  $2n$  rule of prefetch architectures, but it also allows the column address to be changed on every clock cycle to achieve a high-speed, fully random access. Precharging one bank while accessing one of the other three banks will hide the PRECHARGE cycles and provide seamless, high-speed, random-access operation.

SDRAM modules are designed to operate in 3.3V, low-power memory systems. An auto refresh mode is provided, along with a power-saving, power-down mode. All inputs and outputs are LVTTTL-compatible.

SDRAM modules offer substantial advances in DRAM operating performance, including the ability to synchronously burst data at a high data rate with automatic column-address generation, the ability to interleave between internal banks in order to hide pre-charge time, and the capability to randomly change column addresses on each clock cycle during a burst access. For more information regarding SDRAM operation, refer to the 64Mb, 128Mb, or 256Mb SDRAM component data sheets.

## PLL and Register Operation

These modules can be operated in either registered mode (REGE pin HIGH), where the control/address input signals are latched in the register on one rising clock edge and sent to the SDRAM devices on the following rising clock edge (data access is delayed by one clock), or in buffered mode (REGE pin LOW) where the input signals pass through the register/buffer to the SDRAM devices on the same clock. A phase-lock loop (PLL) on the modules is used to redrive the clock signals to the SDRAM devices to minimize system clock loading (CK0 is connected to the PLL, and CK1, CK2 and CK3 are terminated).

## Serial Presence-Detect Operation

SDRAM modules incorporate serial presence-detect (SPD). The SPD function is implemented using a 2,048-bit EEPROM. This nonvolatile storage device contains 256 bytes. The first 128 bytes can be programmed by Micron to identify the module type and various SDRAM organizations and timing parameters. The remaining 128 bytes of storage are available for use by the customer. System READ/WRITE operations between the master (system logic) and the slave EEPROM device (DIMM) occur via a standard I<sup>2</sup>C



bus using the DIMM's SCL (clock) and SDA (data) signals, together with SA(2:0), which provide eight unique DIMM/EEPROM addresses. Write protect (WP) is tied to ground on the module, permanently disabling hardware write protect.

## Initialization

SDRAMs must be powered up and initialized in a predefined manner. Operational procedures other than those specified may result in undefined operation. Once power is applied to VDD and VDDQ (simultaneously) and the clock is stable (stable clock is defined as a signal cycling within timing constraints specified for the clock pin), the SDRAM requires a 100 $\mu$ s delay prior to issuing any command other than a COMMAND INHIBIT or NOP. Starting at some point during this 100 $\mu$ s period and continuing at least through the end of this period, COMMAND INHIBIT or NOP commands should be applied.

Once the 100 $\mu$ s delay has been satisfied with at least one COMMAND INHIBIT or NOP command having been applied, a PRECHARGE command should be applied. All device banks must then be precharged, thereby placing the device in the all banks idle state.

Once in the idle state, two AUTO REFRESH cycles must be performed. After the AUTO REFRESH cycles are complete, the SDRAM is ready for mode register programming. Because the mode register will power up in an unknown state, it should be loaded prior to applying any operational command.

## Mode Register Definition

The mode register is used to define the specific mode of operation of the SDRAM. This definition includes the selection of BL, a burst type, CL, an operating mode, and a write burst mode, as shown in Figure 5 on page 10.

The mode register is programmed via the LOAD MODE REGISTER command and will retain the stored information until it is programmed again or the device loses power.

Mode register bits M0–M2 specify BL, M3 specifies the type of burst (sequential or interleaved), M4–M6 specify CL, M7 and M8 specify the operating mode, M9 specifies the write burst mode, and M10 and M11 are reserved for future use.

The mode register must be loaded when all device banks are idle, and the controller must wait the specified time before initiating the subsequent operation. Violating either of these requirements will result in unspecified operation.

## Burst Length

Read and write accesses to the SDRAM are burst oriented, with BL being programmable, as shown in Figures 5. BL determines the maximum number of column locations that can be accessed for a given READ or WRITE command. BL of 1, 2, 4, or 8 locations are available for both the sequential and the interleaved burst types, and a full-page burst is available for the sequential type. The full-page burst is used in conjunction with the BURST TERMINATE command to generate arbitrary BL.

Reserved states should not be used, as unknown operation or incompatibility with future versions may result.

When a READ or WRITE command is issued, a block of columns equal to the BL is effectively selected. All accesses for that burst take place within this block, meaning that the burst will wrap within the block if a boundary is reached, as shown in Table 6 on page 11. The block is uniquely selected by A1–Ai when BL = 2; by A2–Ai when BL = 4; and by A3–Ai when BL = 8. See note 8 of Table 6, for Ai values. The remaining (least significant) address bit(s) is (are) used to select the starting location within the block. Full-page bursts wrap within the page if the boundary is reached, as shown in Table 6.

**Figure 5: Mode Register Definition**

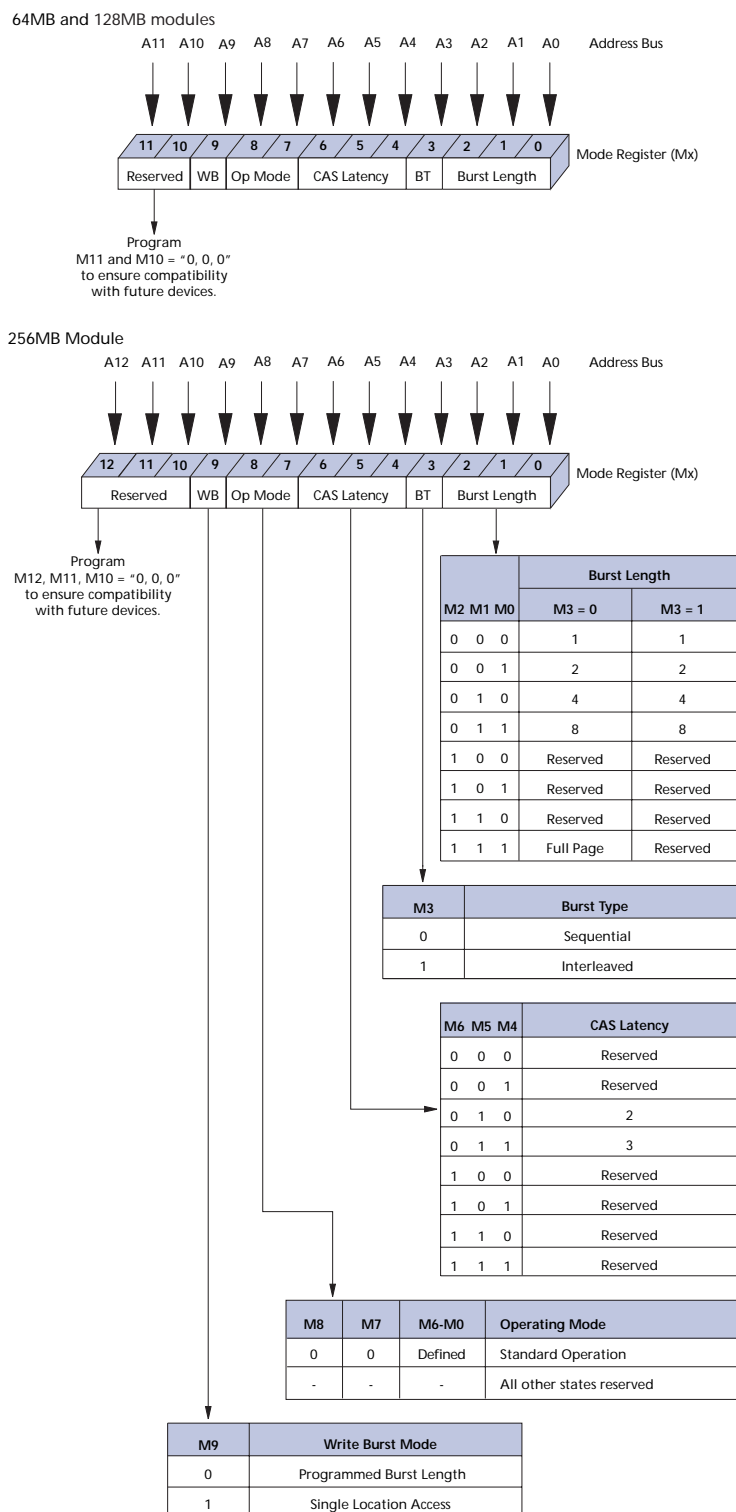
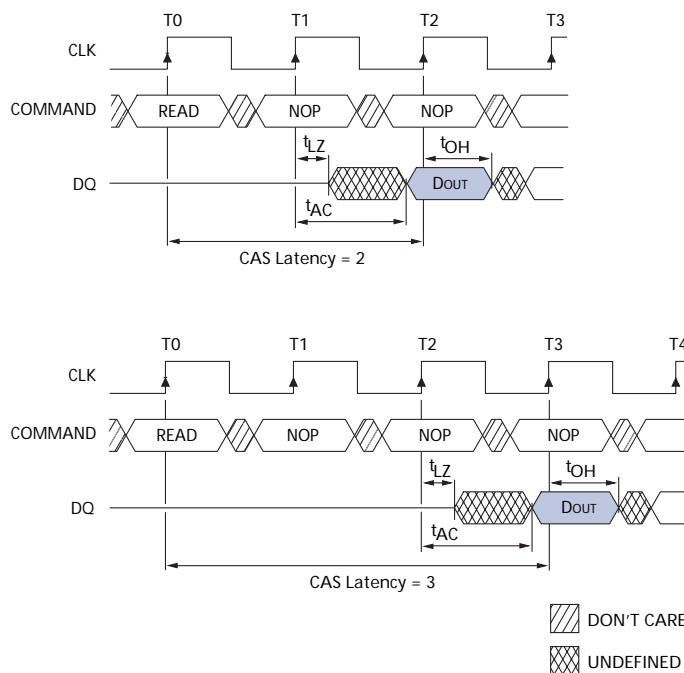


Table 6: Burst Definition

Burst Length	Starting Column Address	Order of Accesses Within a Burst	
		Type = Sequential	Type = Interleaved
2	A0		
	0	0-1	0-1
	1	1-0	1-0
4	A1 A0		
	0 0	0-1-2-3	0-1-2-3
	0 1	1-2-3-0	1-0-3-2
	1 0	2-3-0-1	2-3-0-1
	1 1	3-0-1-2	3-2-1-0
8	A2 A1 A0		
	0 0 0	0-1-2-3-4-5-6-7	0-1-2-3-4-5-6-7
	0 0 1	1-2-3-4-5-6-7-0	1-0-3-2-5-4-7-6
	0 1 0	2-3-4-5-6-7-0-1	2-3-0-1-6-7-4-5
	0 1 1	3-4-5-6-7-0-1-2	3-2-1-0-7-6-5-4
	1 0 0	4-5-6-7-0-1-2-3	4-5-6-7-0-1-2-3
	1 0 1	5-6-7-0-1-2-3-4	5-4-7-6-1-0-3-2
	1 1 0	6-7-0-1-2-3-4-5	6-7-4-5-2-3-0-1
	1 1 1	7-0-1-2-3-4-5-6	7-6-5-4-3-2-1-0
Full Page (y)	n = A0-9/8 (location 0-y)	Cn,Cn+1,Cn+2 Cn+3,Cn+4... ...Cn-1, Cn...	Not supported

- Notes:
1. For full-page accesses: y = 512 (64MB), y = 1,024 (128MB, 256MB)
  2. For BL = 2, A1-Ai select the block of two burst; A0 selects the starting column within the block.
  3. For BL = 4, A2-Ai select the block of four burst; A0-A1 select the starting column within the block.
  4. For BL = 8, A3-Ai select the block of eight burst; A0-A2 select the starting column within the block.
  5. For a full-page burst, the full row is selected and A0-Ai select the starting column.
  6. Whenever a boundary of the block is reached within a given sequence above, the following access wraps within the block.
  7. For BL = 1, A0-Ai select the unique column to be accessed, and Mode Register bit M3 is ignored.
  8. i = 8 for 64MB and 128MB;  
i = 9 for 256MB.

Figure 6: CAS Latency Diagram



## Burst Type

Accesses within a given burst may be programmed to be either sequential or interleaved; this is referred to as the burst type and is selected via bit M3.

The ordering of accesses within a burst is determined by BL, the burst type and the starting column address, as shown in Table 6.

## CAS Latency

CL is the delay, in clock cycles, between the registration of a READ command and the availability of the first piece of output data. The latency can be set to two or three clocks.

If a READ command is registered at clock edge  $n$ , and the latency is  $m$  clocks, the data will be available by clock edge  $n + m$ . The DQ will start driving as a result of the clock edge one cycle earlier ( $n + m - 1$ ), and provided that the relevant access times are met, the data will be valid by clock edge  $n + m$ . For example, assuming that the clock cycle time is such that all relevant access times are met, if a read command is registered at T0 and the latency is programmed to two clocks, the DQ will start driving after T1 and the data will be valid by T2, as shown in Figure 6. Table 7 on page 13 indicates the operating frequencies at which each CL setting can be used.

Reserved states should not be used as unknown operation or incompatibility with future versions may result.

## Operating Mode

The normal operating mode is selected by setting M7 and M8 to zero; the other combinations of values for M7 and M8 are reserved for future use and/or test modes. The programmed BL applies to both read and write bursts.

Test modes and reserved states should not be used because unknown operation or incompatibility with future versions may result.

## Write Burst Mode

When M9 = 0, BL programmed via M0–M2 applies to both read and write bursts; when M9 = 1, the programmed BL applies to read bursts, but write accesses are single-location (nonburst) accesses.

**Table 7: CAS Latency Table**

Registered mode adds one clock cycle to CL

Speed	Allowable Operating Clock Frequency (MHz)	
	CL = 2	CL = 3
-13E	≤ 133	≤ 143
-133	≤ 100	≤ 133

## Commands

Table 8 provides a quick reference of available commands. This is followed by a written description of each command. For a more detailed description of commands and operations refer to the 64Mb, 128Mb, or 256Mb SDRAM component data sheets.

**Table 8: Commands and DQMB Operation Truth Table**

CKE is HIGH for all commands shown except SELF REFRESH

Name (Function)	CS#	RAS#	CAS#	WE#	DQMB	ADDR	DQs	Notes
COMMAND INHIBIT (NOP)	H	X	X	X	X	X	X	
NO OPERATION (NOP)	L	H	H	H	X	X	X	
ACTIVE (Select bank and activate row)	L	L	H	H	X	Bank/Row	X	1
READ (Select bank and column, and start READ burst)	L	H	L	H	L/H <sup>8</sup>	Bank/Col	X	2
WRITE (Select bank and column, and start WRITE burst)	L	H	L	L	L/H <sup>8</sup>	Bank/Col	Valid	2
BURST TERMINATE	L	H	H	L	X	X	Active	
PRECHARGE (Deactivate row in bank or banks)	L	L	H	L	X	Code	X	3
AUTO REFRESH or SELF REFRESH (Enter self refresh mode)	L	L	L	H	X	X	X	4, 5
LOAD MODE REGISTER	L	L	L	L	X	Op-Code	X	6
Write Enable/Output Enable	–	–	–	–	L	–	Active	7
Write Inhibit/Output High-Z	–	–	–	–	H	–	High-Z	7

- Notes:
1. A0–A11 provide row address, and BA0, BA1 determine which bank is made active.
  2. A0–A8 (64MB and 128MB) or A0–A9 (256MB) provide column address; A10 HIGH enables the auto precharge feature (nonpersistent), while A10 LOW disables the auto precharge feature; BA0, BA1 determine which bank is being read from or written to.
  3. A10 LOW: BA0, BA1 determine which bank is being precharged. A10 HIGH: both banks are precharged and BA0, BA1 are “Don’t Care.”
  4. This command is AUTO REFRESH if CKE is HIGH, SELF REFRESH if CKE is LOW.
  5. Internal refresh counter controls row addressing; all inputs and I/Os are “Don’t Care” except for CKE.
  6. A0–A11 define the op-code written to the mode register.
  7. Activates or deactivates the DQ during WRITES (zero-clock delay) and READs (two-clock delay).

## Electrical Specifications

Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

**Figure 7: Absolute Maximum Ratings**

Parameter	Min	Max	Units
Voltage on VDD supply, relative to Vss	-1V	+4.6	V
Voltage on inputs, NC or I/O pins relative to Vss	-1V	+4.6	V
Operating temperature, T <sub>OPR</sub> (Commercial - ambient)	0°C	+55	°C
Storage Temperature (plastic)	-55	+150	°C

**Table 9: DC Electrical Characteristics and Operating Conditions**

Notes: 1, 5, 6; notes appear on pages 18 and 19; VDD, VDDQ = +3.3V ±0.3V

Parameter/Condition		Symbol	Min	Max	Units	Notes
Supply voltage		VDD, VDDQ	3	3.6	V	
Input high voltage: Logic 1; All inputs		VIH	2	VDD + 0.3	V	22
Input low voltage: Logic 0; All inputs		VIL	-0.3	0.8	V	22
Input leakage current: Any input 0V ≤ VIN ≤ VDD (All other pins not under test = 0V)	Command and address	IL	-5	5	μA	32
	S#, CKE		-2.5	2.5		
	CK, DQMB		-5	-5		
Output leakage current: DQ pins are disabled; 0V ≤ VOUT ≤ VDDQ	DQ	IOZ	-5	5	μA	32
Output levels:						
Output high voltage (IOUT = -4mA)		VOH	2.4	–	V	
Output low voltage (IOUT = 4mA)		VOL	–	0.4	V	

**Table 10: IDD Specifications and Conditions – 64MB**

Notes: 1, 5, 6; VDD = +3.3V ±0.3V; notes appear on pages 18 and 19

Parameter/Condition	Symbol	Max		Units	Notes	
		-13E	-133			
Operating current: Active mode; Burst = 2; READ or WRITE; t <sub>RC</sub> = t <sub>RC</sub> (MIN); CL = 3	IDD1	1,125	1,035	mA	3, 18, 19, 29	
Standby current: Power-Down mode; CKE = LOW; All banks idle	IDD2	18	18	mA	29	
Standby current: Active mode; S# = HIGH; CKE = HIGH; All banks active after t <sub>RCD</sub> met; No accesses in progress	IDD3	405	405	mA	3, 18, 19, 29	
Operating current: Burst mode; Continuous burst; READ or WRITE; All banks active; CL = 3	IDD4	1,350	1,260	mA	3, 18, 19, 29	
Auto refresh current: CKE = HIGH; S# = HIGH	t <sub>RC</sub> = t <sub>RC</sub> (MIN)	IDD5	2,070	1,890	mA	3, 18, 19, 29
	t <sub>RC</sub> = 15.625μs	IDD6	27	27	mA	18, 19, 29
Self refresh current: CKE ≤ 0.2V	IDD7	9	9	mA	4	

**Table 11: IDD Specifications and Conditions – 128MB**

Notes: 1, 5, 6, 11, 13; VDD = +3.3V ±0.3V; notes appear on pages 18 and 19

Parameter/Condition	Symbol	Max		Units	Notes
		-13E	-133		
Operating current: Active mode; Burst = 2; READ or WRITE; $t_{RC} = t_{RC}(\text{MIN})$ ; CL = 3	IDD1	1,440	1,350	mA	3, 18, 19, 29
Standby current: Power-Down mode; CKE = LOW; All banks idle	IDD2	18	18	mA	29
Standby current: Active mode; S# = HIGH; CKE = HIGH; All banks active after $t_{RCD}$ met; No accesses in progress	IDD3	450	450	mA	3, 18, 19, 29
Operating current: Burst mode; Continuous burst; READ or WRITE; All banks active; CL = 3	IDD4	1,485	1,350	mA	3, 18, 19, 29
Auto refresh current: CKE = HIGH; S# = HIGH	$t_{RC} = t_{RC}(\text{MIN})$	2,970	2,790	mA	3, 18, 19, 29
	$t_{RC} = 15.625\mu\text{s}$	27	27	mA	18, 19, 29
Self refresh current: CKE ≤ 0.2V	IDD7	18	18	mA	4

**Table 12: IDD Specifications and Conditions – 256MB**

Notes: 1, 5, 6, 11, 13; VDD = +3.3V ±0.3V; notes appear on pages 18 and 19

Parameter/Condition	Symbol	Max		Units	Notes
		-13E	-133		
Operating current: Active mode; Burst = 2; READ or WRITE; $t_{RC} = t_{RC}(\text{MIN})$ ; CL = 3	IDD1	1,215	1,125	mA	3, 18, 19, 29
Standby current: Power-Down mode; CKE = LOW; All banks idle	IDD2	18	18	mA	29
Standby current: Active mode; S# = HIGH; CKE = HIGH; All banks active after $t_{RCD}$ met; No accesses in progress	IDD3	360	360	mA	3, 18, 19, 29
Operating current: Burst mode; Continuous burst; READ or WRITE; All banks active; CL = 3	IDD4	1,215	1,215	mA	3, 18, 19, 29
Auto refresh current: CKE = HIGH; S# = HIGH	$t_{RC} = t_{RC}(\text{MIN})$	2,565	2,430	mA	3, 18, 19, 29
	$t_{RC} = 7.8125\mu\text{s}$	32	32	mA	18, 19, 29
Self refresh current: CKE ≤ 0.2V	IDD7	23	23	mA	4

**Table 13: Capacitance**

Notes: 2; VDD = 3.3V ±0.3V; notes appear on pages 18 and 19

Parameter	Symbol	Max	Units
Input capacitance: Address and command	Ci1	8	pF
Input capacitance: S#, CKE, DQMB#	Ci2	8	pF
Input capacitance: CK	Ci3	6	pF
Input/Output capacitance: DQ, CB	CiO	8	pF



# 64MB, 128MB, 256MB (x72, ECC, SR): 168-PIN SDRAM RDIMM Electrical Specifications

**Table 14: Electrical Characteristics and Recommended AC Operating Conditions**

Notes: 5, 6, 7, 8, 9, 10, 30; VDD = 3.3V ±0.3V; notes appear on pages 18 and 19

AC Characteristics			-13E		-133		Units	Notes
Parameter		Symbol	Min	Max	Min	Max		
Access time from CLK (positive edge)	CL = 3	$t_{AC}$		5.4		5.4	ns	26
	CL = 2	$t_{AC}$		5.4		6	ns	
Address hold time		$t_{AH}$	0.8		0.8		ns	
Address setup time		$t_{AS}$	1.5		1.5		ns	
CLK high level width		$t_{CH}$	2.5		2.5		ns	
CLK low level width		$t_{CL}$	2.5		2.5		ns	
Clock cycle time	CL = 3	$t_{CK}$	7		7.5		ns	13
	CL = 2	$t_{CK}$	7.5		10		ns	13
CKE hold time		$t_{CKH}$	0.8		0.8		ns	
CKE setup time		$t_{CKS}$	1.5		1.5		ns	
CS#, RAS#, CAS#, WE#, DQM hold time		$t_{CMH}$	0.8		0.8		ns	
CS#, RAS#, CAS#, WE#, DQM setup time		$t_{CMS}$	1.5		1.5		ns	
Data-in hold time		$t_{DH}$	0.8		0.8		ns	
Data-in setup time		$t_{DS}$	1.5		1.5		ns	
Data-out High-Z time	CL = 3	$t_{HZ}$		5.4		5.4	ns	
	CL = 2	$t_{HZ}$		5.4		6	ns	
Data-out Low-Z time		$t_{LZ}$	1		1		ns	
Data-out hold time (load)		$t_{OH}$	2.7		2.7		ns	
Data-out hold time (no load)		$t_{OH_N}$	1.8		1.8		ns	24
ACTIVE to PRECHARGE command		$t_{RAS}$	37	120,000	44	120,000	ns	31
ACTIVE to ACTIVE command period		$t_{RC}$	60		66		ns	
ACTIVE to READ or WRITE delay		$t_{RCD}$	15		20		ns	
Refresh period (4,096 cycles)		$t_{REF}$		64		64	ms	
AUTO REFRESH period		$t_{RFC}$	66		66		ns	
PRECHARGE command period		$t_{RP}$	15		20		ns	
ACTIVE bank <i>a</i> to ACTIVE bank <i>b</i> command		$t_{RRD}$	14		15		ns	
Transition time		$t_T$	0.3		0.3	1.2	ns	23
WRITE recovery time		$t_{WR}$	1 CLK + 7ns		1 CLK + 7.5ns		–	27
			14		15		ns	27
Exit SELF REFRESH to ACTIVE command		$t_{XSR}$	67		75		ns	





# 64MB, 128MB, 256MB (x72, ECC, SR): 168-PIN SDRAM RDIMM Electrical Specifications

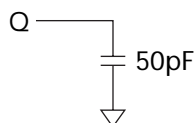
**Table 15: AC Functional Characteristics**

Notes: 5, 6, 7, 8, 9, 11, 13, 30; VDD = 3.3V ±0.3V; notes appear on pages 18 and 19

Parameters		Symbol	-133	Units	Notes
READ/WRITE command to READ/WRITE command		<sup>t</sup> CCD	1	<sup>t</sup> CK	17
CKE to clock disable or power-down entry mode		<sup>t</sup> CKED	1	<sup>t</sup> CK	14, 33
CKE to clock enable or power-down exit setup mode		<sup>t</sup> PED	1	<sup>t</sup> CK	14,
DQM to input data delay		<sup>t</sup> DQD	0	<sup>t</sup> CK	17, 33
DQM to data mask during WRITES		<sup>t</sup> DQM	0	<sup>t</sup> CK	17, 33
DQM to data High-Z during READs		<sup>t</sup> DQZ	2	<sup>t</sup> CK	17, 33
WRITE command to input data delay		<sup>t</sup> DWD	0	<sup>t</sup> CK	17, 33
Data-in to ACTIVE command		<sup>t</sup> DAL	5	<sup>t</sup> CK	15, 21, 33
Data-in to PRECHARGE command		<sup>t</sup> DPL	2	<sup>t</sup> CK	21, 16, 33
Last data-in to burst STOP command		<sup>t</sup> BDL	1	<sup>t</sup> CK	17, 33
Last data-in to new READ/WRITE command		<sup>t</sup> CDL	1	<sup>t</sup> CK	17, 33
Last data-in to PRECHARGE command		<sup>t</sup> RDL	2	<sup>t</sup> CK	21, 16, 33
LOAD MODE REGISTER command to ACTIVE or REFRESH command		<sup>t</sup> MRD	2	<sup>t</sup> CK	25
Data-out to High-Z from PRECHARGE command	CL = 3	<sup>t</sup> ROH	3	<sup>t</sup> CK	17, 33
	CL = 2	<sup>t</sup> ROH	2	<sup>t</sup> CK	17, 33

## Notes

1. All voltages referenced to VSS.
2. This parameter is sampled. VDD, VDDQ = +3.3V; f = 1 MHz; T<sub>A</sub> = 25°C; pin under test biased at 1.4V.
3. IDD is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the outputs open.
4. Enables on-chip refresh and address counters.
5. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range is ensured (0°C to +55°C).
6. An initial pause of 100μs is required after power-up, followed by two AUTO REFRESH commands, before proper device operation is ensured. (VDD and VDDQ must be powered up simultaneously. VSS and VSSQ must be at same potential.) The two AUTO REFRESH command wake-ups should be repeated any time the t<sub>REF</sub> refresh requirement is exceeded.
7. AC characteristics assume t<sub>T</sub> = 1ns.
8. In addition to meeting the transition rate specification, the clock and CKE must transit between VIH and VIL (or between VIL and VIH) in a monotonic manner.
9. Outputs measured at 1.5V with equivalent load:



10. t<sub>HZ</sub> defines the time at which the output achieves the open circuit condition; it is not a reference to VOH or VOL. The last valid data element will meet t<sub>OH</sub> before going High-Z.
11. AC timing and IDD tests have VIL = 0V and VIH = 3V, with timing referenced to 1.5V crossover point. If the input transition time is longer than 1ns, then the timing is referenced at VIL (MAX) and VIH (MIN) and no longer at the ISV crossover point.
12. Other input signals are allowed to transition no more than once every two clocks and are otherwise at valid VIH or VIL levels.
13. Once clock is added to latency in registered mode.
14. Timing actually specified by t<sub>CKS</sub>; clock(s) specified as a reference only at minimum cycle rate.
15. Timing actually specified by t<sub>WR</sub> plus t<sub>RP</sub>; clock(s) specified as a reference only at minimum cycle rate.
16. Timing actually specified by t<sub>WR</sub>.
17. Required clocks are specified by JEDEC functionality and are not dependent on any timing parameter.
18. The IDD current will increase or decrease proportionally according to the amount of frequency alteration for the test condition.
19. Address transitions average one transition every two clocks.
20. CLK must be toggled a minimum of two times during this period.
21. Based on t<sub>CK</sub> = 7.5ns for -133 and -13E.
22. VIH overshoot: VIH (MAX) = VDDQ + 2V for a pulse width ≤ 3ns, and the pulse width cannot be greater than one third of the cycle rate. VIL undershoot: VIL (MIN) = -2V for a pulse width ≤ 3ns.

23. The clock frequency must remain constant (stable clock is defined as a signal cycling within timing constraints specified for the clock pin) during access or precharge states (READ, WRITE, including  $t_{WR}$ , and PRECHARGE commands). CKE may be used to reduce the data rate.
24. Precharge mode only.
25. JEDEC specifies three clocks.
26.  $t_{AC}$  for -133/-13E at CL = 3 with no load is 4.6ns and is guaranteed by design.
27. Parameter guaranteed by design.
28. For -13E, CL = 2 and  $t_{CK}$  = 7.5ns; for -133, CL = 3 and  $t_{CK}$  = 7.5ns.
29. CKE is HIGH during refresh command period  $t_{RFC}$  (MIN) else CKE is LOW. The  $I_{DD6}$  limit is actually a nominal value and does not result in a fail value.
30. Refer to device data sheet for timing waveforms.
31. The value of  $t_{RAS}$  used in -13E speed grade module SPDs is calculated from  $t_{RC} - t_{RP} = 45ns$ .
32. Leakage number reflects the worst case leakage possible through the module pin, not what each memory device contributes.
33. This AC timing function will show an extra clock cycle when in registered mode.

## PLL and Register Specifications

**Table 16: Register Timing Requirements and Switching Characteristics**

Register	Symbol	Parameter	Condition	0°C ≤ T <sub>A</sub> ≤ 55°C V <sub>DD</sub> = +3.3V ±0.3V		Units
				Min	Max	
SSTL bit pattern by JESD82-2	f <sub>clock</sub>	Clock frequency		150	240	MHz
	t <sub>pd1</sub>	Propagation delay, Single rank (CK to Output)	50pF to GND and 50Ω to V <sub>TT</sub>	1.4	3.5	ns
	t <sub>pd2</sub>	Propagation delay, Dual rank (CK to output)	30pF to GND and 50Ω to V <sub>TT</sub>	0.7	2.4	ns
	t <sub>w</sub>	Pulse duration	CK, HIGH or LOW	3.3	–	ns
	t <sub>su</sub>	Setup time	Data before CK HIGH	0.75	–	ns
	t <sub>h</sub>	Hold time	Data after CK HIGH	0.75	–	ns

**Table 17: PLL Clock Driver Timing Requirements And Switching Characteristics**

Parameter	Symbol	0°C ≤ T <sub>A</sub> ≤ 55°C V <sub>DD</sub> = +3.3V ±0.3V		Units	Notes
		Min	Max		
Operating clock frequency	f <sub>CK</sub>	50	140	MHz	
Input duty cycle	t <sub>DC</sub>	44	55	%	
Cycle to cycle jitter	t <sub>JIT<sub>CC</sub></sub>	-75	75	ps	
Static phase offset	t <sub>∅</sub>	-150	150	ps	
SSC induced skew	t <sub>SSC</sub>	-	150	ps	1, 2
Output to output skew	t <sub>SK<sub>O</sub></sub>	-	150	ps	

- Notes: 1. SSC = Spread spectrum clock. The use of SSC synthesizers on the system motherboard will reduce EMI.
2. Skew is defined as the total clock skew between any two outputs and is therefore specified as a maximum only.

## Serial Presence-Detect

### SPD Clock and Data Conventions

Data states on the SDA line can change only during SCL LOW. SDA state changes during SCL HIGH are reserved for indicating start and stop conditions (as shown in Figure 8, and Figure 9 on page 22).

### SPD Start Condition

All commands are preceded by the start condition, which is a HIGH-to-LOW transition of SDA when SCL is HIGH. The SPD device continuously monitors the SDA and SCL lines for the start condition and will not respond to any command until this condition has been met.

### SPD Stop Condition

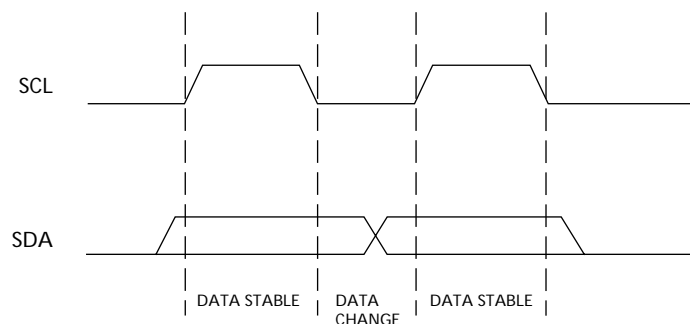
All communications are terminated by a stop condition, which is a LOW-to-HIGH transition of SDA when SCL is HIGH. The stop condition is also used to place the SPD device into standby power mode.

### SPD Acknowledge

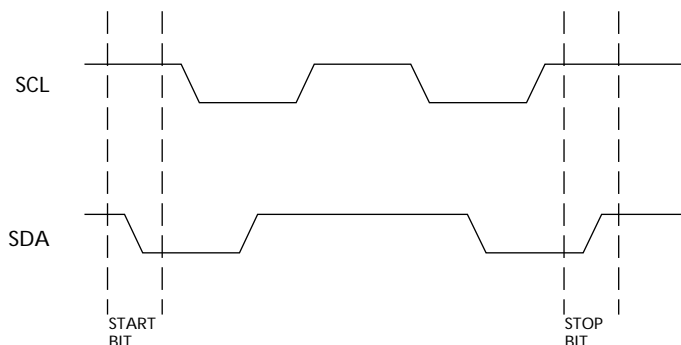
Acknowledge is a software convention used to indicate successful data transfers. The transmitting device, either master or slave, will release the bus after transmitting eight bits. During the ninth clock cycle, the receiver will pull the SDA line LOW to acknowledge that it received the 8 bits of data (as shown in Figure 10 on page 22).

The SPD device will always respond with an acknowledge after recognition of a start condition and its slave address. If both the device and a WRITE operation have been selected, the SPD device will respond with an acknowledge after the receipt of each subsequent 8-bit word. In the read mode the SPD device will transmit eight bits of data, release the SDA line and monitor the line for an acknowledge. If an acknowledge is detected and no stop condition is generated by the master, the slave will continue to transmit data. If an acknowledge is not detected, the slave will terminate further data transmissions and await the stop condition to return to standby power mode.

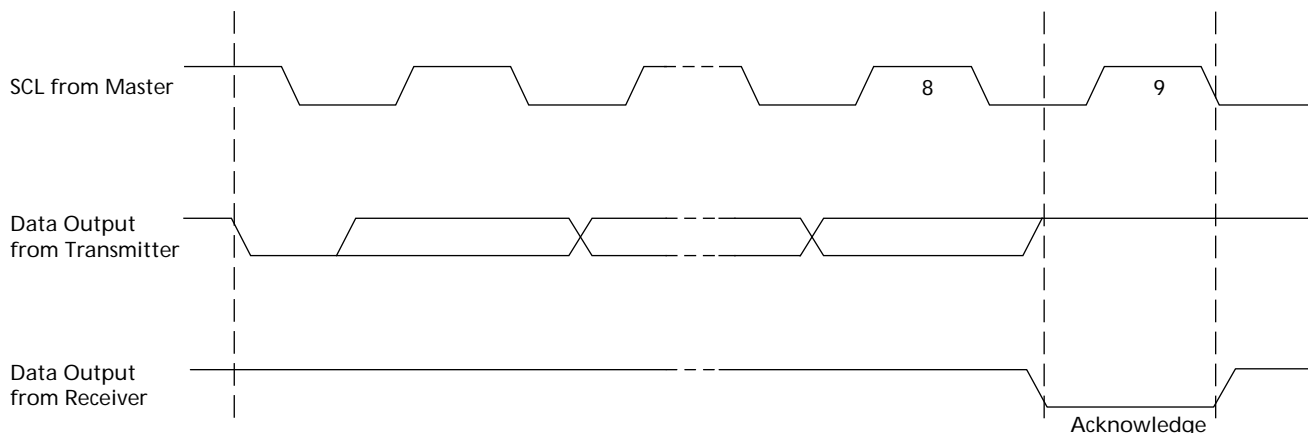
**Figure 8: Data Validity**



**Figure 9: Definition of Start and Stop**



**Figure 10: Acknowledge Response From Receiver**



**Table 18: EEPROM Device Select Code**

Most significant bit (b7) is sent first

Select Code	Device Type Identifier				Chip Enable			R $\overline{W}$
	b7	b6	b5	b4	b3	b2	b1	b0
Memory area select code (two arrays)	1	0	1	0	SA2	SA1	SA0	R $\overline{W}$
Protection register select code	0	1	1	0	SA2	SA1	SA0	R $\overline{W}$

**Table 19: EEPROM Operating Modes**

Mode	R $\overline{W}$ Bit	$\overline{W}C$	Bytes	Initial Sequence
Current address read	1	V <sub>IH</sub> or V <sub>IL</sub>	1	Start, device select, R $\overline{W}$ = 1
Random address read	0	V <sub>IH</sub> or V <sub>IL</sub>	1	Start, device select, R $\overline{W}$ = 0, Address
	1	V <sub>IH</sub> or V <sub>IL</sub>		Restart, device select, R $\overline{W}$ = 1
Sequential read	1	V <sub>IH</sub> or V <sub>IL</sub>	≥ 1	Similar to current or random address read
Byte write	0	V <sub>IL</sub>	1	Start, device select, R $\overline{W}$ = 0
Page write	0	V <sub>IL</sub>	≤ 16	Start, device select, R $\overline{W}$ = 0

Figure 11: SPD EEPROM

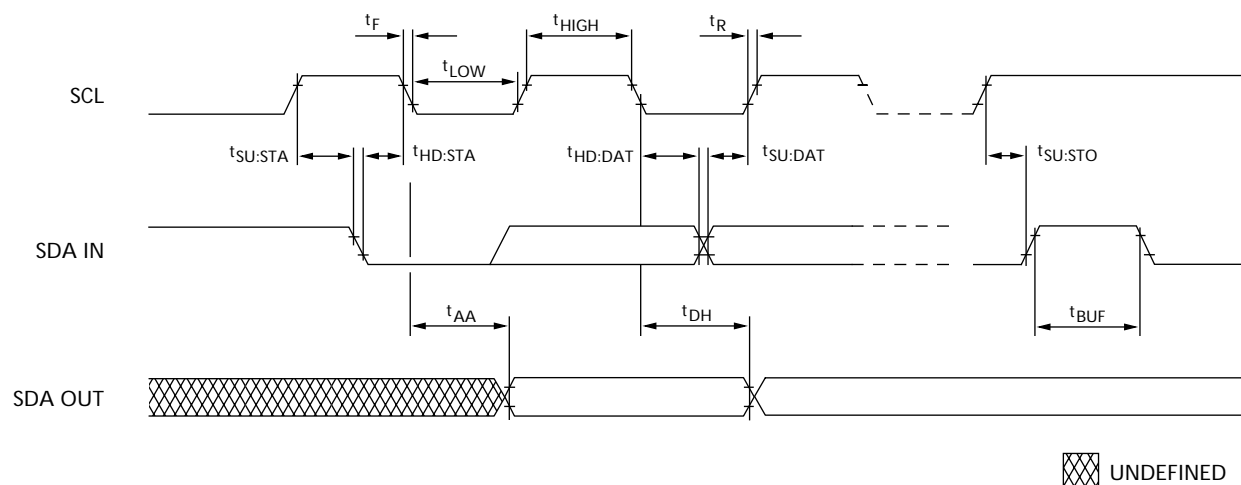


Table 20: Serial Presence-Detect EEPROM DC Operating Conditions

All voltages referenced to  $V_{SS}$ ;  $V_{DDSPD} = +2.3V$  to  $+3.6V$

Parameter/Condition	Symbol	Min	Max	Units
Supply voltage	$V_{DD}$	3	3.6	V
Input high voltage: Logic 1; All inputs	$V_{IH}$	$V_{DD} \times 0.7$	$V_{DD} + 0.5$	V
Input low voltage: Logic 0; All inputs	$V_{IL}$	-1	$V_{DD} \times 0.3$	V
Output low voltage: $I_{OUT} = 3mA$	$V_{OL}$	-	0.4	V
Input leakage current: $V_{IN} = GND$ to $V_{DD}$	$I_{LI}$	-	10	$\mu A$
Output leakage current: $V_{OUT} = GND$ to $V_{DD}$	$I_{LO}$	-	10	$\mu A$
Standby current: $SCL = SDA = V_{DD} - 0.3V$ ; All other inputs = $V_{DD}$ or $V_{SS}$	$I_{SB}$	-	30	$\mu A$
Power supply current: SCL clock frequency = 100 KHz	$I_{DD}$	-	2	mA

**Table 21: Serial Presence-Detect EEPROM AC Operating Conditions**

All voltages referenced to V<sub>SS</sub>; V<sub>DDSPD</sub> = +2.3V to +3.6V

Parameter/Condition	Symbol	Min	Max	Units	Notes
SCL LOW to SDA data-out valid	$t_{AA}$	0.2	0.9	$\mu s$	1
Time the bus must be free before a new transition can start	$t_{BUF}$	1.3		$\mu s$	
Data-out hold time	$t_{DH}$	200		ns	
SDA and SCL fall time	$t_F$		300	ns	2
Data-in hold time	$t_{HD:DAT}$	0		$\mu s$	
Start condition hold time	$t_{HD:STA}$	0.6		$\mu s$	
Clock HIGH period	$t_{HIGH}$	0.6		$\mu s$	
Noise suppression time constant at SCL, SDA inputs	$t_I$		50	ns	
Clock LOW period	$t_{LOW}$	1.3		$\mu s$	
SDA and SCL rise time	$t_R$		0.3	$\mu s$	2
SCL clock frequency	$f_{SCL}$		400	KHz	
Data-in setup time	$t_{SU:DAT}$	100		ns	
Start condition setup time	$t_{SU:STA}$	0.6		$\mu s$	3
Stop condition setup time	$t_{SU:STO}$	0.6		$\mu s$	
WRITE cycle time	$t_{WRC}$		10	ms	4

- Notes: 1. To avoid spurious start and stop conditions, a minimum delay is placed between SCL = 1 and the falling or rising edge of SDA.
2. This parameter is sampled.
3. For a restart condition, or following a WRITE cycle.
4. The SPD EEPROM WRITE cycle time ( $t_{WRC}$ ) is the time from a valid stop condition of a write sequence to the end of the EEPROM internal erase/program cycle. During the WRITE cycle, the EEPROM bus interface circuit is disabled, SDA remains HIGH due to pull-up resistor, and the EEPROM does not respond to its slave address.



**Table 22: Serial-Presence Detect Matrix**  
 "1"/"0": Serial Data, "driven to HIGH"/"driven to LOW"

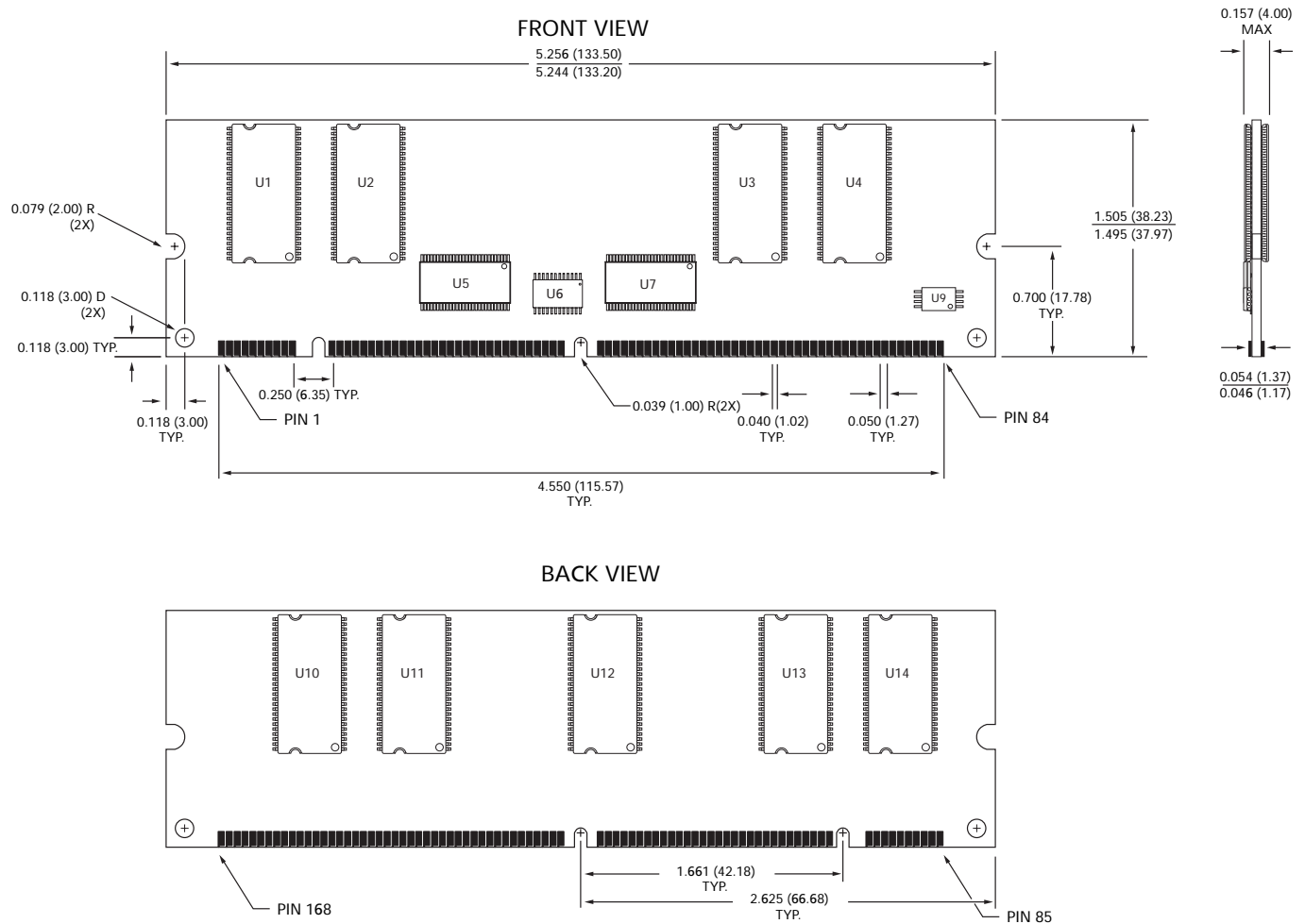
Byte	Description	Entry (Version)	MT9LSDT872	MT9LSDT1672	MT9LSDT3272
0	Number of bytes used by Micron	128	80	80	80
1	Total number of SPD memory bytes	256	08	08	08
2	Memory type	SDRAM	04	04	04
3	Number of row addresses	12 or 13	0C	0C	0D
4	Number of column addresses	9 or 10	09	0A	0A
5	Number of banks	1	01	01	01
6	Module data width	72	48	48	48
7	Module data width (continued)	0	00	00	00
8	Module voltage interface levels	LVTTL	01	01	01
9	SDRAM cycle time, $t_{CK}$ (CL = 3)	7ns (-13E) 7.5ns (-133)	70 75	70 75	70 75
10	SDRAM access from clock, $t_{AC}$ (CL = 3)	5.4ns (-13E/-133)	54	54	54
11	Module configuration type	ECC	02	02	02
12	Refresh rate/type	15.6 $\mu$ s or 7.8/SELF	80	80	82
13	SDRAM width (primary DRAM)	8	08	08	08
14	Error-checking SDRAM data width	8	08	08	08
15	Min. clock delay from back-to-back random column addresses, $t_{CCD}$	1	01	01	01
16	Burst lengths supported	1, 2, 4, 8, PAGE	8F	8F	8F
17	Number of banks on SDRAM device	4	04	04	04
18	CAS latencies supported	2,3	06	06	06
19	CS latency	0	01	01	01
20	WE latency	0	01	01	01
21	SDRAM module attributes	-13E/-133	1F	1F	1F
22	SDRAM device attributes: General	0E	0E	0E	0E
23	SDRAM cycle time, $t_{CK}$ (CL = 2)	7.5ns (-13E) 10ns (-133)	75 A0	75 A0	75 A0
24	SDRAM access from clock, $t_{AC}$ (CL = 2)	5.4ns (-13E) 6ns (-133)	54 60	54 60	54 60
25	SDRAM cycle time, $t_{CK}$ (CL = 1)	–	00	00	00
26	SDRAM access from clock, $t_{AC}$ (CL = 1)	–	00	00	00
27	Minimum row precharge time, $t_{RP}$	15ns (-13E) 20ns (-133) 14ns (-13E)	0F 14 14	0F 14 14	0F 14 14
28	Minimum row active to row active, $t_{RRD}$	14ns (-13E) 15ns (-133)	0E 0F	0E 0F	0E 0F
29	Minimum RAS# to CAS# delay, $t_{RCD}$	15ns (-13E) 20ns (-133)	0F 14	0F 14	0F 14
30	Minimum RAS# pulse width, $t_{RAS}$	37ns (-13E) 44ns (-133)	2D 2C	2D 2C	2D 2C
31	Module rank density	64MB/128MB/ 256MB	10	20	40
32	Command and address setup time, $t_{AS}$ , $t_{CMS}$	1.5ns (-13E/-133)	15	15	15

**Table 22: Serial-Presence Detect Matrix (Continued)**  
 "1"/"0": Serial Data, "driven to HIGH"/"driven to LOW"

Byte	Description	Entry (Version)	MT9LSDT872	MT9LSDT1672	MT9LSDT3272
33	Command and address hold time, <sup>t</sup> AH, <sup>t</sup> CMH	0.8ns (-13E/-133)	08	08	08
34	Data signal input setup time, <sup>t</sup> DS	1.5ns (-13E/-133)	15	15	15
35	Data signal input hold time, <sup>t</sup> DH	0.8ns (-13E/-133)	08	08	08
36-40	Reserved		00	00	00
41	Device minimum active/auto-refresh time, <sup>t</sup> RC	66ns (-13E) 71ns (-133)	3C 42	3C 42	3C 42
42-61	Reserved		00	00	00
62	SPD revision	REV. 2.0	02	02	02
63	Checksum for bytes 0-62	-13E -133	B4 00	C5 11	E8 34
64	Manufacturer's JEDEC ID code	MICRON	2C	2C	2C
65-71	Manufacturer's JEDEC ID code (continued)		FF	FF	FF
72	Manufacturing location	01-12	01-0C	01-0C	01-0C
73-90	Module part number (ASCII)		Variable data	Variable data	Variable data
91	PCB identification code	1-9	01-09	01-09	01-09
92	Identification code (cont.)	0	00	00	00
93	Year of manufacture in BCD		Variable data	Variable data	Variable data
94	Week of manufacture in BCD		Variable data	Variable data	Variable data
95-98	Module serial number		Variable data	Variable data	Variable data
99-125	Manufacturer-Specific data (RSVD)		-	-	-
126	System frequency	100 MHz (-13E/-133)	64	64	64
127	SDRAM component and clock detail		8F	8F	8F

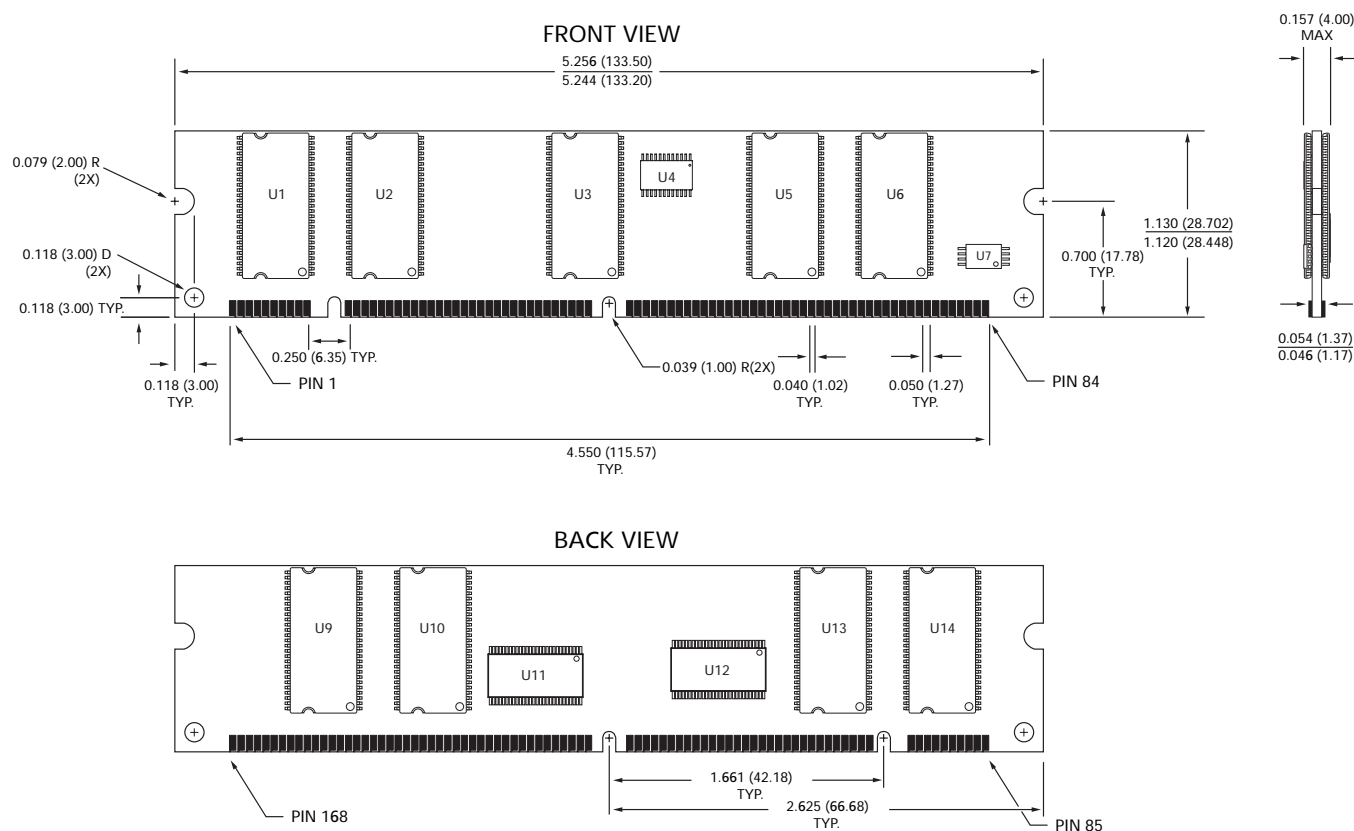
## Module Dimensions

Figure 12: 168-Pin DIMM Dimensions – Standard PCB



Note: All dimensions in inches (millimeters);  $\frac{\text{MAX}}{\text{MIN}}$  or typical where noted.

**Figure 13: 168-Pin DIMM Dimensions – Low-Profile PCB**



Note: All dimensions in inches (millimeters);  $\frac{\text{MAX}}{\text{MIN}}$  or typical where noted.



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This data sheet contains minimum and maximum limits specified over the complete power supply and temperature range for production devices. Although considered final, these specifications are subject to change, as further product development and data characterization sometimes occur.