MOTOROLA
SEMICONDUCTOR TECHNICAL DATA

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Product Preview

TMOS E-FET ™
High Energy Power FET

D^2PAK for Surface Mount
N–Channel Enhancement–Mode Silicon Gate

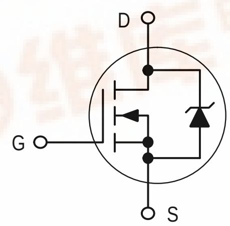
MTB3N60E

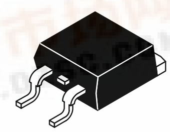
Motorola Preferred Device

TMOS POWER FET
3.0 AMPERES
600 VOLTS
$R_{DS(on)}$ = 2.2 OHMS

This advanced high voltage TMOS E–FET is designed to withstand high energy in the avalanche mode and switch efficiently. This new high energy device also offers a drain–to–source diode with fast recovery time. Designed for high voltage, high speed switching applications such as power supplies, PWM motor controls and other inductive loads, the avalanche energy capability is specified to eliminate the guesswork in designs where inductive loads are switched and offer additional safety margin against unexpected voltage transients.

- Avalanche Energy Capability Specified at Elevated Temperature
- Low Stored Gate Charge for Efficient Switching
- Internal Source–to–Drain Diode Designed to Replace External Zener Transient Suppressor — Absorbs High Energy in the Avalanche Mode
- Source–to–Drain Diode Recovery Time Comparable to Discrete Fast Recovery Diode





CASE 418B–03, Style 2
D^2PAK

MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain–Source Voltage	V_{DSS}	600	Vdc
Drain–Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	600	Vdc
Gate–Source Voltage — Continuous — Non–repetitive	V_{GS} V_{GSM}	±20 ±40	Vdc Vpk
Drain Current — Continuous — Continuous @ 100°C — Pulsed	I_D I_D I_{DM}	3.0 2.4 14	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C Total Power Dissipation @ T_A = 25°C(1)	P_D	75 0.6 2.5	Watts W/°C Watts
Operating and Storage Temperature Range	T_J, T_{stg}	–55 to 150	°C

UNCLAMPED DRAIN–TO–SOURCE AVALANCHE CHARACTERISTICS (T_J < 150°C)

Rating	Symbol	Value	Unit
Single Pulse Drain–to–Source Avalanche Energy — T_J = 25°C — T_J = 100°C Repetitive Pulse Drain–to–Source Avalanche Energy	W_{DSR}(2) W_{DSR}(3)	290 46 7.5	mJ

THERMAL CHARACTERISTICS

Rating	Symbol	Value	Unit
Thermal Resistance — Junction to Case — Junction to Ambient — Junction to Ambient(1)	$R_{\theta JC}$ $R_{\theta JA}$ $R_{\theta JA}$	1.67 62.5 50	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 10 seconds	T_L	260	°C

(1) When surface mounted to an FR–4 board using the minimum recommended pad size
(2) V_{DD} = 50 V, I_D = 3.0 A
(3) Pulse Width and frequency is limited by T_J(max) and thermal response

This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

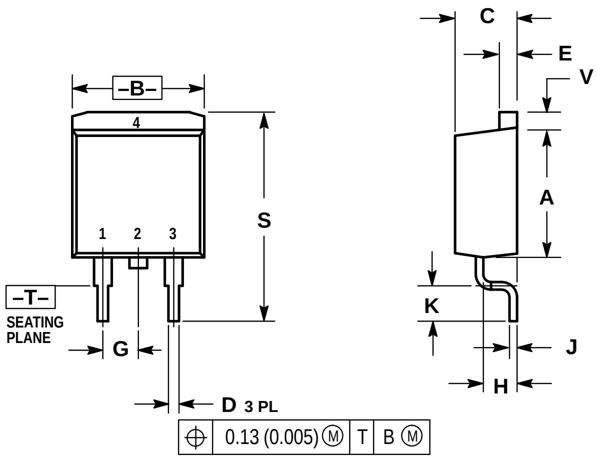
Preferred devices are Motorola recommended choices for future use and best overall value.

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain–to–Source Breakdown Voltage (V_{GS} = 0, I_D = 250 μAdc)		$V_{(BR)DSS}$	600	—	—	Vdc
Zero Gate Voltage Drain Current (V_{DS} = 600 V, V_{GS} = 0) (V_{DS} = 480 V, V_{GS} = 0, T_J = 125°C)		I_{DSS}	— —	— —	10 100	μAdc
Gate–Body Leakage Current — Forward (V_{GSF} = 20 Vdc, V_{DS} = 0)		I_{GSSF}	—	—	100	nAdc
Gate–Body Leakage Current — Reverse (V_{GSR} = 20 Vdc, V_{DS} = 0)		I_{GSSR}	—	—	100	nAdc
ON CHARACTERISTICS*						
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 250 μAdc) (T_J = 125°C)		$V_{GS(th)}$	2.0 1.5	— —	4.0 3.5	Vdc
Static Drain–to–Source On–Resistance (V_{GS} = 10 Vdc, I_D = 1.5 A)		$R_{DS(on)}$	—	2.1	2.2	Ohms
Drain–to–Source On–Voltage (V_{GS} = 10 Vdc) (I_D = 3.0 A) (I_D = 1.5 A, T_J = 100°C)		$V_{DS(on)}$	— —	— —	9.0 7.5	Vdc
Forward Transconductance (V_{DS} = 15 Vdc, I_D = 1.5 A)		g_{FS}	1.5	—	—	mhos
DYNAMIC CHARACTERISTICS						
Input Capacitance	(V_{DS} = 25 V, V_{GS} = 0, f = 1.0 MHz)	C_{iss}	—	770	—	pF
Output Capacitance		C_{oss}	—	105	—	
Transfer Capacitance		C_{rss}	—	19	—	
SWITCHING CHARACTERISTICS*						
Turn–On Delay Time	(V_{DD} = 300 V, I_D ≈ 3.0 A, R_L = 100 Ω, R_G = 12 Ω, $V_{GS(on)}$ = 10 V)	$t_{d(on)}$	—	23	—	ns
Rise Time		t_r	—	34	—	
Turn–Off Delay Time		$t_{d(off)}$	—	58	—	
Fall Time		t_f	—	35	—	
Total Gate Charge	(V_{DS} = 420 V, I_D = 3.0 A, V_{GS} = 10 V)	Q_g	—	28	31	nC
Gate–Source Charge		Q_{gs}	—	5.0	—	
Gate–Drain Charge		Q_{gd}	—	17	—	
SOURCE–DRAIN DIODE CHARACTERISTICS						
Forward On–Voltage	(I_S = 3.0 A, di/dt = 100 A/μs)	V_{SD}	—	—	1.4	Vdc
Forward Turn–On Time		t_{on}	—	**	—	ns
Reverse Recovery Time		t_{rr}	—	400	—	
INTERNAL PACKAGE INDUCTANCE						
Internal Drain Inductance (Measured from the contact screw on tab to center of die) (Measured from the drain lead 0.25″ from package to center of die)		L_d	— —	3.5 4.5	— —	nH
Internal Source Inductance (Measured from the source lead 0.25″ from package to source bond pad)		L_s	—	7.5	—	

* Pulse Test: Pulse Width = 300 μs, Duty Cycle ≤ 2.0%.
** Limited by circuit inductance.

PACKAGE DIMENSIONS



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	0.340	0.380	8.64	9.65
B	0.380	0.405	9.65	10.29
C	0.160	0.190	4.06	4.83
D	0.020	0.035	0.51	0.89
E	0.045	0.055	1.14	1.40
G	0.100 BSC		2.54 BSC	
H	0.080	0.110	2.03	2.79
J	0.018	0.025	0.46	0.64
K	0.090	0.110	2.29	2.79
S	0.575	0.625	14.60	15.88
V	0.045	0.055	1.14	1.40

STYLE 2:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

CASE 418B–03
ISSUE C

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