

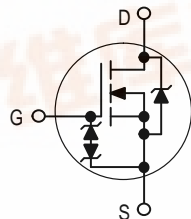
Advance Information

TMOS E-FET™

High Energy Power FET D2PAK for Surface Mount N-Channel Enhancement-Mode Silicon Gate

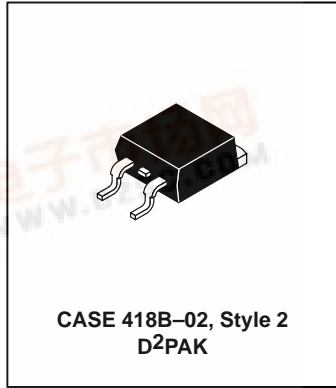
This advanced high voltage TMOS E-FET is designed to withstand high energy in the avalanche mode and switch efficiently. This new high energy device also offers a drain-to-source diode with fast recovery time. Designed for high voltage, high speed switching applications in power supplies, PWM motor controls and other inductive loads, the avalanche energy capability is specified to eliminate the guesswork in designs where inductive loads are switched and offer additional safety margin against unexpected voltage transients.

- Avalanche Energy Capability Specified at Elevated Temperature
- Source-to-Drain Diode Recovery Time Comparable to a Discrete Fast Recovery Diode
- Low Stored Gate Charge for Efficient Switching
- Internal Source-to-Drain Diode Designed to Replace External Zener Transient Suppressor—Absorbs High Energy in the Avalanche Mode
- ESD Protected. Designed to Typically Withstand 400 V Machine Model and 4000 V Human Body Model.



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TMOS POWER FET
55 AMPERES
60 VOLTS
RDS(on) = 18 mΩ



MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain-to-Source Voltage	V _{DSS}	60	Vdc
Drain-to-Gate Voltage (R _{GS} = 1.0 MΩ)	V _{DGR}	60	Vdc
Gate-to-Source Voltage — Continuous	V _{GS}	±20	Vdc
— Non-Repetitive (t _p ≤ 10 ms)	V _{GS(M)}	±40	Vpk
Drain Current — Continuous @ T _C = 25°C	I _D	55	Adc
— Continuous @ T _C = 100°C	I _D	35.5	
— Single Pulse (t _p ≤ 10 μs)	I _{DM}	165	Apk
Total Power Dissipation @ T _C = 25°C	P _D	113	Watts
Derate above 25°C		0.91	W/°C
Total Power Dissipation @ T _A = 25°C (1)		2.5	
Operating and Storage Temperature Range	T _J , T _{stg}	-55 to 150	°C
Single Pulse Drain-to-Source Avalanche Energy — Starting T _J = 25°C (V _{DD} = 25 Vdc, V _{DS} = 60 Vdc, V _{GS} = 10 Vdc, Peak I _L = 55 Apk, L = 0.3 mH, R _G = 25 Ω)	E _{AS}	454	mJ
Thermal Resistance — Junction to Case	R _{θJC}	1.1	°C/W
— Junction to Ambient	R _{θJA}	62.5	
— Junction to Ambient (1)	R _{θJA}	50	
Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 10 seconds	T _L	260	°C

(1) When surface mounted to an FR4 board using the minimum recommended pad size.

This document contains information on a new product. Specifications and information herein are subject to change without notice.

E-FET is a trademark of Motorola, Inc. TMOS is a registered trademark of Motorola, Inc.



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ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage (V _{GS} = 0 Vdc, I _D = 250 μAdc) Temperature Coefficient (Positive)	(Cpk ≥ 2.0) V _{(BR)DSS}	60 —	— 53	— —	Vdc mV/°C
Zero Gate Voltage Drain Current (V _{DS} = 60 Vdc, V _{GS} = 0 Vdc) (V _{DS} = 60 Vdc, V _{GS} = 0 Vdc, T _J = 125°C)	I _{DSS}	— —	— —	1.0 10	μAdc
Gate-Body Leakage Current (V _{GS} = ±20 Vdc, V _{DS} = 0 Vdc)	I _{GSS}	—	—	100	nAdc

ON CHARACTERISTICS (1)

Gate Threshold Voltage (V _{DS} = V _{GS} , I _D = 250 μAdc) Threshold Temperature Coefficient (Negative)	(Cpk ≥ 2.0) V _{GS(th)}	2.0 —	3.0 6.0	4.0 —	Vdc mV/°C
Static Drain-to-Source On-Resistance (V _{GS} = 10 Vdc, I _D = 27.5 Adc)	(Cpk ≥ 2.0) R _{DS(on)}	—	14	18	mΩ
Drain-to-Source On-Voltage (V _{GS} = 10 Vdc) (I _D = 55 Adc) (I _D = 27.5 Adc, T _J = 125°C)	V _{DS(on)}	— —	0.825 0.74	1.2 1.0	Vdc
Forward Transconductance (V _{DS} = 4.0 Vdc, I _D = 27.5 Adc)	g _{FS}	12	15	—	Mhos

DYNAMIC CHARACTERISTICS

Input Capacitance	(V _{DS} = 25 Vdc, V _{GS} = 0 Vdc, f = 1.0 MHz)	C _{iss}	—	1390	1950	pF
Output Capacitance		C _{oss}	—	520	730	
Transfer Capacitance		C _{rss}	—	119	238	

SWITCHING CHARACTERISTICS (2)

Turn-On Delay Time	(V _{DD} = 30 Vdc, I _D = 55 Adc, V _{GS(on)} = 10 Vdc, R _G = 9.1 Ω)	t _{d(on)}	—	27	54	ns
Rise Time		t _r	—	157	314	
Turn-Off Delay Time		t _{d(off)}	—	116	232	
Fall Time		t _f	—	126	252	
Gate Charge (See Figure 8)	(V _{DS} = 48 Vdc, I _D = 55 Adc, V _{GS} = 10 Vdc)	Q _T	—	40	56	nC
		Q ₁	—	7.0	—	
		Q ₂	—	18	—	
		Q ₃	—	15	—	

SOURCE-DRAIN DIODE CHARACTERISTICS

Forward On-Voltage	(I _S = 55 Adc, V _{GS} = 0 Vdc) (I _S = 55 Adc, V _{GS} = 0 Vdc, T _J = 125°C)	V _{SD}	— —	0.93 0.82	1.1 —	Vdc
Reverse Recovery Time	(I _S = 55 Adc, V _{GS} = 0 Vdc, dI _S /dt = 100 A/μs)	t _{rr}	—	57	—	ns
		t _a	—	32	—	
		t _b	—	25	—	
Reverse Recovery Stored Charge		Q _{RR}	—	0.11	—	μC

INTERNAL PACKAGE INDUCTANCE

Internal Drain Inductance (Measured from contact screw on tab to center of die) (Measured from drain lead 0.25" from package to center of die)	L _D	— —	3.5 4.5	— —	nH
Internal Source Inductance (Measured from the source lead 0.25" from package to source bond pad)	L _S	—	7.5	—	

- (1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
- (2) Switching characteristics are independent of operating junction temperature.

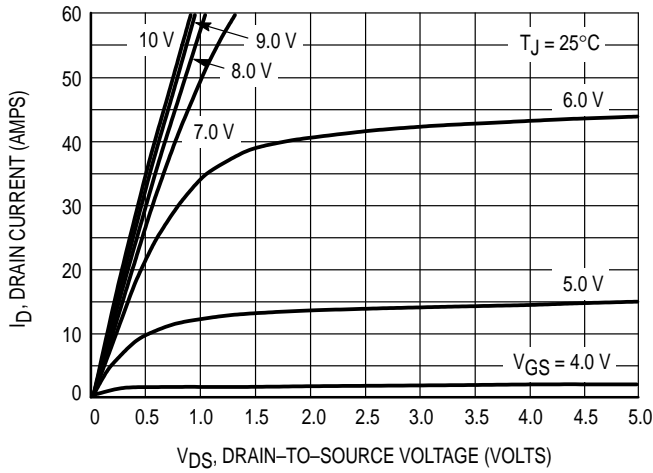


Figure 1. On-Region Characteristics

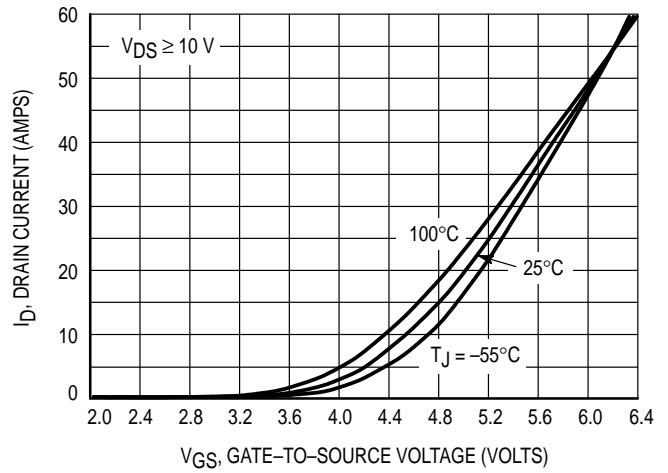


Figure 2. Transfer Characteristics

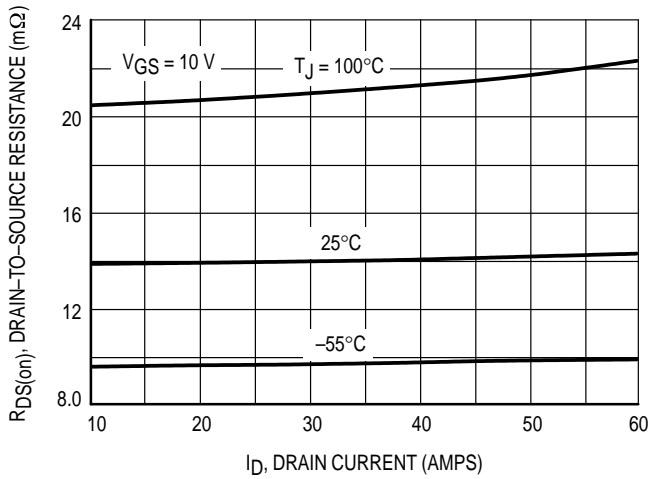


Figure 3. On-Resistance versus Drain Current and Temperature

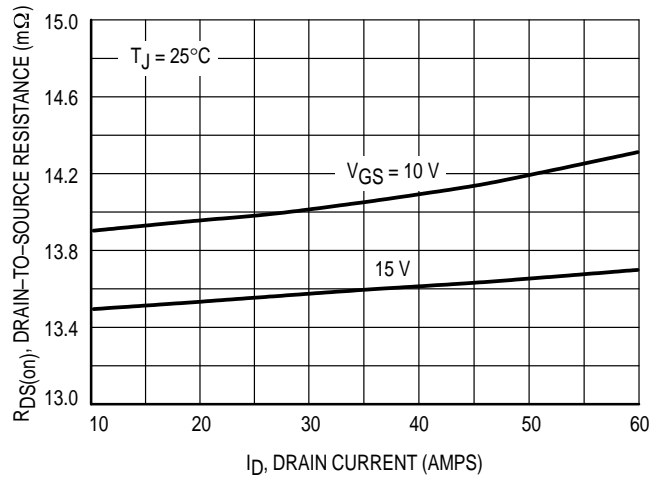


Figure 4. On-Resistance versus Drain Current and Gate Voltage

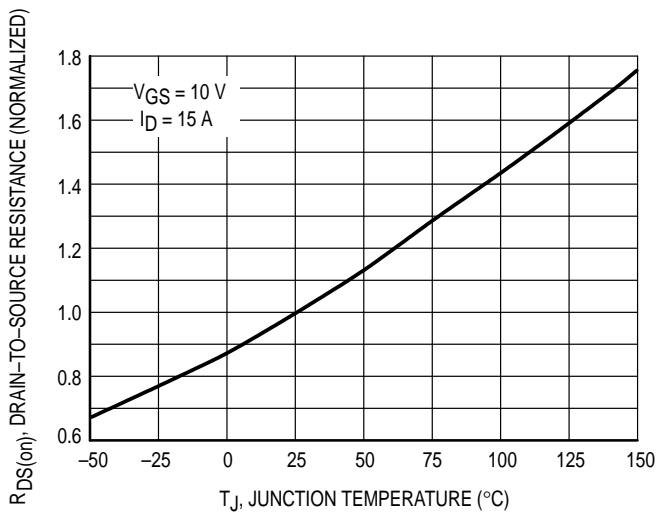


Figure 5. On-Resistance Variation with Temperature

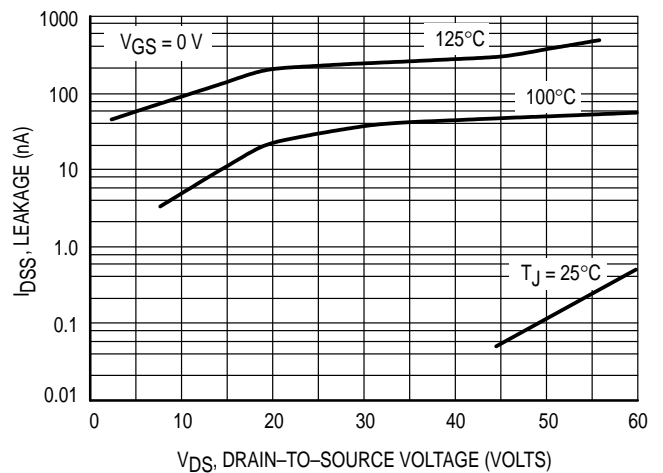


Figure 6. Drain-to-Source Leakage Current versus Voltage

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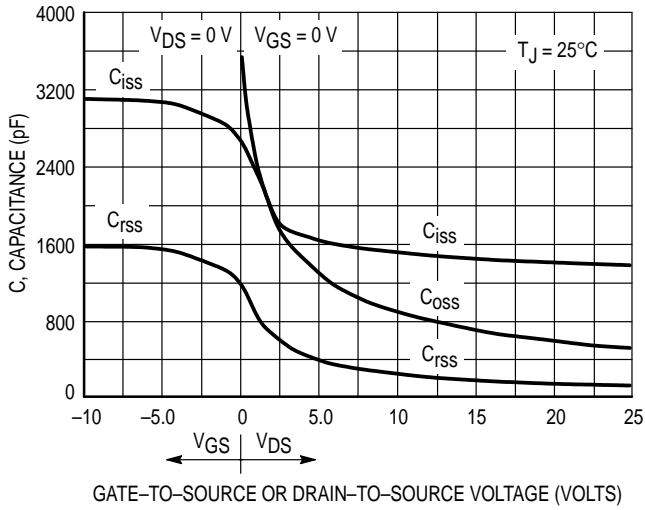


Figure 7. Capacitance Variation

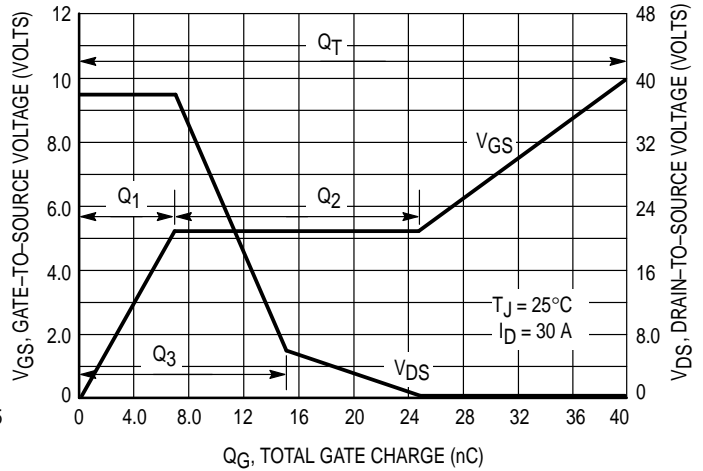


Figure 8. Gate-to-Source and Drain-to-Source Voltage versus Total Charge

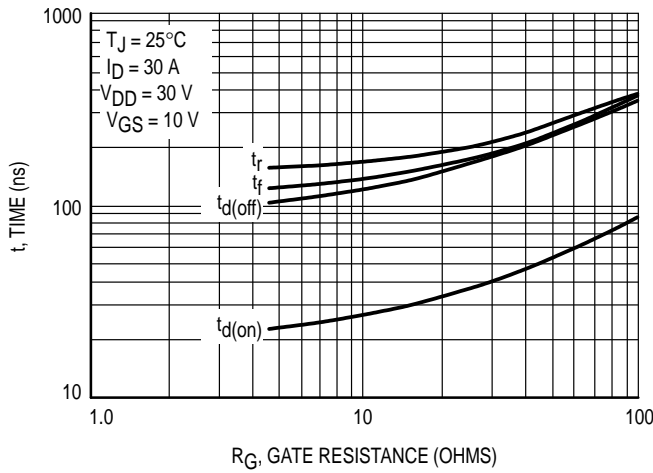


Figure 9. Resistive Switching Time Variation versus Gate Resistance

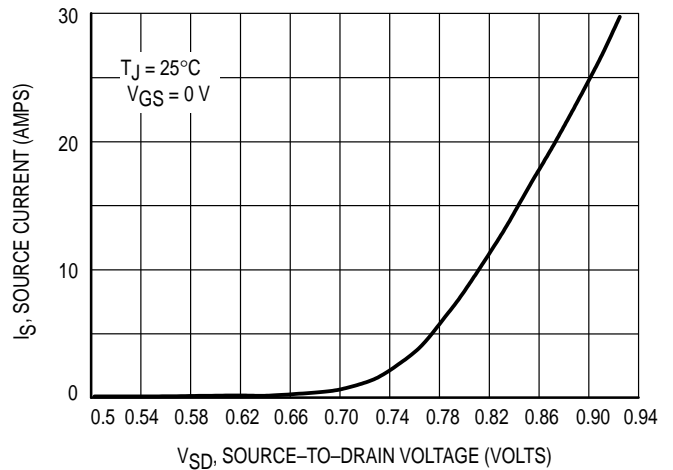


Figure 10. Diode Forward Voltage versus Current

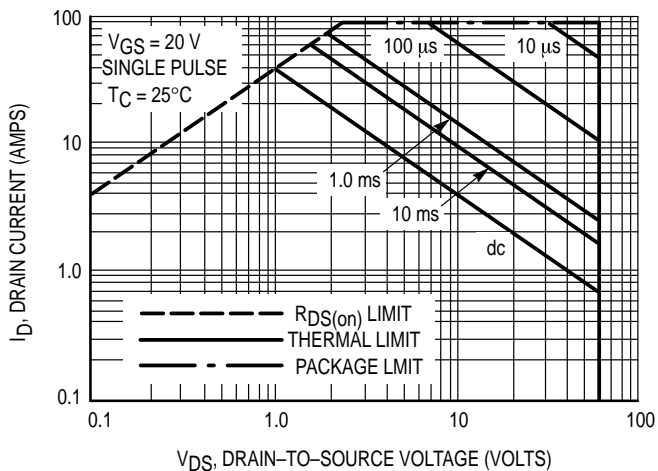


Figure 11. Maximum Rated Forward Biased Safe Operating Area

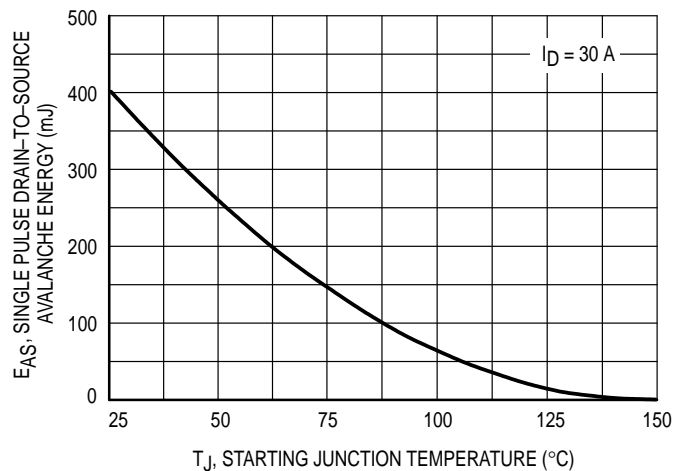


Figure 12. Maximum Avalanche Energy versus Starting Junction Temperature

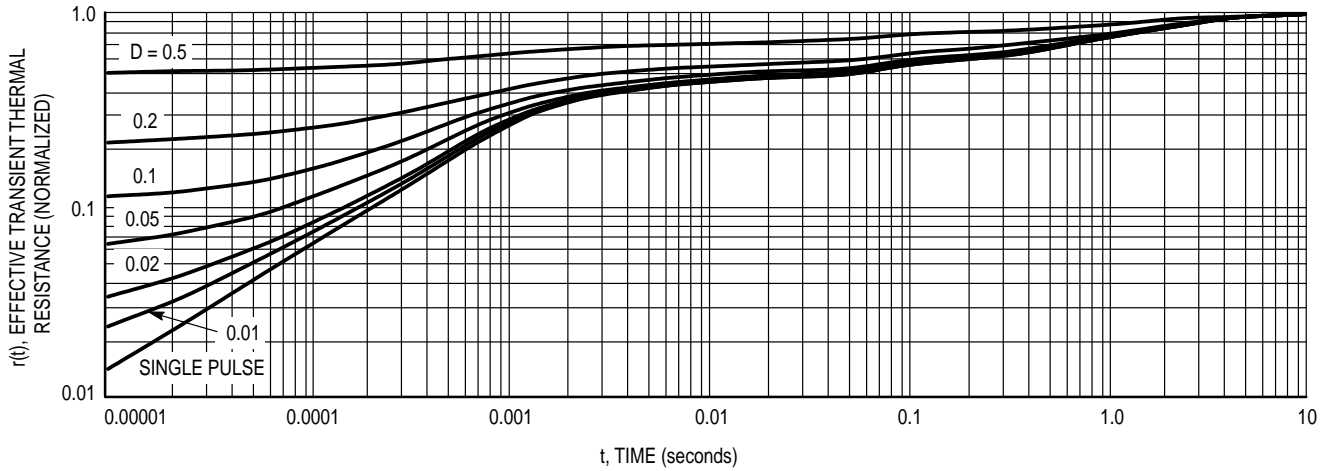
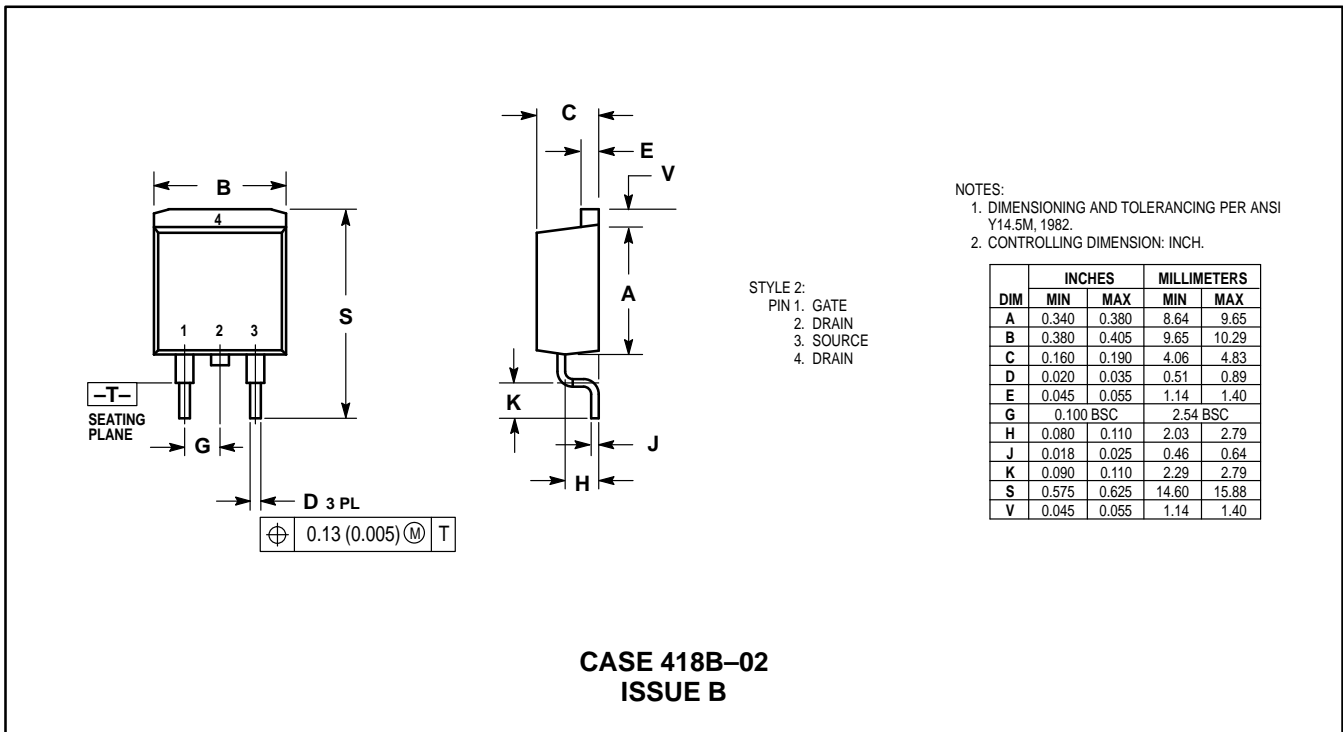



Figure 13. Thermal Response

PACKAGE DIMENSIONS



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How to reach us:

USA/EUROPE/Locations Not Listed: Motorola Literature Distribution;
P.O. Box 5405, Denver, Colorado 80217. 303-675-2140 or 1-800-441-2447

JAPAN: Nippon Motorola Ltd.; Tatsumi-SPD-JLDC, 6F Seibu-Butsuryu-Center,
3-14-2 Tatsumi Koto-Ku, Tokyo 135, Japan. 81-3-3521-8315

Mfax™: RMFAX0@email.sps.mot.com – TOUCHTONE 602-244-6609
– US & Canada ONLY 1-800-774-1848

ASIA/PACIFIC: Motorola Semiconductors H.K. Ltd.; 8B Tai Ping Industrial Park,
51 Ting Kok Road, Tai Po, N.T., Hong Kong. 852-26629298

INTERNET: <http://www.mot.com/SPS/>



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