

**MYSON  
TECHNOLOGY**

**MTD658E**

**5/8 Port 10/100 Hub Build\_in Bridge And Memory**

**FEATURES**

- IEEE802.3 Clause 9 and IEEE802.3u Clause 27 compliant.
- Provide 8 RMI (8 port mode), or 4 RMI + 1 MII (5 port mode).
- Provide 2 inter\_repeater stacking bus for 10M and 100M port expansion each.
- Support stacking to 4 units without any external arbitration logic ( if use external arbitration logic, theoretically can stack to 6 units and up).
- Build\_in 2 port switch controller, support up to 2048 MAC addresses filtering database.
- Optional back\_pressure flow control.
- Optional up\_link\_switch port function (in slave hub), support 100FX 2km distance extension in 100FD mode.
- Meet Class\_2 repeater specification for 100M\_hub.
- Pin compatible with MTD658/655 application, no need any external memory buffers.
- 128 pin QFP package, 3.3V operation voltage.

**GENERAL DESCRIPTION**

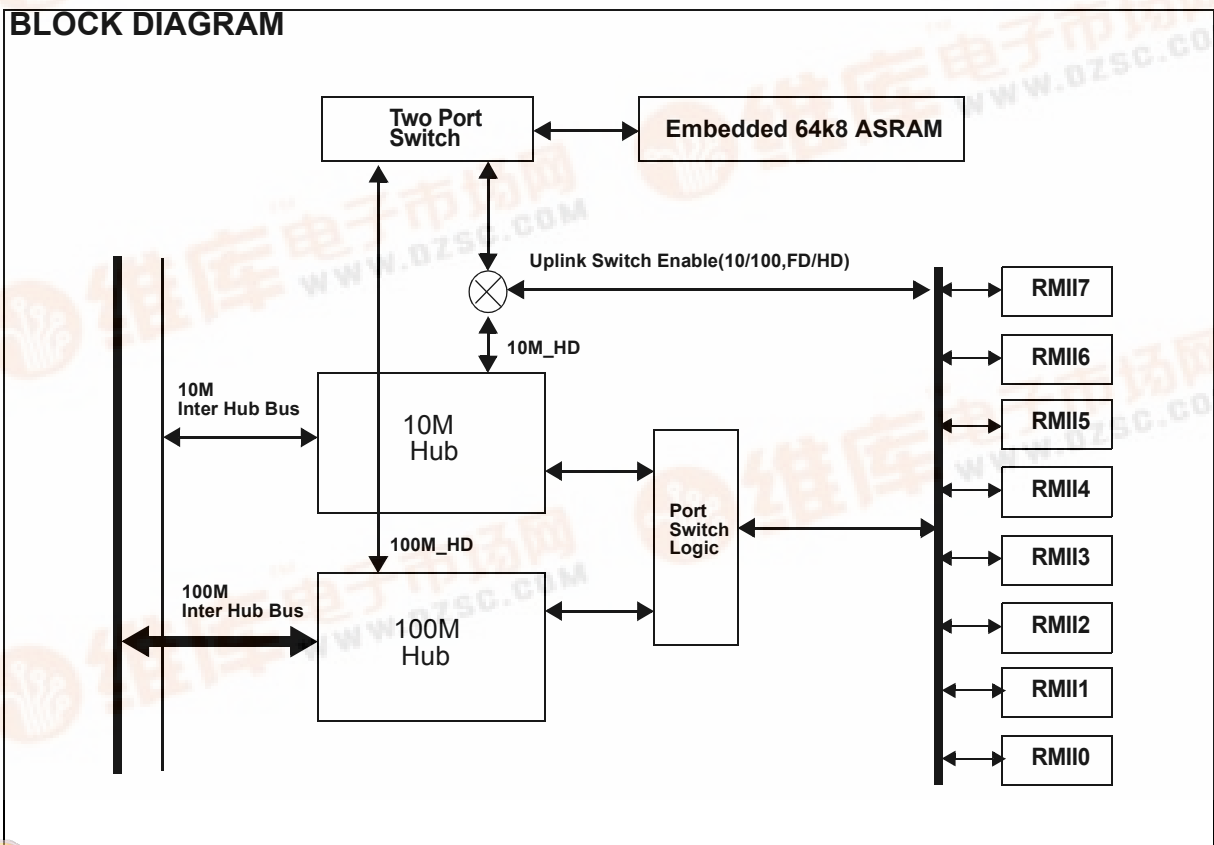
The MTD658E is a highly integrated, 10M/100M dual speed hub with build\_in 2 port switch and 64k8 embedded ASRAM. Support 8 RMI ports for 10M/100M operation, and really meet 100M\_hub class\_2 spec when connect with external QPHYceivers.

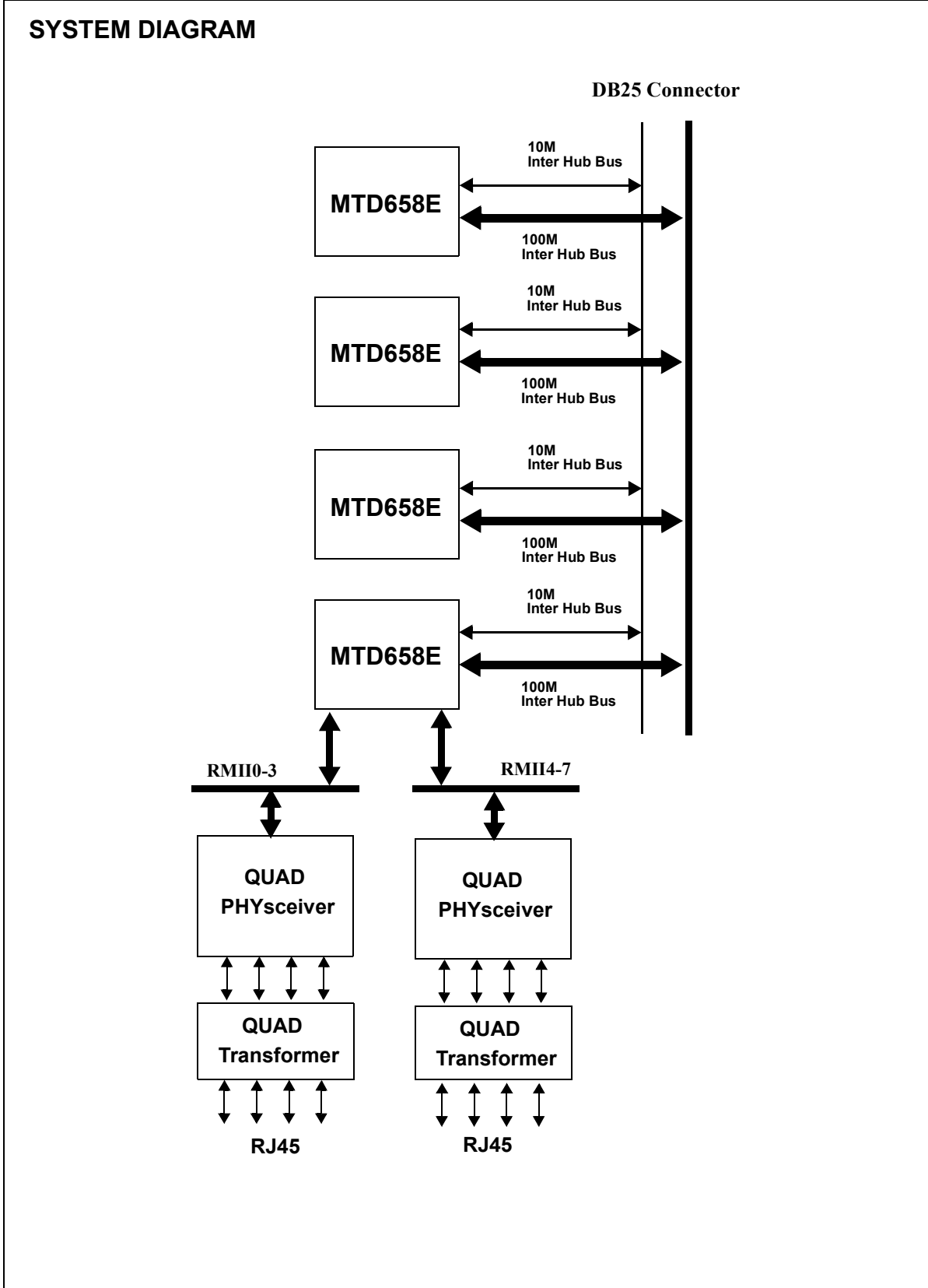
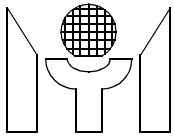
The MTD658E provides two Inter-repeater stacking bus for 10M and 100M expansion each, easily stack to 4 units without any external arbitration logic. If using external arbitration logic and proper bus driver, can stack to 6 units and up.

The build\_in 2 port switch, support 2k MAC addresses filtering, and use embedded asynchronous high speed SRAM (64k\*8) for packet buffering. This 2 port switch can also be configured to be up\_link switch when hub is under slave mode.

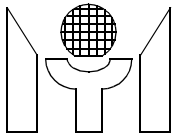
The MTD658E also support an simple and effective LED display function, provide 10M\_col, 100M\_col, and per port's partition status.

**BLOCK DIAGRAM**

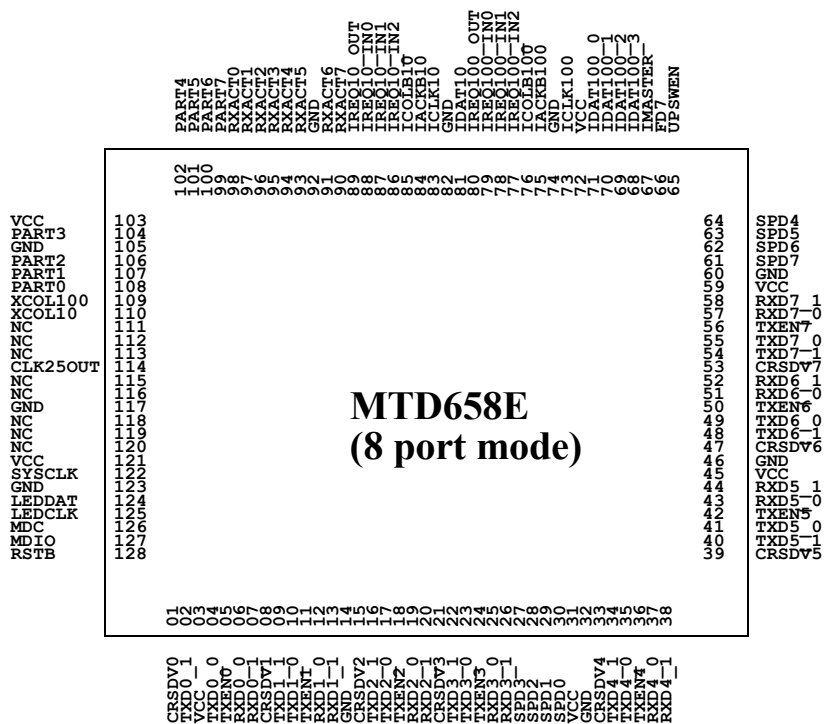


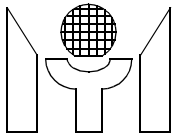


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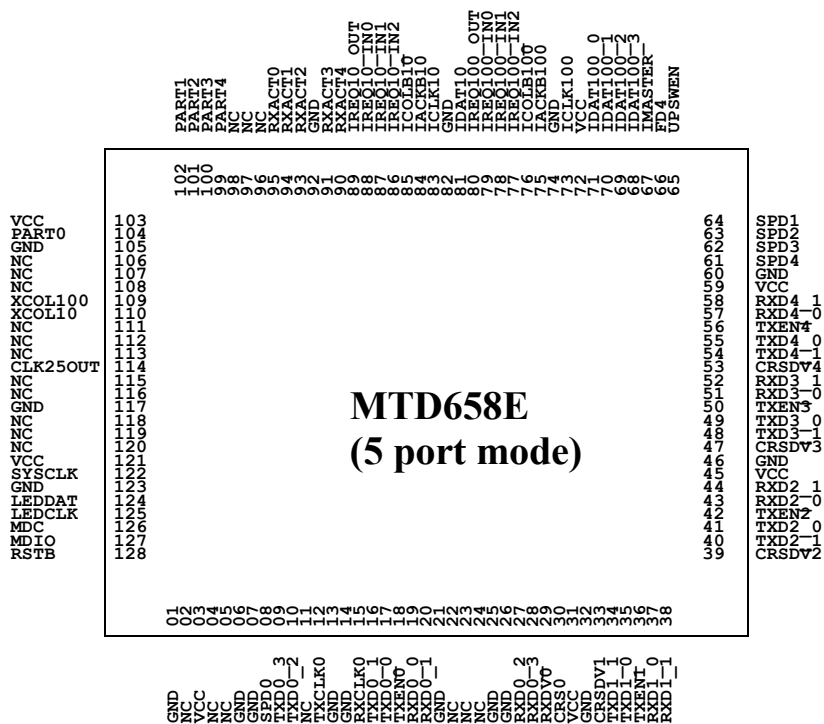


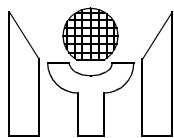
1.0 PIN CONNECTION (for 8 port mode)





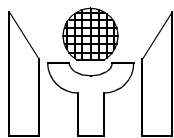
**2.0 PIN CONNECTION (for 5 port mode)**





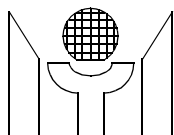
**3.0 PIN DESCRIPTIONS (for 8 port mode)**

<b>RMII Port Interface Pins (for 8 port mode)</b>			
<b>Name</b>	<b>Pin Number</b>	<b>I/O</b>	<b>Descriptions</b>
CRSDV0	1	I	Port0 RMII receive interface signal, CRSDV0 is asserted high when port0 media is non_idle.
RXD0_0	6	I	Port0 RMII receive data bit_0.
RXD0_1	7	I	Port0 RMII receive data bit_1.
TXEN0	5	O	Port0 RMII transmit enable signal.
TXD0_0	4	O	Port0 RMII transmit data bit_0.
TXD0_1	2	O	Port0 RMII transmit data bit_1.
CRSDV1	8	I	Port1 RMII receive interface signal, CRSDV1 is asserted high when port1 media is non_idle.
RXD1_0	12	I	Port1 RMII receive data bit_0.
RXD1_1	13	I	Port1 RMII receive data bit_1.
TXEN1	11	O	Port1 RMII transmit enable signal.
TXD1_0	10	O	Port1 RMII transmit data bit_0.
TXD1_1	9	O	Port1 RMII transmit data bit_1.
CRSDV2	15	I	Port2 RMII receive interface signal, CRSDV2 is asserted high when port2 media is non_idle.
RXD2_0	19	I	Port2 RMII receive data bit_0.
RXD2_1	20	I	Port2 RMII receive data bit_1.
TXEN2	18	O	Port2 RMII transmit enable signal.
TXD2_0	17	O	Port2 RMII transmit data bit_0.
TXD2_1	16	O	Port2 RMII transmit data bit_1.
CRSDV3	21	I	Port3 RMII receive interface signal, CRSDV3 is asserted high when port3 media is non_idle.
RXD3_0	25	I	Port3 RMII receive data bit_0.
RXD3_1	26	I	Port3 RMII receive data bit_1.
TXEN3	24	O	Port3 RMII transmit enable signal.
TXD3_0	23	O	Port3 RMII transmit data bit_0.
TXD3_1	22	O	Port3 RMII transmit data bit_1.
CRSDV4	33	I	Port4 MII receive interface signal, CRSDV4 is asserted high when port4 media is non_idle.
RXD4_0	37	I	Port4 RMII receive data bit_0.
RXD4_1	38	I	Port4 RMII receive data bit_1.
TXEN4	36	O	Port4 RMII transmit enable signal.
TXD4_0	35	O	Port4 RMII transmit data bit_0.
TXD4_1	34	O	Port4 RMII transmit data bit_1.
CRSDV5	39	I	Port5 RMII receive interface signal, CRSDV5 is asserted high when port5 media is non_idle.
RXD5_0	43	I	Port5 RMII receive data bit_0.
RXD5_1	44	I	Port5 RMII receive data bit_1.
TXEN5	42	O	Port5 RMII transmit enable signal.
TXD5_0	41	O	Port5 RMII transmit data bit_0.
TXD5_1	40	O	Port5 RMII transmit data bit_1.



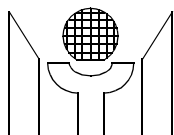
<b>RMII Port Interface Pins (for 8 port mode)</b>			
<b>Name</b>	<b>Pin Number</b>	<b>I/O</b>	<b>Descriptions</b>
CRSDV6	47	I	Port6 RMII receive interface signal, CRSDV6 is asserted high when port6 media is non_idle.
RXD6_0	51	I	Port6 RMII receive data bit_0.
RXD6_1	52	I	Port6 RMII receive data bit_1.
TXEN6	50	O	Port6 RMII transmit enable signal.
TXD6_0	49	O	Port6 RMII transmit data bit_0.
TXD6_1	48	O	Port6 RMII transmit data bit_1.
CRSDV7	53	I	Port7 RMII receive interface signal, CRSDV7 is asserted high when port7 media is non_idle.
RXD7_0	57	I	Port7 RMII receive data bit_0.
RXD7_1	58	I	Port7 RMII receive data bit_1.
TXEN7	56	O	Port7 RMII transmit enable signal.
TXD7_0	55	O	Port7 RMII transmit data bit_0.
TXD7_1	54	O	Port7 RMII transmit data bit_1.

<b>10M Inter-Bus Interface pins (for 8 port mode)</b>			
<b>Name</b>	<b>Pin Number</b>	<b>I/O</b>	<b>Descriptions</b>
IMASTER	67	I	Master hub selection: when high: means hub internal inter_bus arbiter is enabled and hub internal two_port switch is well conneted to 10M_hub core and 100M_hub core . when low: means hub internal inter_bus arbiter is disabled and hub internal two_port switch is not connected to 10M_hub core and 100M_hub core.
IACKB10	84	I/O	10M Inter-Bus port access acknowledge signal (low active). For master hub, this pin is output; for slave hub is input, or while EXT_ARB jumper was set to high, this pin is input from an external arbitration device.
ICOLB10	85	I/O	10M Inter-Bus collision signal (low active). For master hub, this pin can output multi hub collision event to inform all slave hub ; for slave hub, this pin is an input, or while EXT_ARB jumper was set to high, this pin is input from an external arbitration device.
IREQ10_IN0	88	I	10M Inter-Bus port access request input.
IREQ10_IN1	87	I	10M Inter-Bus port access request input.
IREQ10_IN2	86	I	10M Inter-Bus port access request input.
IREQ10_OUT	89	O	10M Inter-Bus port access request output.
ICLK10	83	I/O	10M Inter-Bus port clock.
IDAT10	81	I/O	10M Inter-Bus port data bit



<b>100M Inter-Bus Interface pins (for 8 port mode)</b>			
<b>Name</b>	<b>Pin Number</b>	<b>I/O</b>	<b>Descriptions</b>
IACKB100	75	I/O	100M Inter-Bus port access acknowledge signal (low active). For master hub, this pin is output; for slave hub is input, or while EXT_ARB jumper was set to high, this pin is input from an external arbitration device.
ICOLB100	76	I/O	100M Inter-Bus collision signal (low active). For master hub, this pin can output multi hub collision event to inform all slave hub ; for slave hub, this pin is an input, or while EXT_ARB jumper was set to high, this pin is input from an external arbitration device.
IREQ100_IN0	79	I	100M Inter-Bus port access request input.
IREQ100_IN1	78	I	100M Inter-Bus port access request input.
IREQ100_IN2	77	I	100M Inter-Bus port access request input.
IREQ100_OUT	80	O	100M Inter-Bus port access request output.
ICLK100	73	I/O	100M Inter-Bus port clock.
IDAT100_0	71	I/O	100M Inter-Bus port data bit 0.
IDAT100_1	70	I/O	100M Inter-Bus port data bit 1.
IDAT100_2	69	I/O	100M Inter-Bus port data bit 2.
IDAT100_3	68	I/O	100M Inter-Bus port data bit 3.

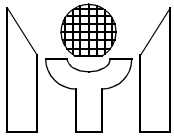
<b>LED Interface Pins (for 8 port mode)</b>			
<b>Name</b>	<b>Pin Number</b>	<b>I/O</b>	<b>Descriptions</b>
RXACT7-0	90,91,93,94, 95,96,97,98	I/O	Port 7-0 Rx Activity LED Outputs, low_active. Direct output per port receive activity status for LED display.
PART7-0	99,100,101, 102,104,106, 107,108	I/O	Port 7-0 Partition LED Outputs, low_active. Direct output per port partition status for LED display. During power on reset PART7 pin use as MII setting start PHY device ID selection. 4.7K pull up resistor will set PHY device ID from 5h08 - 5h0f, no pull up 4.7k resistor will set PHY device ID from 5h04 -5h0b.
XCOL100	109	I/O	100M Hub Collision LED Output, low_active.
XCOL10	110	I/O	10M Hub Collision LED Output, low_active.



<b>LED Interface Pins (for 8 port mode)</b>			
<b>Name</b>	<b>Pin Number</b>	<b>I/O</b>	<b>Descriptions</b>
LEDDAT	124	I/O	LED display serial data out, high_active; mapping for LEDCLK signal's burst clock, its serial out data sequence is: (first bit be shifted out is from b00, and end of burst bit is b23) b00: port0 partition    b08: 10hub_col        b16: port0 rx_activity b01: port1 partition    b09: 100hub_col       b17: port1 rx_activity b02: port2 partition    b10: asram_test_fail    b18: port2 rx_activity b03: port3 partition    b11: port3 partition    b19: port3 rx_activity b04: port4 partition    b12: port4 partition    b20: port4 rx_activity b05: port5 partition    b13: port5 partition    b21: port5 rx_activity b06: port6 partition    b14: port6 partition    b22: port6 rx_activity b07: port7 partition    b15: port7 partition    b23: port7 rx_activity
LEDCLK	125	I/O	LED display clock signal; the signal is a discontinued clock for LED data serial shift out. Every clock burst have 24 cycles (period: 160 ns), and the clock burst will be repeated with every 42ms.

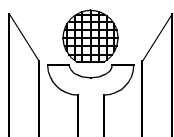
<b>Miscellaneous Pins (for 8 port mode)</b>			
<b>Name</b>	<b>Pin Number</b>	<b>I/O</b>	<b>Descriptions</b>
RSTB	128	I	System reset input, low active.
SYSCLK	122	I	50MHz system clock input.
CLK25MOUT	114	I/O	25MHz clock output.
MDC	126	I/O	MII management clock inout.
MDIO	127	I/O	MII management data inout.
UPSWEN	65	I	Up_link switch port enabling: one of internal two_port switch port will connect to 100M_hub domain, and another port will redirect to RMII port7.
FD7	66	I	When up_link switch port enabling, this pin is port7's full_duplex indicator, input from PHY. When high, indicate port7 in running on full_duplex mode. When low, indicate on half_duplex mode.
SPD0	30	I	Port0 speed indicator, input from PHY. SPD0 input low: 100M, input high: 10M.
SPD1	29	I	Port1 speed indicator, input from PHY. SPD1 input low: 100M, input high: 10M.
SPD2	28	I	Port2 speed indicator, input from PHY. SPD2 input low: 100M, input high: 10M.
SPD3	27	I	Port3 speed indicator, input from PHY. SPD3 input low: 100M, input high: 10M.
SPD4	64	I	Port4 speed indicator, input from PHY. SPD4 input low: 100M, input high: 10M.
SPD5	63	I	Port5 speed indicator, input from PHY. SPD5 input low: 100M, input high: 10M.
SPD6	62	I	Port6 speed indicator, input from PHY. SPD6 input low: 100M, input high: 10M.





<b>Miscellaneous Pins (for 8 port mode)</b>			
<b>Name</b>	<b>Pin Number</b>	<b>I/O</b>	<b>Descriptions</b>
SPD7	61	I	Port7 speed indicator, input from PHY. SPD7 input low: 100M , input high: 10M.
VCC	3,31,45,59, 72,103,121	PWR	Power pins
GND	14,32,46,60, 74,82,92,105 ,117,123	GND	Ground pins
NC_pin	111,112,113, 115,116,118, 119,120	NC	No connection pins

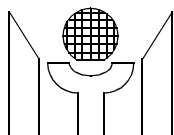
<b>Power On Configuration Set Up Table (for 8 port mode)</b>			
<b>Name</b>	<b>Pin Number</b>	<b>I/O</b>	<b>Descriptions</b>
TXEN2	18	I/O	Back_pressure disable : ( power on external jumper configuration ) - external pull_low (default) : normal mode (back_pressure enable) - external pull_high: back_pressure disable
TXEN5	42	I/O	Auto MII_setting bypass : ( power on external jumper configuration ) - external pull_low (default) : normal mode ( auto MII_setting); after power_on, MTD658E will auto setup PHY devices be forced in half duplex mode for repeater application. - external pull_high: auto MII_setting bypass
PART7	99	I/O	PHY_ID 5h8 starting enable :(power on external jumper configuration) - external pull_low (default) : MII setting PHY_ID start address from 5h04 to 5h0b. - external pull_high: MII setting PHY_ID start address from 5h08 to 5h0f.
MDC	126	I/O	1522 bytes packet accept enable : ( power on external jumper configuration ) - external pull_low (default) : normal mode ( <=1518 bytes packet accept) - external pull_high: <= 1522 bytes packet accept
LEDDAT	124	I/O	External arbiter enable : ( power on external jumper configuration ) - external pull_low (default) : normal mode (inter_repeater bus use internal arbiter) - external pull_high: inter_repeater bus use external arbiter .



## 4.0 PIN DESCRIPTIONS (for 5 port mode)

MII Port (port0) Interface Pins (for 5 port mode)			
Name	Pin Number	I/O	Descriptions
RXD0_0	19	I	Port0 MII receive data bit_0.
RXD0_1	20	I	Port0 MII receive data bit_1.
RXD0_2	27	I	Port0 MII receive data bit_2.
RXD0_3	28	I	Port0 MII receive data bit_3.
CRSO	30	I	Port0 MII asynchronous carrier indicator from PHY device.
RXDV0	29	I	Port0 MII synchronous receive data valid signal from PHY device.
RXCLK0	15	I	Port0 MII receive clock.
TXEN0	18	O	Port0 MII transmit enable signal.
TXD0_0	17	O	Port0 MII transmit data bit_0.
TXD0_1	16	O	Port0 MII transmit data bit_1.
TXD0_2	10	O	Port0 MII transmit data bit_2.
TXD0_3	9	O	Port0 MII transmit data bit_3.
TXCLK0	12	I	Port0 MII transmit clock.

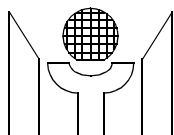
RMII Port (port1~port4) Interface Pins (for 5 port mode)			
Name	Pin Number	I/O	Descriptions
CRSDV1	33	I	Port1 RMII receive interface signal, CRSDV1 is asserted high when port1 media is non_idle.
RXD1_0	37	I	Port1 RMII receive data bit_0.
RXD1_1	38	I	Port1 RMII receive data bit_1.
TXEN1	36	O	Port1 RMII transmit enable signal.
TXD1_0	35	O	Port1 RMII transmit data bit_0.
TXD1_1	34	O	Port1 RMII transmit data bit_1.
CRSDV2	39	I	Port2 RMII receive interface signal, CRSDV2 is asserted high when port2 media is non_idle.
RXD2_0	43	I	Port2 RMII receive data bit_0.
RXD2_1	44	I	Port2 RMII receive data bit_1.
TXEN2	42	O	Port2 RMII transmit enable signal.
TXD2_0	41	O	Port2 RMII transmit data bit_0.
TXD2_1	40	O	Port2 RMII transmit data bit_1.
CRSDV3	47	I	Port3 RMII receive interface signal, CRSDV3 is asserted high when port3 media is non_idle.
RXD3_0	51	I	Port3 RMII receive data bit_0.
RXD3_1	52	I	Port3 RMII receive data bit_1.
TXEN3	50	O	Port3 RMII transmit enable signal.
TXD3_0	49	O	Port3 RMII transmit data bit_0.
TXD3_1	48	O	Port3 RMII transmit data bit_1.
CRSDV4	53	I	Port4 RMII receive interface signal, CRSDV4 is asserted high when port4 media is non_idle.



<b>RMII Port (port1~port4) Interface Pins (for 5 port mode)</b>			
<b>Name</b>	<b>Pin Number</b>	<b>I/O</b>	<b>Descriptions</b>
RXD4_0	57	I	Port4 RMII receive data bit_0.
RXD4_1	58	I	Port4 RMII receive data bit_1.
TXEN4	56	O	Port4 RMII transmit enable signal.
TXD4_0	55	O	Port4 RMII transmit data bit_0.
TXD4_1	54	O	Port4 RMII transmit data bit_1.

<b>10M Inter-Bus Interface pins (for 5 port mode)</b>			
<b>Name</b>	<b>Pin Number</b>	<b>I/O</b>	<b>Descriptions</b>
IMASTER	67	I	Master hub selection: when high: means hub internal inter_bus arbiter is enabled and hub internal two_port switch is well conneted to 10M_hub core and 100M_hub core . when low: means hub internal inter_bus arbiter is disabled and hub internal two_port switch is not connected to 10M_hub core and 100M_hub core.
IACKB10	84	I/O	10M Inter-Bus port access acknowledge signal (low active). For master hub, this pin is output; for slave hub is input, or while EXT_ARB jumper was set to high, this pin is input from an external arbitration device.
ICOLB10	85	I/O	10M Inter-Bus collision signal (low active). For master hub, this pin can output multi hub collision event to inform all slave hub ; for slave hub, this pin is an input, or while EXT_ARB jumper was set to high, this pin is input from an external arbitration device.
IREQ10_IN0	88	I	10M Inter-Bus port access request input.
IREQ10_IN1	87	I	10M Inter-Bus port access request input.
IREQ10_IN2	86	I	10M Inter-Bus port access request input.
IREQ10_OUT	89	O	10M Inter-Bus port access request output.
ICLK10	83	I/O	10M Inter-Bus port clock.
IDAT10	81	I/O	10M Inter-Bus port data bit

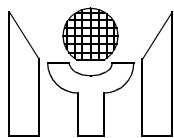
<b>100M Inter-Bus Interface pins (for 5 port mode)</b>			
<b>Name</b>	<b>Pin Number</b>	<b>I/O</b>	<b>Descriptions</b>
IACKB100	75	I/O	100M Inter-Bus port access acknowledge signal (low active). For master hub, this pin is output; for slave hub is input, or while EXT_ARB jumper was set to high, this pin is input from an external arbitration device.
ICOLB100	76	I/O	100M Inter-Bus collision signal (low active). For master hub, this pin can output multi hub collision event to inform all slave hub ; for slave hub, this pin is an input, or while EXT_ARB jumper was set to high, this pin is input from an external arbitration device.
IREQ100_IN0	79	I	100M Inter-Bus port access request input.
IREQ100_IN1	78	I	100M Inter-Bus port access request input.
IREQ100_IN2	77	I	100M Inter-Bus port access request input.
IREQ100_OUT	80	O	100M Inter-Bus port access request output.



<b>100M Inter-Bus Interface pins (for 5 port mode)</b>			
<b>Name</b>	<b>Pin Number</b>	<b>I/O</b>	<b>Descriptions</b>
ICLK100	73	I/O	100M Inter-Bus port clock.
IDAT100_0	71	I/O	100M Inter-Bus port data bit 0.
IDAT100_1	70	I/O	100M Inter-Bus port data bit 1.
IDAT100_2	69	I/O	100M Inter-Bus port data bit 2.
IDAT100_3	68	I/O	100M Inter-Bus port data bit 3.

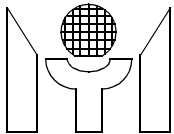
<b>LED Interface Pins (for 5 port mode)</b>			
<b>Name</b>	<b>Pin Number</b>	<b>I/O</b>	<b>Descriptions</b>
RXACT4-0	90,91,93,94, 95	I/O	Port 4-0 Rx Activity LED Outputs, low_active. Direct output per port receive activity status for LED display.
PART4-0	99,100,101, 102,104	I/O	Port 4-0 Partition LED Outputs, low_active. Direct output per port partition status for LED display. During power on reset PART4 pin use as MII setting start PHY device ID selection. 4.7K pull up resistor will set PHY device ID from 5h08 - 5h0f, no pull up 4.7k resistor will set PHY device ID from 5h04 -5h0b.
XCOL100	109	I/O	100M Hub Collision LED Output, low_active.
XCOL10	110	I/O	10M Hub Collision LED Output, low_active.
LEDDAT	124	I/O	LED display serial data out, high_active; mapping for LEDCLK signal's burst clock , its serial out data sequence is : ( first bit be shifted out is from b00, and end of burst bit is b23)  b00: *****    b08: 10hub_col        b16: ***** b01: *****    b09: 100hub_col        b17: ***** b02: *****    b10: asram_test_fail    b18: ***** b03: port0 partition    b11: port0 partition    b19: port0 rx_activity b04: port1 partition    b12: port1 partition    b20: port1 rx_activity b05: port2 partition    b13: port2 partition    b21: port2 rx_activity b06: port3 partition    b14: port3 partition    b22: port3 rx_activity b07: port4 partition    b15: port4 partition    b23: port4 rx_activity
LEDCLK	125	I/O	LED display clock signal, the signal is a discontinued clock for LED data serial shift out. Every clock burst have 24 cycles ( period : 160 ns), and the clock burst will be repeated with every 42ms.

<b>Miscellaneous Pins (for 5 port mode)</b>			
<b>Name</b>	<b>Pin Number</b>	<b>I/O</b>	<b>Descriptions</b>
RSTB	128	I	System reset input, low active.
SYSCLK	122	I	50MHz system clock input
CLK25MOUT	114	I/O	25MHz clock output.
MDC	126	I/O	MII management clock inout
MDIO	127	I/O	MII management data inout

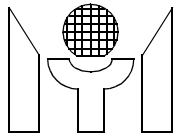


<b>Miscellaneous Pins (for 5 port mode)</b>			
<b>Name</b>	<b>Pin Number</b>	<b>I/O</b>	<b>Descriptions</b>
UPSWEN	65	I	Up_link switch port enabling : one of internal two_port switch port will connect to 100M_hub domain, and another port will redirect to RMII port4.
FD4	66	I	When up_link switch port enabling, this pin is port4's full_duplex indicator, input from PHY. When high , indicate port4 in running on full_duplex mode. When low, indicate on half_duplex mode.
SPD0	8	I	Port0 speed indicator, input from PHY. SPD0 input low: 100M , input high: 10M.
SPD1	64	I	Port1 speed indicator, input from PHY. SPD1 input low: 100M , input high: 10M.
SPD2	63	I	Port2 speed indicator, input from PHY. SPD2 input low: 100M , input high: 10M.
SPD3	62	I	Port3 speed indicator, input from PHY. SPD3 input low: 100M , input high: 10M.
SPD4	61	I	Port4 speed indicator, input from PHY. SPD4 input low: 100M , input high: 10M.
NC_pin	2,4,5,11,22, 23,24,96,97, 98,106,107, 108,111,112, 113,115,116, 118,119,120	NC	No connection pins
VCC	3,31,45,59, 72,103,121	PWR	Power pins
GND	1,6,7,13,14, 21,25,26,32, 46,60,74,82, 92,105,117, 123	GND	Ground pins

<b>Power On Configuration Set Up Table (for 5 port mode)</b>			
<b>Name</b>	<b>Pin Number</b>	<b>I/O</b>	<b>Descriptions</b>
NC_11	11	I/O	Port0 MII interface enable : ( power on external jumper configuration ) - pin floating : Port0 MII interface disable (Port0 : be configured in RMII interface) - external pull_high: Port0 MII interface enable. (suitable for 5 port dual speed hub application).
TXEN0	18	I/O	Back_pressure disable : ( power on external jumper configuration ) - external pull_low (default ) : normal mode (back_pressure enable) - external pull_high: back_pressure disable



<b>Power On Configuration Set Up Table (for 5 port mode)</b>			
<b>Name</b>	<b>Pin Number</b>	<b>I/O</b>	<b>Descriptions</b>
TXEN2	42	I/O	Auto MII_setting bypass : ( power on external jumper configuration ) - external pull_low (default ) : normal mode ( auto MII_setting); after power_on, MTD658E will auto setup PHY devices be forced in half_duplex mode for repeater application. - external pull_high: auto MII_setting bypass.
PART4	99	I/O	PHY_ID 5h0b starting enable :(power on external jumper configuration) - external pull_low (default ) : MII setting PHY_ID start address from 5h07 to 5h0b. - external pull_high: MII setting PHY_ID start address from 5h0b to 5h0f.
MDC	126	I/O	1522 bytes packet accept enable : ( power on external jumper configuration ) - external pull_low (default ) : normal mode ( <=1518 bytes packet accept) - external pull_high: <= 1522 bytes packet accept
LEDDAT	124	I/O	External arbiter enable : ( power on external jumper configuration ) - external pull_low (default ) : normal mode (inter_repeater bus use internal arbiter) - external pull_high: inter_repeater bus use external arbiter .



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## 5.0 FUNCTIONAL DESCRIPTIONS

The MTD658E is conformed to IEEE802.3 chapter 9 and IEEE802.3u clause 27 specifications. The MTD658E provides 8 Reduced MII interfaces and an embedded two port switch (built in 64k8 ASRAM on chip) to construct a 10M/100M dual speed Hub application. And also, MTD658E can be configured to 5 port mode, it will provide 4 RMII and 1 MII interface. Two Inter-Bus are also provided for stackable 10M/100M dual speed Hub application. Since MTD658E built in memory on chip, there are no need any extra memories in the application board. The MTD658E functions are described as follows:

### 5.1 Repeation and data handling

8 independent RMII ports integrated with IEEE802.3 chapter 9 and IEEE802.3u clause 27 repeater functions simultaneously. MTD658E embedded two Hub cores (10M and 100M), and each dedicated RMII interface port can get per port's speed information from per port speed input pin, and then MTD658E will switch individual port to their appropriated Hub core functions (10M or 100M). The MTD658E receive packets from each RMII ports, and redirect port's input packet to 10M or 100M Hub core according each port's speed. The internal IEEE802.3 chapter 9 or IEEE802.3u clause 27 repeater main state machine will starts to repeat the input packet to all ports except the input port. If larger than or equal to two ports have input packet simultaneously, this will be treated as a collision, and MTD658E will assert an arbitrary JAM pattern to all ports' output until collision event disappear and network is idle.

### 5.2 Partition

The MTD658E provides 10M/100M auto partition/reconnection functions to guarantee the network segment performance by means of detecting a consecutive collisions. Each dedicated RMII port has implement a individual 10M/100M auto partition/reconnection state machine. If port's consecutive collision number over or equal to CClimit (10M CClimit default is 32, 100M CClimit default is 64), this port will be partitioned. Reconnection will occurs after a larger than 512 bit time packet was received or transmitted from this partitioned port without any collision.

When port is under partition state, MTD658E will not accept any input messages from this port (just monitor input message), but will continue output repeated messages to this partition port.

Some new partition criterions are also implement, such as long\_collision\_partition event, jabber\_partition event. In 10M/100M partition state machine, longer than 1024 bit time continuous collision will force port enter partition state. In 100M partition state machine, if port enter jabber\_on state, this port will be partitioned. In 10M, jabber\_partition function is not implemented.

### 5.3 Jabber

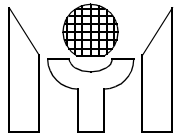
The jabber protect function is used to prevent an illegally long packet reception. After the MTD658E received a longer than 65536 +/- 6.25% bit times packet, this receive port's receive/transmit path will be inhibited until carrier is no longer detected.

### 5.4 MII Setting

Due to HUB is an half duplex device, the MTD658E need to force all connected physical devices to work in half duplex environment. The MTD658E will setting all PHY's SMI register 4's half/full duplex bit during power on, and than restart auto-negotiation procedure to work in half duplex mode. In 8 port mode, the PHY's device ID should be setted from 5h04 - 5h0b (port0-7) or from 5h08 -5h0f (port0-7); In 5 port mode, the PHY device ID should be setted from 5h07 - 5h0b (port0-4) or from 5h0b -5h0f (port0-4).

### 5.5 Inter-Bus Interface

Two Inter-Bus Interface are provided by the MTD658E, One is 10M Inter-Bus Interface, the other is 100M Inter-Bus Interface. The Inter-Bus interface is designed for stackable hub application. For each domain, up to 4 MTD658Es can be stacked through this Inter-Bus without any external arbitration logic. The Inter-Bus Interface includes IMASTER, IDATA (100M: use IDAT<3:0>, 10M: use only IDAT), REQOUT, REQIN0-2, ICLK, IACKB, ICOLB pins. IMASTER decide which MTD658E can arbitrate the Inter-Bus, and only one MTD658E's IMASTER can be tie high in a stackable Hub. IDATA are synchro-



nous with ICLK. The MTD658E output REQOUT to inform Inter-Bus Interface that it need the Inter-Bus right. When IACKB is asserted by Inter-Bus master after REQOUT asserted, the MTD658E which asserted REQOUT will get the bus right and put the transmit data into IDATA. If the MTD658E did not assert REQOUT , but IACKB is asserted, means this MTD658E can get data from IDATA bus. When only one MTD658E output REQOUT to Inter-Bus Interface, IACKB will be asserted by Inter-Bus master device, If larger than two MTD658E's REQOUT were asserted, Inter-Bus master will not assert IACKB , but will assert ICOLB to inform all the connected MTD658Es.

The Inter-Bus interface can also be programmed to EXT\_ARB mode, using LEDDAT pin's jumper setting. In this mode, Inter-Bus interface need an external arbitration logic to arbitrate Inter-Bus operation. And in this mode, the stackable capability is not limited by the MTD658E's REQIN pins number.

**5.6 10M/100M packet Switch**

The MTD658E implements a 10/100M two port switch for 10M/100M packet switching. Total 2K address entrys are provided for packets' SA learning and DA routing; and also provide automatic aging function ( aging time = 300secs). The input packet from 10M Hub ( or 100M Hub) will be stored to external memory first, while packet is good for forward ( CRC check ok, length = 64Bytes ~ 1518Bytes or 1522 Bytes, and not local packets ) , than forward this packet to 100M Hub (or 10M Hub).

**5.7 Uplink Switch Port**

The MTD658E can config one switch port as an uplink switch port. When UPSWEN pin is high, and IMASTER pin is low, one of the intenal switch port is connect to 100M Hub, the other is connected to RMII the highest port . In uplink switch mode, the highest port can operate in 10M/100M (in 8 port mode : from SPD7 pin; in 5 port mode: from SPD4 pin ), and operate in half/full duplex (in 8 port mode: from FD7 pin; in 5 port mode: from FD4 pin).

**5.8 Memory Interface**

The MTD658E build-in an asynchronous SRAM as two port switches' packet buffers, total has 64K byte embedded memory for packet buffering.

**5.9 MII management**

The MTD658E can be managed through MDC, MDIO pins. The MTD658E implements 3 MII registers for function control and status report (see Section 4.0 on page ).

The management frame format is compliant to IEEE802.3u clause 22, and the device ID is fixed to 5'h1f internally.

**5.10 LED display**

The MTD658E implements three display modes, port RX activity, 10/100M domain collision, port partition. The LED data pin LEDDAT is high activated.

One strobe pin LEDCLK(24 burst clock/per 42ms) is used to latch serial LEDDAT information, and user can shift the latched data into byte aligned shift register to drive LEDs.

The MTD658E also provide status pins to direct output per port's receive activity/partition, 100M Hub collision, 10M Hub collision, embedded ASRM memory test fail status.

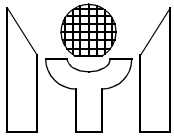
**6.0 Registers**

The MTD658E implements 3 MII registers, define as following tables:

**TABLE 1. MII registers**

REG NO	Bits	Name	R/W	Descriptions	Default
0		CtlReg0	R/W	<b>CONTROL REGISTER 0</b>	
	0			Reserved.	1b0
	1	DisPar10		Set this bit will disable 10M hub core partition function.	1b0

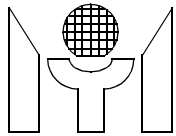




**TABLE 1. MII registers**

<b>REG NO</b>	<b>Bits</b>	<b>Name</b>	<b>R/W</b>	<b>Descriptions</b>	<b>Default</b>
	2	DisPar100		Set this bit will disable 100M hub core partition function.	1b0
	3	DisJab10		Set this bit will disable 10M hub core Jabber function.	1b0
	4	DisJab100		Set this bit will disable 100M hub core Jabber function.	1b0
	5-8			Reserved	4b000
	9	CClimit100		Set high will program 100M partition cclimit to 128.	1b0(64)
	10	CClimit10		Set high will program 10M partition cclimit to 64.	1b0(32)
	11-15			Reserved	2b00
<b>1</b>		<b>CtlReg1</b>	<b>R/W</b>	<b>CONTROL REGISTER 1</b>	<b>16h0000</b>
	0-7	DisPort		Set bits high disable port 0-7 RMII ports.	8h000
	8-15			Reserved.	
<b>2</b>				<b>Reserved</b>	
<b>3</b>				<b>Reserved</b>	
<b>4</b>		<b>AgeReg</b>	<b>R/W</b>	<b>AGE REGISTER</b>	<b>16h12c</b>
	0-15	AgeTime		Change this register's content will change Aging Time value(Unit:Sec)	

"R/W" means read/writable.



## 7.0 Electrical Characteristics

### 7.1 Absolute Maximum Ratings

Symbol	Parameter	RATING	Unit
V <sub>CC</sub>	Power Supply Voltage	-0.3 to 3.6	V
V <sub>IN</sub>	Input Voltage	-0.3 to V <sub>CC</sub> +0.3	V
V <sub>OUT</sub>	Output Voltage	-0.3 to V <sub>CC</sub> +0.3	V
T <sub>STG</sub>	Storage Temperature	-55 to 150	°C

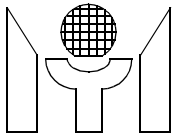
### 7.2 Recommended Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
V <sub>CC</sub>	Commercial Power Supply Voltage	3.0	3.3	3.6	V
V <sub>IN</sub>	Input Voltage	0	-	V <sub>CC</sub>	V
T <sub>OPR</sub>	Commercial Junction Operating Temperature	0	25	115	°C
	Industrial Junction Operating Temperature	-40	25	125	°C

### 7.3 DC Electrical Characteristics

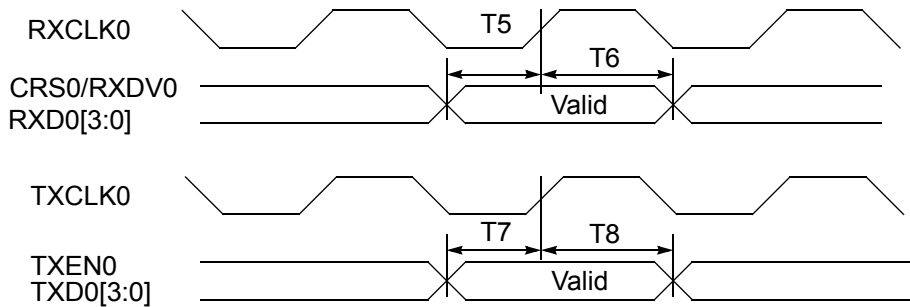
Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I <sub>IL</sub>	Input Leakage Current	no pull-up or down	-1		1	uA
I <sub>OZ</sub>	Tri-state Leakage Current		-10		10	uA
C <sub>IN</sub>	Input Capacitance			2.8		pF
C <sub>OUT</sub>	Output Capacitance		2.7		4.9	pF
C <sub>BID3</sub>	Bi-direction buffer Capacitance		2.7		4.9	pF
V <sub>IL</sub>	Input Low Voltage	CMOS			0.3*V <sub>CC</sub>	V
V <sub>IH</sub>	Input High Voltage	CMOS	0.7*V <sub>CC</sub>			V
V <sub>OH</sub>	Output High Voltage	I <sub>OL</sub> =2,4,8,12,16,24mA	2.4			V
V <sub>OL</sub>	Output Low Voltage	I <sub>OH</sub> =2,4,8,12,16,24mA			0.4	V
R <sub>I</sub>	Input Pull-up/down resistance	V <sub>IL</sub> =0V or V <sub>IH</sub> =V <sub>CC</sub>		75		KOhm

(Under recommended operating conditions and V<sub>CC</sub> = 3.0 ~ 3.6V, T<sub>J</sub> = 0 to +115 °C)



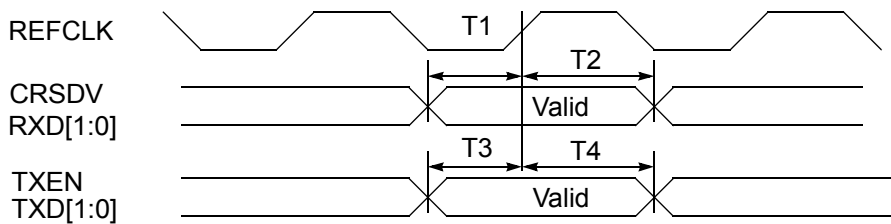
**7.4 Electrical Characteristics**

**FIGURE 1. MII timing**

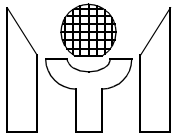


Symbol	Parameter	Min.	Typ.	Max.	Unit	Note
T5	MII input setup time	10			nS	
T6	MII input hold time	10			nS	
T7	MII output setup time	3			nS	
T8	MII output hold time	5			nS	

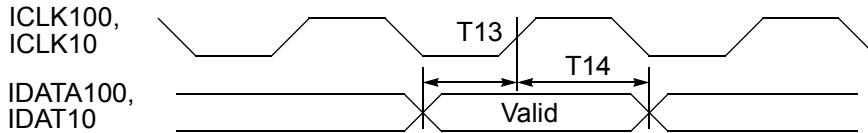
**FIGURE 2. RMII timing**



Symbol	Parameter	Min.	Typ.	Max.	Unit	Note
T1	RMII input setup time	1			nS	
T2	RMII input hold time	1			nS	
T3	RMII output setup time	3			nS	
T4	RMII output hold time	5			nS	

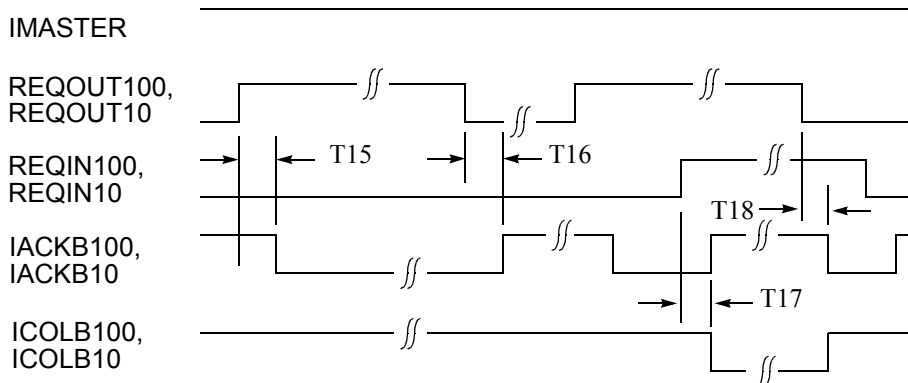


**FIGURE 3. Inter-Bus Interface timing I**



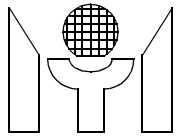
Symbol	Parameter	Min.	Typ.	Max.	Unit	Note
T13	Inter-Bus output setup time(100M)	15		20	nS	
	Inter-Bus output setup time(10M)		50		nS	
T14	Inter-Bus output hold time(100M)	20		25	nS	
	Inter-Bus output hold time(10M)		50		nS	

**FIGURE 4. Inter-Bus Interface timing II**

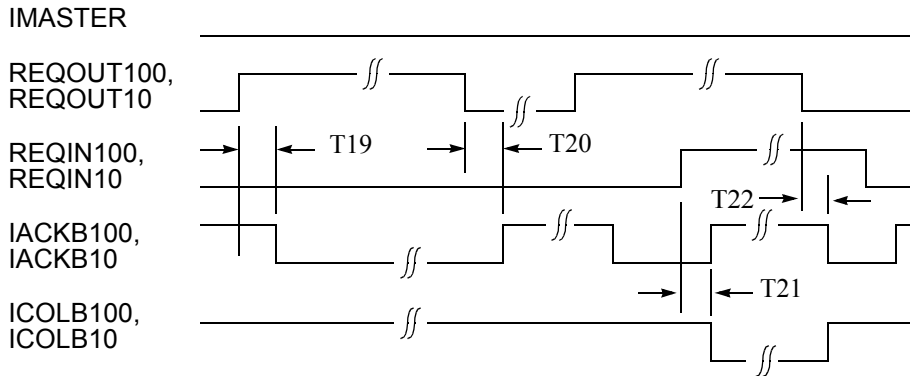


Symbol	Parameter	Min.	Typ.	Max.	Unit	Note
T15	Inter-Bus master REQOUT asserted to IACKB asserted propagation delay	7		20	nS	1
T16	Inter-Bus master REQOUT deasserted to IACKB deasserted propagation delay	0	1	5	nS	1
T17	Inter-Bus master REQIN asserted to IACKB deasserted(ICOLB asserted) propagation delay(SOJ)	5		17	nS	1
T18	Inter-Bus master REQOUT deasserted to IACKB asserted(ICOLB deasserted) propagation delay(EOJ)	0	1	5	nS	1

Note 1 : In 10M/100M Inter-Bus interface, T15-T18 have the same value.



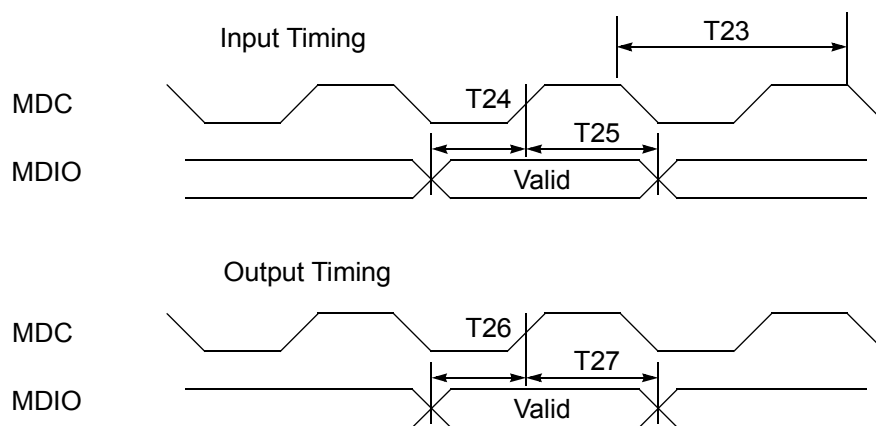
**FIGURE 5. Inter-Bus Interface timing III**



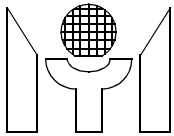
Symbol	Parameter	Min.	Typ.	Max.	Unit	Note
T19	Inter-Bus slave REQOUT asserted to IACKB asserted propogation delay	5		20	nS	2
T20	Inter-Bus slave REQOUT deasserted to IACKB deasserted propogation delay	5		20	nS	2
T21	Inter-Bus slave REQIN asserted to IACKB deasserted(ICOLB asserted) propogation delay(SOJ)	5		20	nS	2
T22	Inter-Bus slave REQOUT deasserted to IACKB asserted(ICOLBdeasserted) propogation delay(EOJ)	5		20	nS	2

Note 2 : In 10M/100M Inter-Bus interface, T19-T22 have the same value.

**FIGURE 6. MII Management timing**

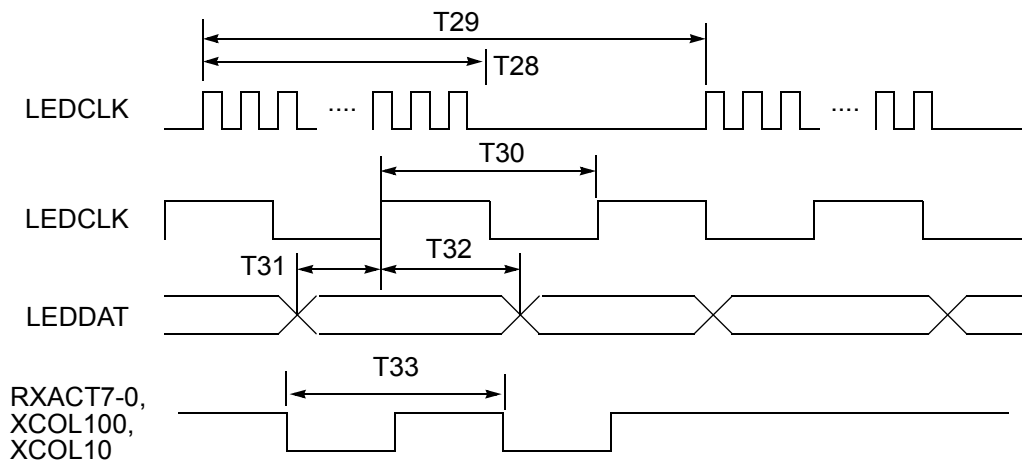


Symbol	Parameter	Min.	Typ.	Max.	Unit	Note
T23	MDC clock cycle		400		nS	
T23	MDIO input setup time	10			nS	

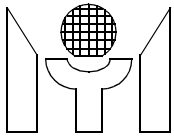


Symbol	Parameter	Min.	Typ.	Max.	Unit	Note
T25	MDIO input hold time	10			nS	
T26	MDIO output setup time	182		194	nS	
T27	MDIO output hold time	206		218	nS	

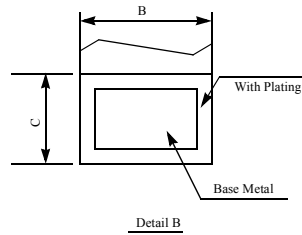
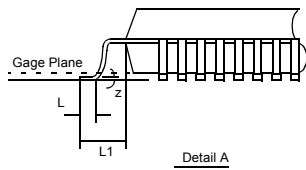
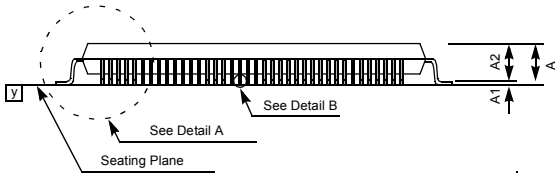
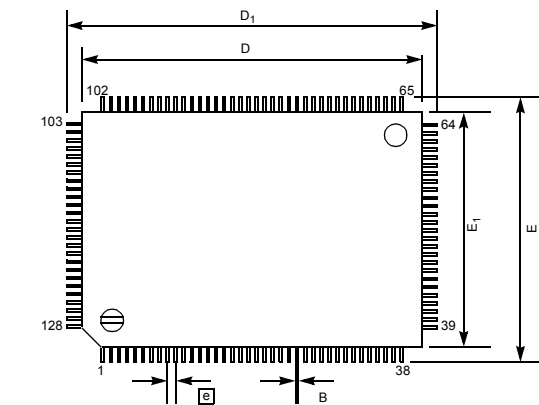
**FIGURE 7. LED output timing**



Symbol	Parameter	Min.	Typ.	Max.	Unit	Note
T28	24 LED burst clocks duration		3.84		uS	
T29	LED burst clock cycle time		42		mS	
T30	LED burst clock cycle		160		nS	
T31	LEDDAT to LEDCLK setup time		80		nS	
T32	LEDDAT to LEDCLK setup time		80		nS	
T33	LED Output flash rate		42		mS	



**8.0 128 pin PQFP Package Data**



Symbol	Dimension in inch			Dimension in mm		
	Min	Norm	Max	Min	Norm	Max
A	-	-	0.134	-	-	3.40
A1	0.010	-	-	0.25	-	-
A2	0.107	0.112	0.117	2.73	2.85	2.97
B	0.007	0.009	0.011	0.17	0.22	0.27
C	0.004	-	0.008	0.09	-	0.20
D	0.906	0.913	0.921	23.00	23.20	23.40
D1	0.783	0.787	0.791	19.90	20.00	20.10
E	0.669	0.677	0.685	17.00	17.20	17.40
E1	0.547	0.551	0.555	13.90	14.00	14.10
$\square$	0.020 BSC			0.50 BSC		
L	0.029	0.035	0.041	0.73	0.88	1.03
L1	0.063 BSC			1.60 BSC		
y	-	-	0.004	-	-	0.10
z	0°	-	7°	0°	-	7°

Note:  
 1.Dimension D1 & E1 do not include mold protrusion.  
 But mold mismatch is included. Allowable protrusion is .25mm/.010" per side.  
 2.Dimension B does not include dambar protrusion. Allowable dambar protrusion .08mm/.003". Total in excess of the B dimension at maximum material condition. Dambar cannot be located on the lower radius or the foot.  
 3.Controlling dimension : Millimeter.