

# Designer's™ Data Sheet

## HDTMOS E-FET™

### High Density Power FET

#### N-Channel Enhancement-Mode Silicon Gate

This advanced high-cell density HDTMOS E-FET is designed to withstand high energy in the avalanche and commutation modes. This new energy efficient design also offers a drain-to-source diode with a fast recovery time. Designed for low-voltage, high-speed switching applications in power supplies, converters and PWM motor controls, and inductive loads. The avalanche energy capability is specified to eliminate the guesswork in designs where inductive loads are switched, and to offer additional safety margin against unexpected voltage transients.

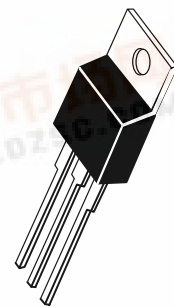
- Ultra Low  $R_{DS(on)}$ , High-Cell Density, HDTMOS
- Diode is Characterized for Use in Bridge Circuits
- $I_{DSS}$  and  $V_{DS(on)}$  Specified at Elevated Temperature
- Avalanche Energy Specified



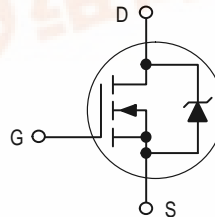
**MTP75N06HD**

Motorola Preferred Device

TMOS POWER FET  
75 AMPERES  
 $R_{DS(on)} = 10.0 \text{ m}\Omega$   
60 VOLTS



CASE 221A-06, Style 5  
TO-220AB



#### MAXIMUM RATINGS ( $T_C = 25^\circ\text{C}$ unless otherwise noted)

Rating	Symbol	Value	Unit
Drain-Source Voltage	$V_{DS}$	60	Vdc
Drain-Gate Voltage ( $R_{GS} = 1.0 \text{ M}\Omega$ )	$V_{DGR}$	60	Vdc
Gate-Source Voltage — Continuous — Single Pulse	$V_{GS}$	$\pm 20$ $\pm 30$	Vdc Vpk
Drain Current — Continuous — Continuous @ $100^\circ\text{C}$ — Single Pulse ( $t_p \leq 10 \mu\text{s}$ )	$I_D$ $I_D$ $I_{DM}$	75 50 225	Adc Adc Apk
Total Power Dissipation Derate above $25^\circ\text{C}$	$P_D$	150 1.0	Watts W/ $^\circ\text{C}$
Operating and Storage Temperature Range	$T_J, T_{stg}$	-55 to 175	$^\circ\text{C}$
Single Pulse Drain-to-Source Avalanche Energy — Starting $T_J = 25^\circ\text{C}$ ( $V_{DD} = 25 \text{ Vdc}$ , $V_{GS} = 10 \text{ Vdc}$ , $I_L = 75 \text{ Apk}$ , $L = 0.177 \text{ mH}$ , $R_G = 25 \Omega$ )	EAS	500	mJ
Thermal Resistance — Junction to Case — Junction to Ambient	$R_{\theta JC}$ $R_{\theta JA}$	1.0 62.5	$^\circ\text{C/W}$
Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 10 seconds	$T_L$	260	$^\circ\text{C}$

**Designer's Data for "Worst Case" Conditions** — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

E-FET, Designer's and HDTMOS are trademarks of Motorola, Inc.  
TMOS is a registered trademark of Motorola, Inc.

Preferred devices are Motorola recommended choices for future use and best overall value.

# MTP75N06HD

## ELECTRICAL CHARACTERISTICS (T<sub>J</sub> = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
<b>OFF CHARACTERISTICS</b>					
Drain–Source Breakdown Voltage (V <sub>GS</sub> = 0 Vdc, I <sub>D</sub> = 250 μAdc) Temperature Coefficient (Positive)	V(BR)DSS	60	68 60.4	—	Vdc mV/°C
Zero Gate Voltage Drain Current (V <sub>DS</sub> = 60 Vdc, V <sub>GS</sub> = 0 Vdc) (V <sub>DS</sub> = 60 Vdc, V <sub>GS</sub> = 0 Vdc, T <sub>J</sub> = 125°C)	I <sub>DSS</sub>	—	—	10 100	μAdc
Gate–Body Leakage Current (V <sub>GS</sub> = ± 20 Vdc, V <sub>DS</sub> = 0 V)	I <sub>GSS</sub>	—	5.0	100	nAdc

### ON CHARACTERISTICS (1)

Gate Threshold Voltage (V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μAdc) Temperature Coefficient (Negative)	V <sub>GS(th)</sub>	2.0	3.0 8.38	4.0	Vdc mV/°C
Static Drain–Source On–Resistance (V <sub>GS</sub> = 10 Vdc, I <sub>D</sub> = 37.5 Adc)	R <sub>DS(on)</sub>	—	8.3	10	mΩ
Drain–Source On–Voltage (V <sub>GS</sub> = 10 Vdc) (I <sub>D</sub> = 75 Adc) (I <sub>D</sub> = 37.5 Adc, T <sub>J</sub> = 125°C)	V <sub>DS(on)</sub>	—	0.7 0.53	0.9 0.8	Vdc
Forward Transconductance (V <sub>DS</sub> = 15 Vdc, I <sub>D</sub> = 37.5 Adc)	g <sub>FS</sub>	15	32	—	mhos

### DYNAMIC CHARACTERISTICS

Input Capacitance	(V <sub>DS</sub> = 25 Vdc, V <sub>GS</sub> = 0 Vdc, f = 1.0 MHz)	C <sub>iss</sub>	—	2800	3920	pF
Output Capacitance		C <sub>oss</sub>	—	928	1300	
Reverse Transfer Capacitance		C <sub>rss</sub>	—	180	252	

### SWITCHING CHARACTERISTICS (2)

Turn–On Delay Time	(V <sub>DS</sub> = 30 Vdc, I <sub>D</sub> = 75 Adc, V <sub>GS</sub> = 10 Vdc, R <sub>G</sub> = 9.1 Ω)	t <sub>d(on)</sub>	—	18	26	ns
Rise Time		t <sub>r</sub>	—	218	306	
Turn–Off Delay Time		t <sub>d(off)</sub>	—	67	94	
Fall Time		t <sub>f</sub>	—	125	175	
Gate Charge	(V <sub>DS</sub> = 48 Vdc, I <sub>D</sub> = 75 Adc, V <sub>GS</sub> = 10 Vdc)	Q <sub>T</sub>	—	71	100	nC
		Q <sub>1</sub>	—	16.3	—	
		Q <sub>2</sub>	—	31	—	
		Q <sub>3</sub>	—	29.4	—	

### SOURCE–DRAIN DIODE CHARACTERISTICS

Forward On–Voltage	(I <sub>S</sub> = 75 Adc, V <sub>GS</sub> = 0 Vdc) (I <sub>S</sub> = 75 Adc, V <sub>GS</sub> = 0 Vdc, T <sub>J</sub> = 125°C)	V <sub>SD</sub>	—	0.97 0.88	1.1	Vdc
Reverse Recovery Time	(I <sub>S</sub> = 75 Adc, V <sub>GS</sub> = 0 Vdc, dI <sub>S</sub> /dt = 100 A/μs)	t <sub>rr</sub>	—	56	—	ns
		t <sub>a</sub>	—	44	—	
		t <sub>b</sub>	—	12	—	
Reverse Recovery Stored Charge		Q <sub>RR</sub>	—	0.103	—	μC

### INTERNAL PACKAGE INDUCTANCE

Internal Drain Inductance (Measured from contact screw on tab to center of die) (Measured from the drain lead 0.25" from package to center of die)	L <sub>D</sub>	—	3.5	—	nH
Internal Source Inductance (Measured from the source lead 0.25" from package to source bond pad)	L <sub>S</sub>	—	7.5	—	nH

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

(2) Switching characteristics are independent of operating junction temperature.

(3) Reflects typical values.  $C_{pk} = \left| \frac{\text{Max limit} - \text{Typ}}{3 \times \text{SIGMA}} \right|$

TYPICAL ELECTRICAL CHARACTERISTICS

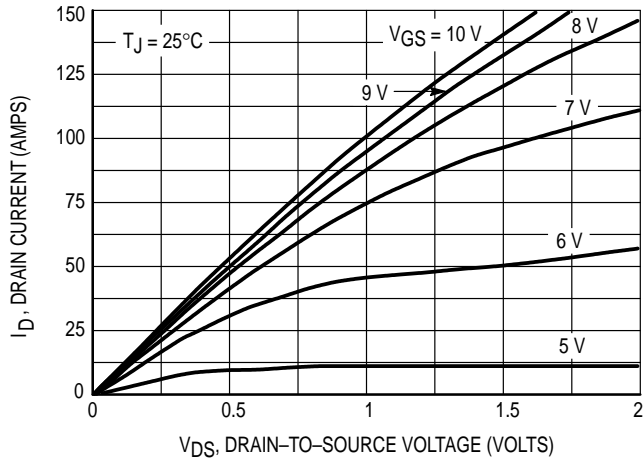


Figure 1. On-Region Characteristics

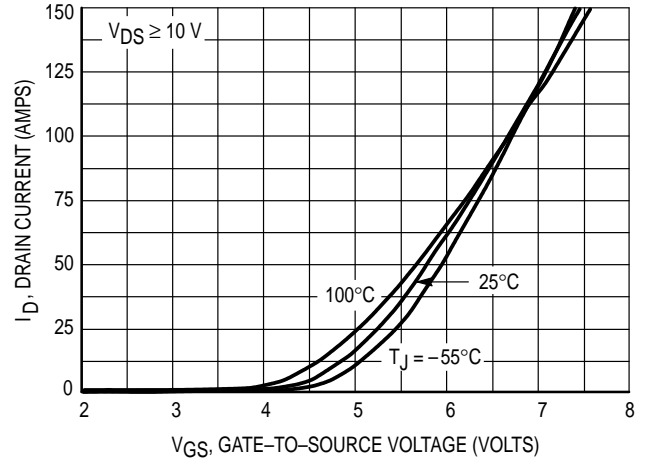


Figure 2. Transfer Characteristics

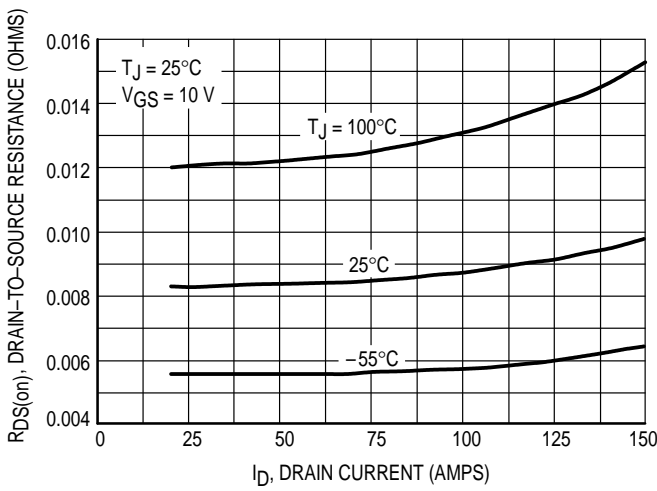


Figure 3. On-Resistance versus Drain Current and Temperature

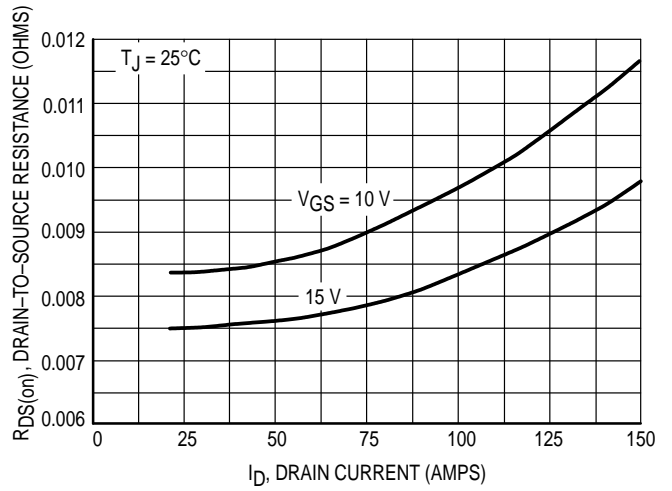


Figure 4. On-Resistance versus Drain Current and Gate Voltage

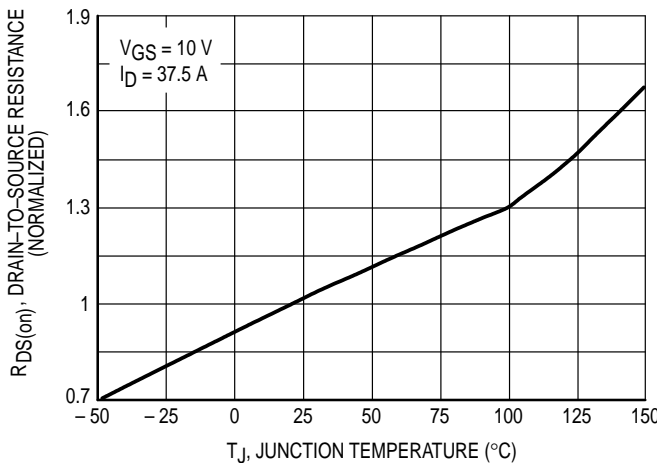


Figure 5. On-Resistance Variation with Temperature

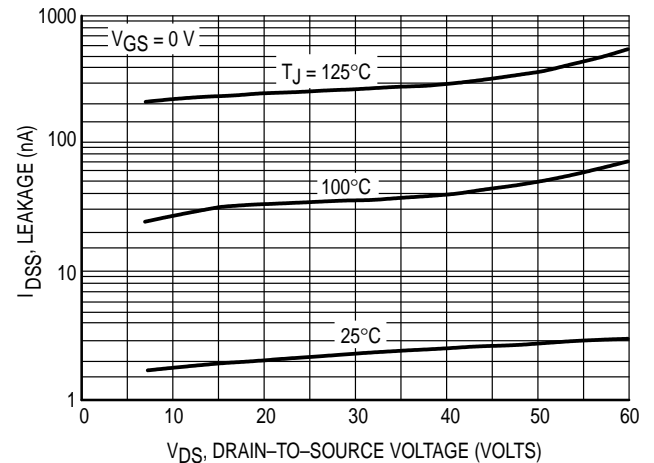


Figure 6. Drain-To-Source Leakage Current versus Voltage

## MTP75N06HD

### POWER MOSFET SWITCHING

Switching behavior is most easily modeled and predicted by recognizing that the power MOSFET is charge controlled. The lengths of various switching intervals ( $\Delta t$ ) are determined by how fast the FET input capacitance can be charged by current from the generator.

The published capacitance data is difficult to use for calculating rise and fall because drain–gate capacitance varies greatly with applied voltage. Accordingly, gate charge data is used. In most cases, a satisfactory estimate of average input current ( $I_{G(AV)}$ ) can be made from a rudimentary analysis of the drive circuit so that

$$t = Q/I_{G(AV)}$$

During the rise and fall time interval when switching a resistive load,  $V_{GS}$  remains virtually constant at a level known as the plateau voltage,  $V_{GSP}$ . Therefore, rise and fall times may be approximated by the following:

$$t_r = Q_2 \times R_G / (V_{GG} - V_{GSP})$$

$$t_f = Q_2 \times R_G / V_{GSP}$$

where

$V_{GG}$  = the gate drive voltage, which varies from zero to  $V_{GG}$

$R_G$  = the gate drive resistance

and  $Q_2$  and  $V_{GSP}$  are read from the gate charge curve.

During the turn–on and turn–off delay times, gate current is not constant. The simplest calculation uses appropriate values from the capacitance curves in a standard equation for voltage change in an RC network. The equations are:

$$t_{d(on)} = R_G C_{iss} \ln [V_{GG} / (V_{GG} - V_{GSP})]$$

$$t_{d(off)} = R_G C_{iss} \ln (V_{GG} / V_{GSP})$$

The capacitance ( $C_{iss}$ ) is read from the capacitance curve at a voltage corresponding to the off–state condition when calculating  $t_{d(on)}$  and is read at a voltage corresponding to the on–state when calculating  $t_{d(off)}$ .

At high switching speeds, parasitic circuit elements complicate the analysis. The inductance of the MOSFET source lead, inside the package and in the circuit wiring which is common to both the drain and gate current paths, produces a voltage at the source which reduces the gate drive current. The voltage is determined by  $L di/dt$ , but since  $di/dt$  is a function of drain current, the mathematical solution is complex. The MOSFET output capacitance also complicates the mathematics. And finally, MOSFETs have finite internal gate resistance which effectively adds to the resistance of the driving source, but the internal resistance is difficult to measure and, consequently, is not specified.

The resistive switching time variation versus gate resistance (Figure 9) shows how typical switching performance is affected by the parasitic circuit elements. If the parasitics were not present, the slope of the curves would maintain a value of unity regardless of the switching speed. The circuit used to obtain the data is constructed to minimize common inductance in the drain and gate circuit loops and is believed readily achievable with board mounted components. Most power electronic loads are inductive; the data in the figure is taken with a resistive load, which approximates an optimally snubbed inductive load. Power MOSFETs may be safely operated into an inductive load; however, snubbing reduces switching losses.

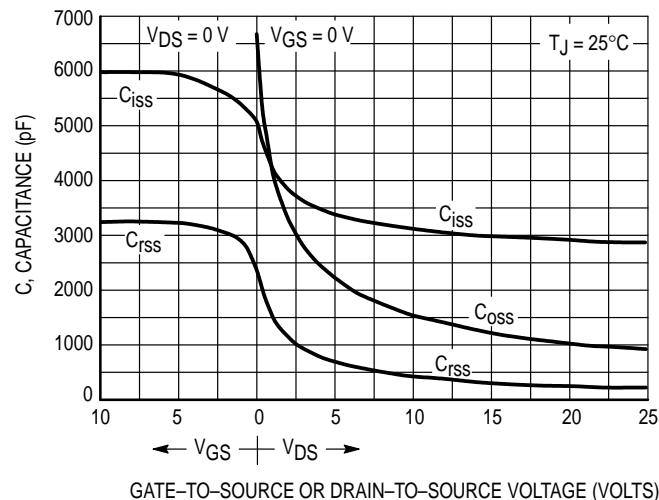


Figure 7. Capacitance Variation

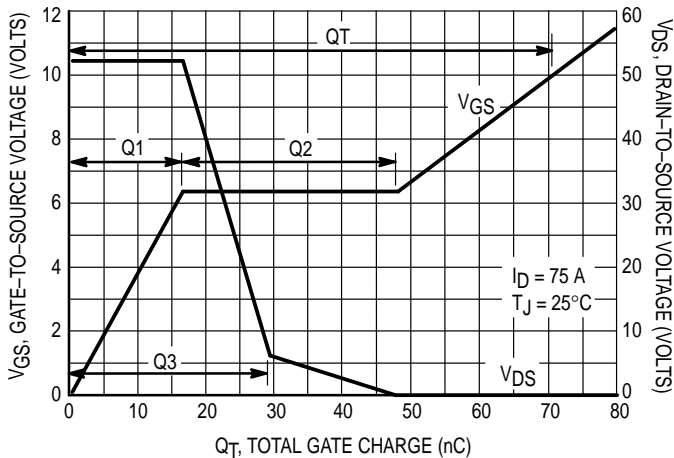


Figure 8. Gate-To-Source and Drain-To-Source Voltage versus Total Charge

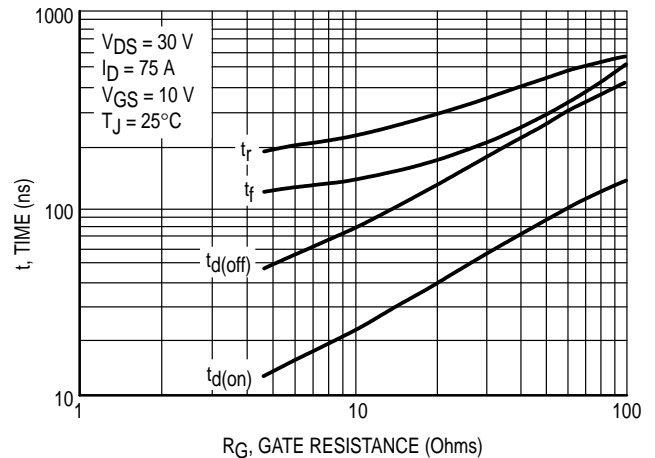


Figure 9. Resistive Switching Time Variation versus Gate Resistance

**DRAIN-TO-SOURCE DIODE CHARACTERISTICS**

The switching characteristics of a MOSFET body diode are very important in systems using it as a freewheeling or commutating diode. Of particular interest are the reverse recovery characteristics which play a major role in determining switching losses, radiated noise, EMI and RFI.

System switching losses are largely due to the nature of the body diode itself. The body diode is a minority carrier device, therefore it has a finite reverse recovery time,  $t_{rr}$ , due to the storage of minority carrier charge,  $Q_{RR}$ , as shown in the typical reverse recovery wave form of Figure 12. It is this stored charge that, when cleared from the diode, passes through a potential and defines an energy loss. Obviously, repeatedly forcing the diode through reverse recovery further increases switching losses. Therefore, one would like a diode with short  $t_{rr}$  and low  $Q_{RR}$  specifications to minimize these losses.

The abruptness of diode reverse recovery effects the amount of radiated noise, voltage spikes, and current ringing. The mechanisms at work are finite irremovable circuit parasitic inductances and capacitances acted upon by high

$di/dts$ . The diode's negative  $di/dt$  during  $t_a$  is directly controlled by the device clearing the stored charge. However, the positive  $di/dt$  during  $t_b$  is an uncontrollable diode characteristic and is usually the culprit that induces current ringing. Therefore, when comparing diodes, the ratio of  $t_b/t_a$  serves as a good indicator of recovery abruptness and thus gives a comparative estimate of probable noise generated. A ratio of 1 is considered ideal and values less than 0.5 are considered snappy.

Compared to Motorola standard cell density low voltage MOSFETs, high cell density MOSFET diodes are faster (shorter  $t_{rr}$ ), have less stored charge and a softer reverse recovery characteristic. The softness advantage of the high cell density diode means they can be forced through reverse recovery at a higher  $di/dt$  than a standard cell MOSFET diode without increasing the current ringing or the noise generated. In addition, power dissipation incurred from switching the diode will be less due to the shorter recovery time and lower switching losses.

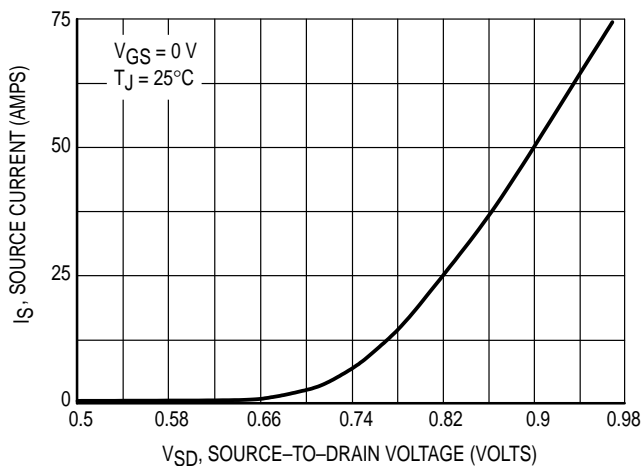


Figure 10. Diode Forward Voltage versus Current

# MTP75N06HD

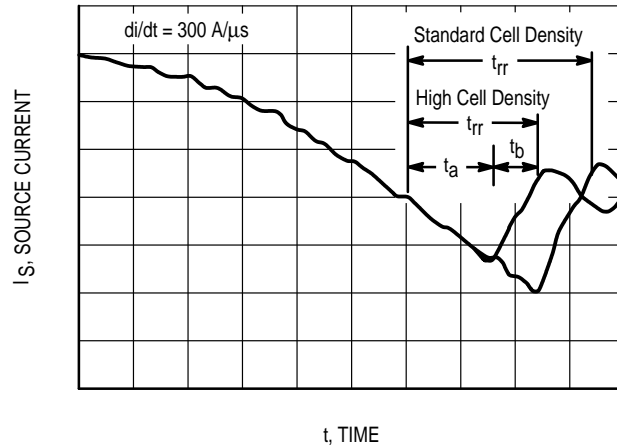


Figure 11. Reverse Recovery Time ( $t_{rr}$ )

## SAFE OPERATING AREA

The Forward Biased Safe Operating Area curves define the maximum simultaneous drain-to-source voltage and drain current that a transistor can handle safely when it is forward biased. Curves are based upon maximum peak junction temperature and a case temperature ( $T_C$ ) of  $25^\circ\text{C}$ . Peak repetitive pulsed power limits are determined by using the thermal response data in conjunction with the procedures discussed in AN569, "Transient Thermal Resistance – General Data and Its Use."

Switching between the off-state and the on-state may traverse any load line provided neither rated peak current ( $I_{DM}$ ) nor rated voltage ( $V_{DSS}$ ) is exceeded, and that the transition time ( $t_r$ ,  $t_f$ ) does not exceed  $10 \mu\text{s}$ . In addition the total power averaged over a complete switching cycle must not exceed  $(T_{J(\text{MAX})} - T_C)/(R_{\theta J C})$ .

A power MOSFET designated E-FET can be safely used in switching circuits with unclamped inductive loads. For reli-

able operation, the stored energy from circuit inductance dissipated in the transistor while in avalanche must be less than the rated limit and must be adjusted for operating conditions differing from those specified. Although industry practice is to rate in terms of energy, avalanche energy capability is not a constant. The energy rating decreases non-linearly with an increase of peak current in avalanche and peak junction temperature.

Although many E-FETs can withstand the stress of drain-to-source avalanche at currents up to rated pulsed current ( $I_{DM}$ ), the energy rating is specified at rated continuous current ( $I_D$ ), in accordance with industry custom. The energy rating must be derated for temperature as shown in the accompanying graph (Figure 13). Maximum energy at currents below rated continuous  $I_D$  can safely be assumed to equal the values indicated.

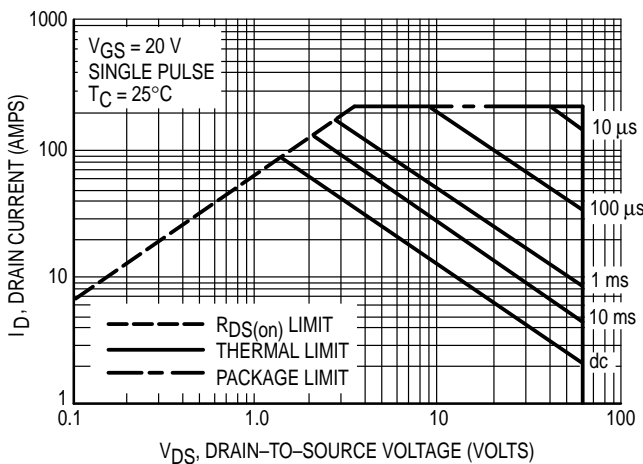


Figure 12. Maximum Rated Forward Biased Safe Operating Area

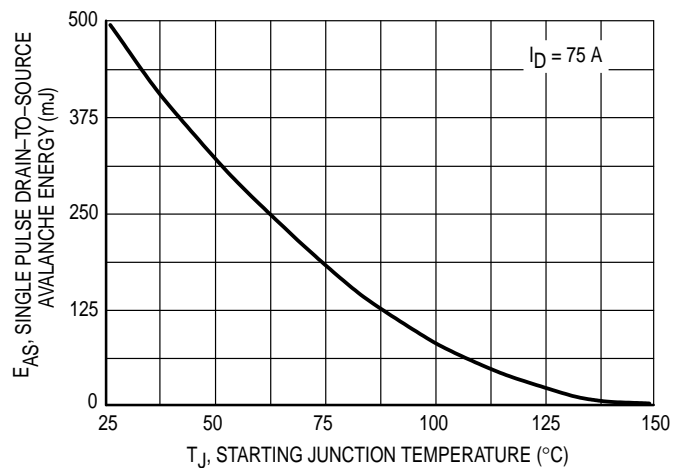


Figure 13. Maximum Avalanche Energy versus Starting Junction Temperature

TYPICAL ELECTRICAL CHARACTERISTICS

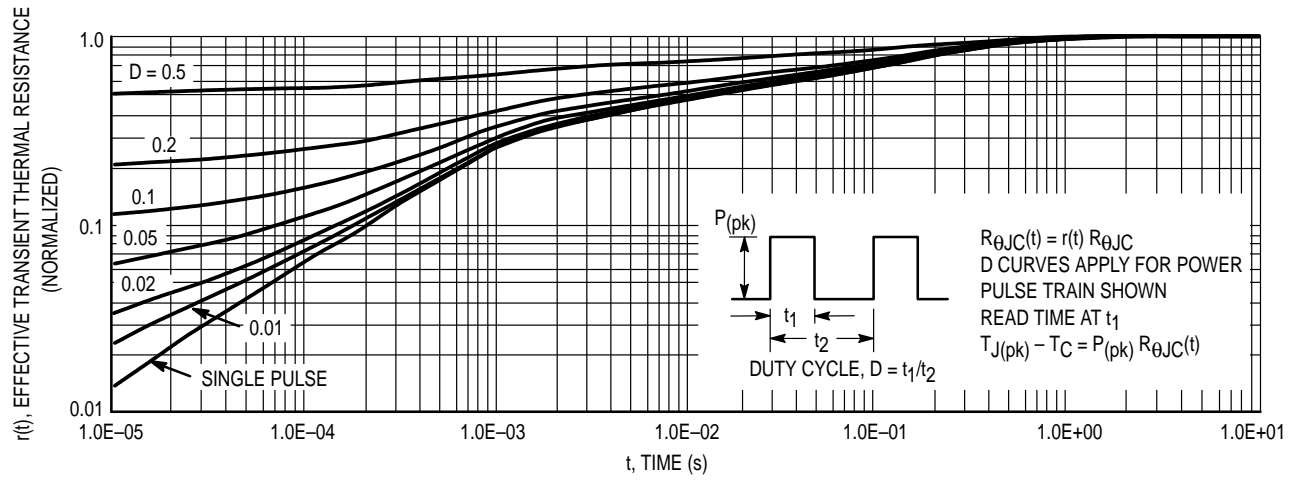


Figure 14. Thermal Response

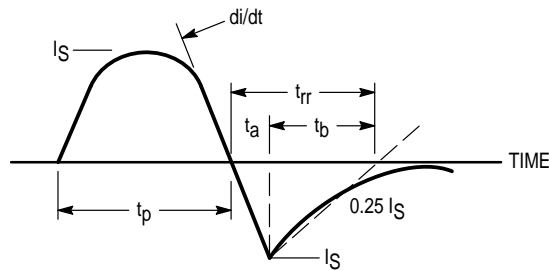
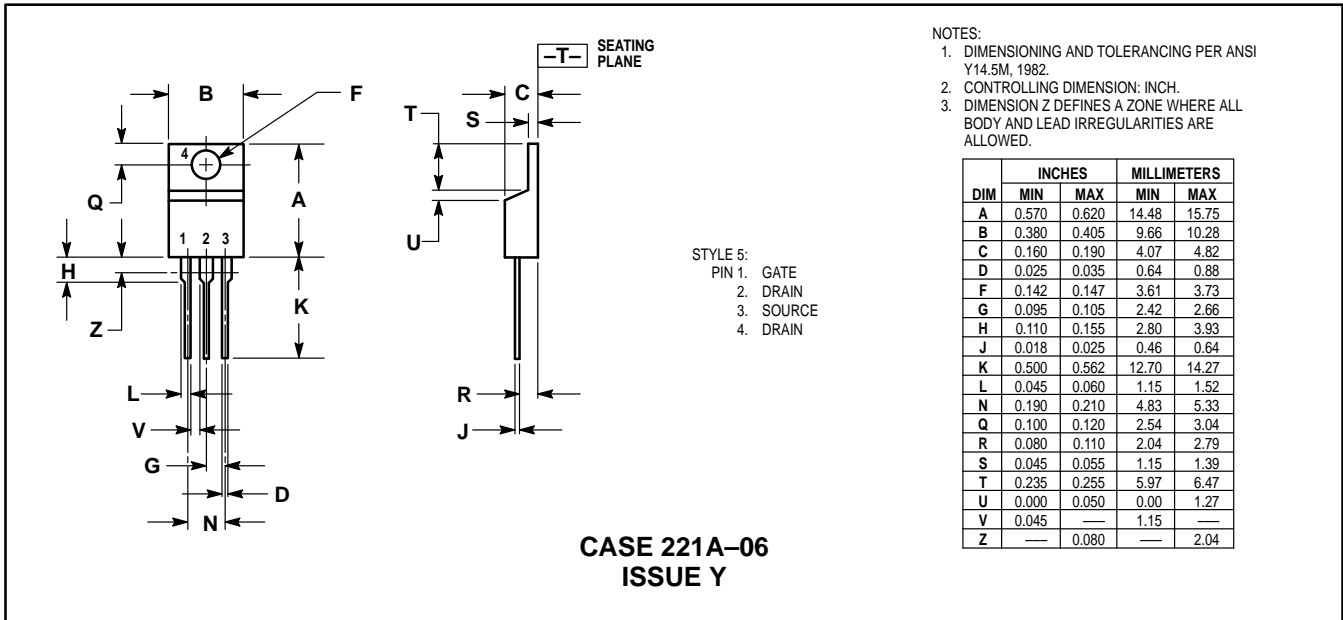


Figure 15. Diode Reverse Recovery Waveform

**MTP75N06HD**

**PACKAGE DIMENSIONS**



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: INCH.
  3. DIMENSION Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

Motorola reserves the right to make changes without further notice to any products herein. Motorola makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does Motorola assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation consequential or incidental damages. "Typical" parameters can and do vary in different applications. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. Motorola does not convey any license under its patent rights nor the rights of others. Motorola products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the Motorola product could create a situation where personal injury or death may occur. Should Buyer purchase or use Motorola products for any such unintended or unauthorized application, Buyer shall indemnify and hold Motorola and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that Motorola was negligent regarding the design or manufacture of the part. Motorola and are registered trademarks of Motorola, Inc. Motorola, Inc. is an Equal Opportunity/Affirmative Action Employer.

**How to reach us:**

**USA / EUROPE:** Motorola Literature Distribution;  
P.O. Box 20912; Phoenix, Arizona 85036. 1-800-441-2447

**JAPAN:** Nippon Motorola Ltd.; Tatsumi-SPD-JLDC, Toshikatsu Otsuki,  
6F Seibu-Butsuryu-Center, 3-14-2 Tatsumi Koto-Ku, Tokyo 135, Japan. 03-3521-8315

**MFAX:** RMFA00@email.sps.mot.com – TOUCHTONE (602) 244-6609  
**INTERNET:** http://Design-NET.com

**HONG KONG:** Motorola Semiconductors H.K. Ltd.; 8B Tai Ping Industrial Park,  
51 Ting Kok Road, Tai Po, N.T., Hong Kong. 852-26629298

