MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

Designer's Data Sheet

Power Field Effect Transistor

P-Channel Enhancement-Mode Silicon Gate

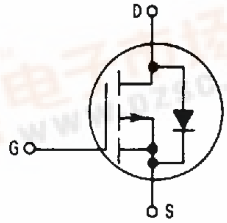
MTP8P10

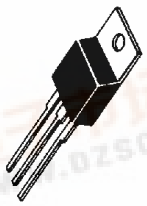
TMOS POWER FET
8 AMPERES
$R_{DS(on)}$ = 0.4 OHM
100 VOLTS

TMOS®

This TMOS Power FET is designed for medium voltage, high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds — Switching Times Specified at 100°C
- Designer's Data — I_{DSS}, $V_{DS(on)}$, $V_{GS(th)}$ and SOA Specified at Elevated Temperature
- Rugged — SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads





CASE 221A-06
TO-220AB

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MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	100	Vdc
Drain-Gate Voltage (R_{GS} = 1 MΩ)	V_{DGR}	100	Vdc
Gate-Source Voltage — Continuous — Non-repetitive ($t_p \leq 50\ \mu s$)	V_{GS} V_{GSM}	±20 ±40	Vdc Vpk
Drain Current — Continuous — Pulsed	I_D I_{DM}	8 25	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	75 0.6	Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	−65 to 150	°C

THERMAL CHARACTERISTICS

Thermal Resistance Junction to Case		$R_{\theta JC}$	1.67	°C/W
Junction to Ambient	TO-204	$R_{\theta JA}$	30	
	TO-220		62.5	
Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 5 seconds		T_L	260	°C

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 0.25 mA)	$V_{(BR)DSS}$	100	—	Vdc
Zero Gate Voltage Drain Current (V_{DS} = Rated V_{DSS}, V_{GS} = 0)	I_{DSS}	—	10	μAdc
(V_{DS} = Rated V_{DSS}, V_{GS} = 0, T_J = 125°C)		—	100	
Gate-Body Leakage Current, Forward (V_{GSF} = 20 Vdc, V_{DS} = 0)	I_{GSSF}	—	100	nAdc
Gate-Body Leakage Current, Reverse (V_{GSR} = 20 Vdc, V_{DS} = 0)	I_{GSSR}	—	100	nAdc
ON CHARACTERISTICS*				
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 1 mA)	$V_{GS(th)}$	2	4.5	Vdc
T_J = 100°C		1.5	4	
Static Drain-Source On-Resistance (V_{GS} = 10 Vdc, I_D = 4 Adc)	$R_{DS(on)}$	—	0.4	Ohm
Drain-Source On-Voltage (V_{GS} = 10 V) (I_D = 8 Adc)	$V_{DS(on)}$	—	4.8	Vdc
(I_D = 4 Adc, T_J = 100°C)		—	3	
Forward Transconductance (V_{DS} = 15 V, I_D = 4 A)	g_{FS}	2	—	mhos
DYNAMIC CHARACTERISTICS				
Input Capacitance	C_{iss}	—	1200	pF
Output Capacitance	C_{oss}	—	600	
Reverse Transfer Capacitance	C_{rss}	—	180	
SWITCHING CHARACTERISTICS* (T_J = 100°C)				
Turn-On Delay Time	$t_{d(on)}$	—	80	ns
Rise Time	t_r	—	150	
Turn-Off Delay Time	$t_{d(off)}$	—	200	
Fall Time	t_f	—	150	
Total Gate Charge	Q_g	33 (Typ)	50	nC
Gate-Source Charge	Q_{gs}	16 (Typ)	—	
Gate-Drain Charge	Q_{gd}	17 (Typ)	—	
SOURCE DRAIN DIODE CHARACTERISTICS*				
Forward On-Voltage	V_{SD}	3 (Typ)	6	Vdc
Forward Turn-On Time	t_{on}	Limited by stray inductance		
Reverse Recovery Time	t_{rr}	300 (Typ)	—	ns
INTERNAL PACKAGE INDUCTANCE (TO-220)				
Internal Drain Inductance (Measured from the contact screw on tab to center of die)	L_d	3.5 (Typ)	—	nH
(Measured from the drain lead 0.25" from package to center of die)		4.5 (Typ)	—	
Internal Source Inductance (Measured from the source lead 0.25" from package to source bond pad.)	L_s	7.5 (Typ)	—	

(V_{DS} = 25 V, V_{GS} = 0, f = 1 MHz) See Figure 11

(V_{DD} = 25 V, I_D = 0.5 Rated I_D, R_{gen} = 50 ohms) See Figures 9, 13 and 14

(V_{DS} = 0.8 Rated V_{DSS}, I_D = Rated I_D, V_{GS} = 10 V)

(I_S = Rated I_D, V_{GS} = 0)

*Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%

TYPICAL ELECTRICAL CHARACTERISTICS

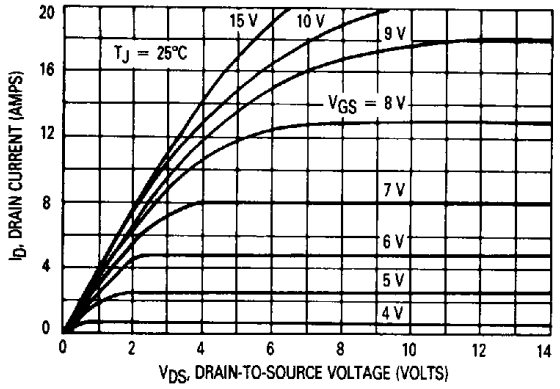

Figure 1. On-Region Characteristics

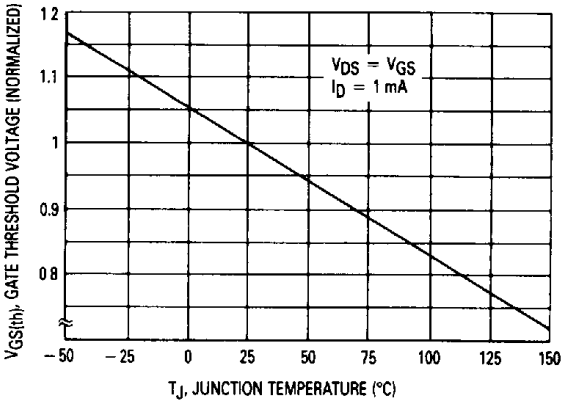

Figure 2. Gate-Threshold Voltage Variation With Temperature

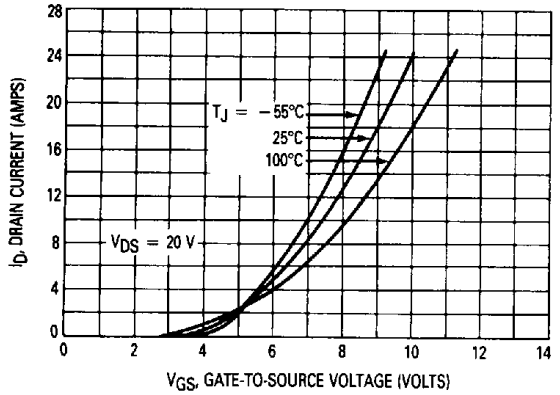

Figure 3. Transfer Characteristics

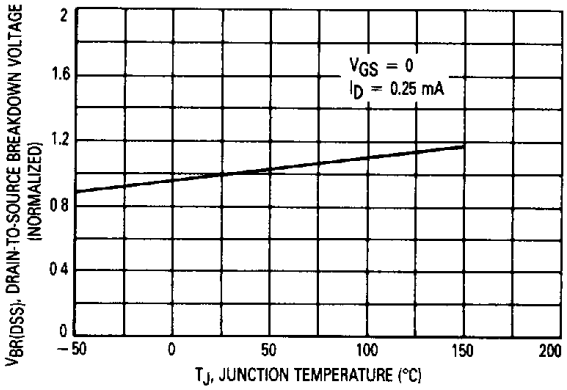

Figure 4. Normalized Breakdown Voltage versus Temperature

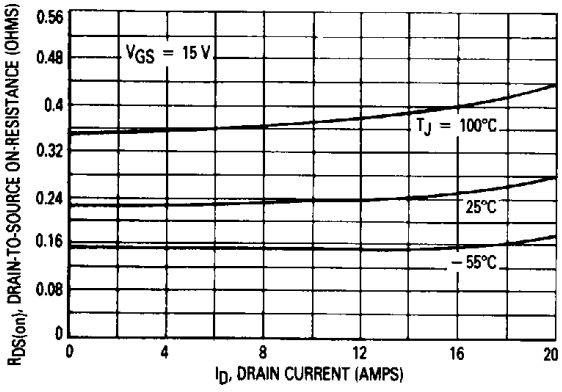

Figure 5. On-Resistance versus Drain Current

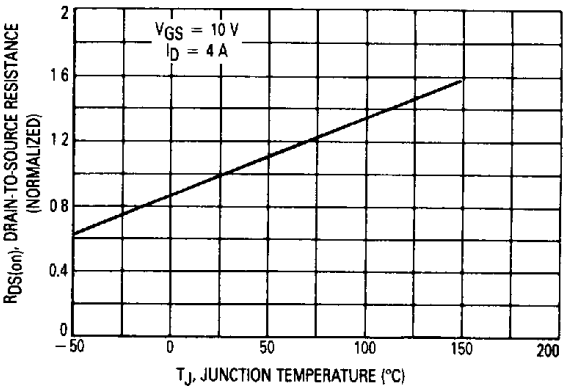

Figure 6. On-Resistance Variation With Temperature

SAFE OPERATING AREA INFORMATION

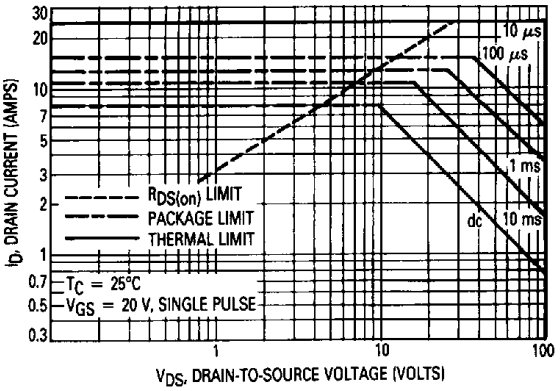

Figure 7. Maximum Rated Forward Biased Safe Operating Area

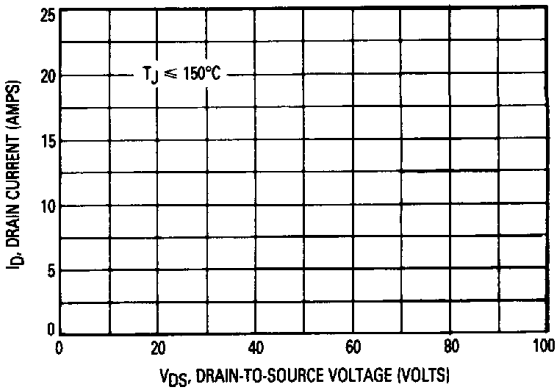

Figure 8. Maximum Rated Switching Safe Operating Area

FORWARD BIASED SAFE OPERATING AREA

The FBSOA curves define the maximum drain-to-source voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a case temperature of 25°C and a maximum junction temperature of 150°C. Limitations for repetitive pulses at various case temperatures can be determined by using the thermal response curves. Motorola Application Note, AN569, "Transient Thermal Resistance-General Data and Its Use" provides detailed instructions.

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 8 is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, I_{DM} and the breakdown voltage, $V_{(BR)DSS}$. The switching SOA shown in Figure 8 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

$$\frac{T_{J(max)} - T_C}{R_{\theta JC}}$$

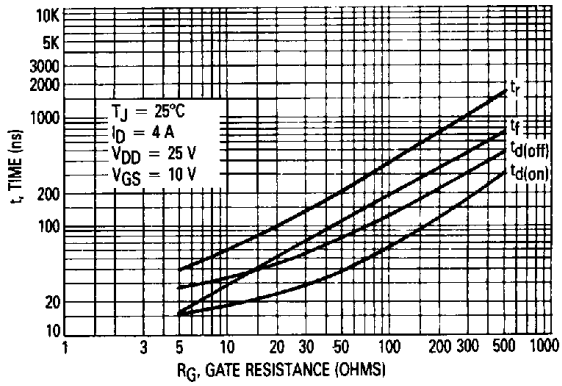

Figure 9. Resistive Switching Time Variation versus Gate Resistance

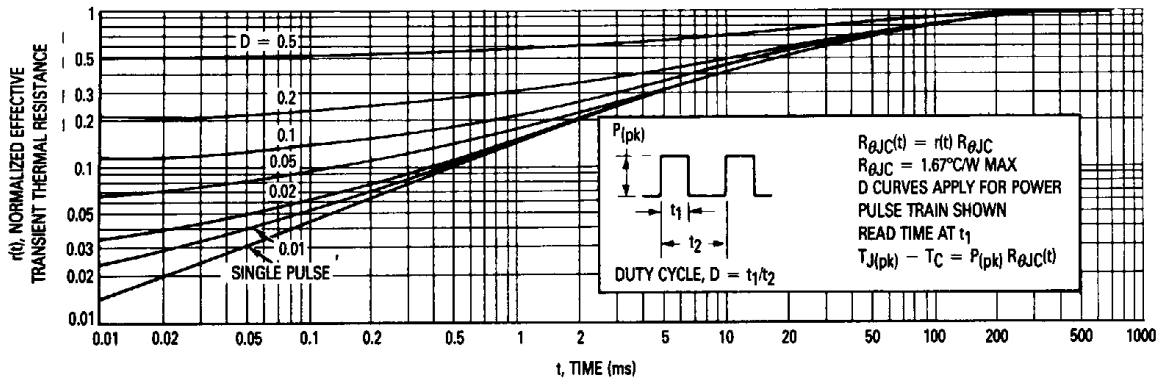

Figure 10. Thermal Response

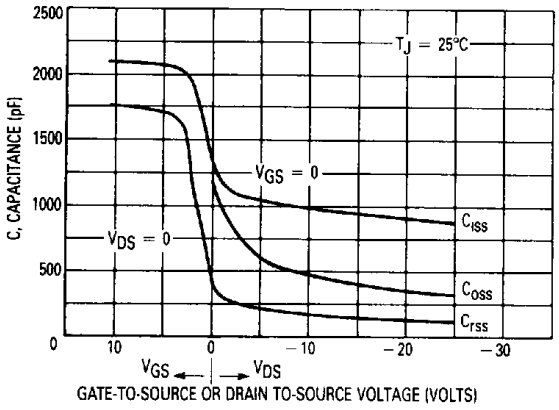

Figure 11. Capacitance Variation

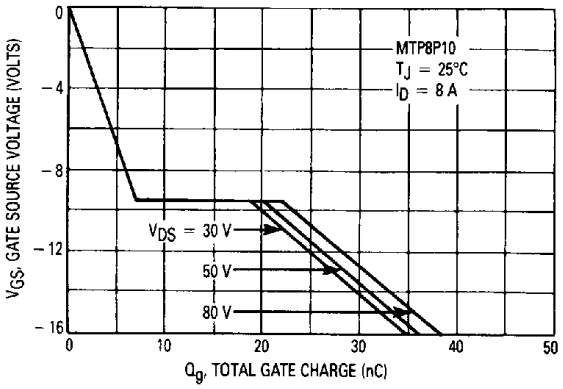

Figure 12. Gate Charge versus Gate-to-Source Voltage

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RESISTIVE SWITCHING

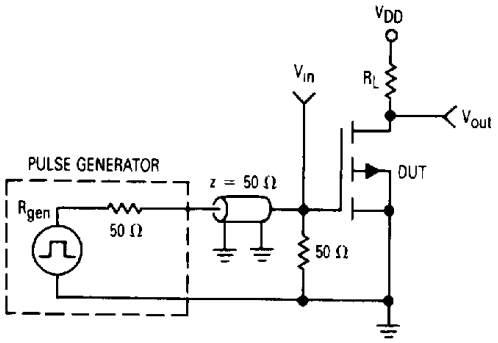

Figure 13. Switching Test Circuit

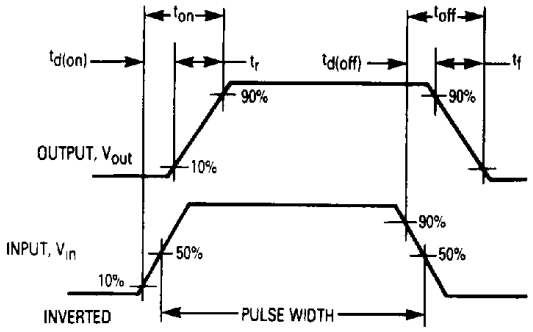

Figure 14. Switching Waveforms