MYSON TECHNOLOGY

MTV016

Enhanced On-Screen-Display Controller

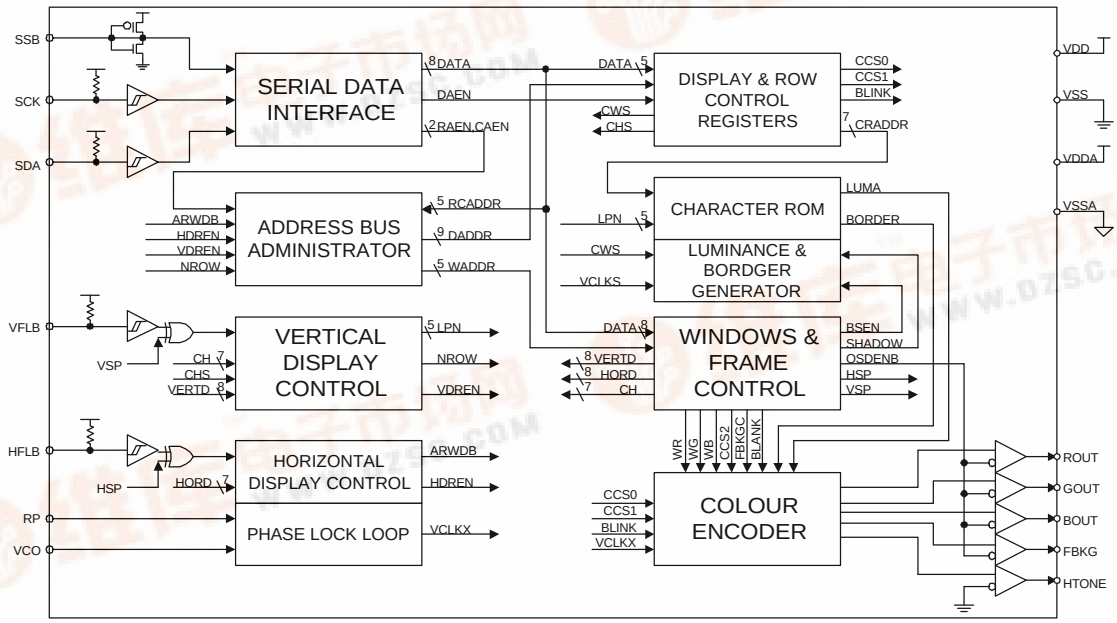
FEATURES

- Horizontal SYNC input up to 100 KHz.
- On-chip PLL circuitry up to a 90 MHz pixel rate for multi-SYNC operation.
- Programmable horizontal resolutions up to 1524 dots per display row.
- 538-byte display registers to control full screen display.
- Full screen display consists of 10 (rows) by 24 (columns) characters.
- 12 x 18 dot matrix per character.
- 128 built-in characters and graphic symbols, and character by character color selection.
- Maximum of 8 colors selectable per display row.
- Double character height and/or width control.
- Programmable positioning for display screen center.
- Bordering and shadowing effect for display.
- Programmable vertical character height (18 to 71 lines) for multi-SYNC operation.
- 4 programmable background windows with multi-level windowing effect.
- Software clear function for display frame buffer.
- HSYNC and VSYNC input polarity selectable.
- Auto detection for input edge distortion between HSYNC and VSYNC inputs.
- Half tone and fast blanking output.
- Software force blank function for display frame.
- Compatible with both SPI bus and I^2C interface through pin selection.
- 16-pin PDIP package.

GENERAL DESCRIPTION

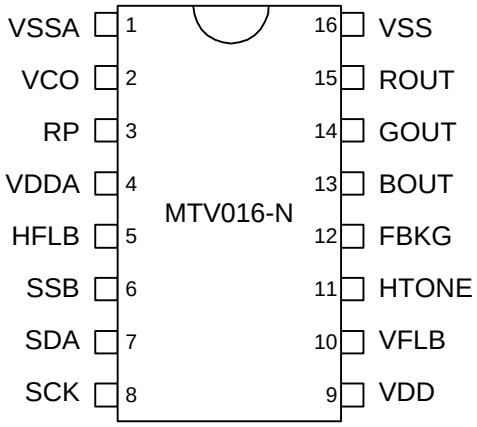
MTV016 is designed for use in monitor applications to display the built-in characters or symbols onto a monitor screen. The display operation occurs by transferring data and control information in the micro-controller to RAM through a serial data interface. It can execute a full screen display automatically and specific functions such as character bordering, shadowing, double height and width, font by font color control, frame positioning, frame size control by character height and horizontal display resolution, and windowing effect.

BLOCK DIAGRAM



1.0 CONNECTION DIAGRAM

(16-PIN PDIP 300 MIL PACKAGE)



2.0 PIN DESCRIPTIONS

Name	I/O	Pin#	Function
VSSA	-	1	**Analog Ground.** Used for internal analog circuitry.
VCO	I/O	2	**Voltage Control Oscillator.** Used to control the internal oscillator frequency by DC voltage input from an external low pass filter.
RP	I/O	3	**Bias Resistor.** Used to regulate the appropriate bias current for the internal oscillator to resonate at a specific dot frequency.
VDDA	-	4	**Analog Power Supply.** Positive 5 V DC supplies for internal analog circuitry. A 0.1uF decoupling capacitor should be connected across VDDA and VSSA.
HFLB	I	5	**Horizontal Input.** Used to input the horizontal synchronizing signal. It is negative edge triggered and has an internal 100 kΩ pull-up resistor.
SSB	I	6	**Serial Interface Enable.** Used to enable the serial data and to select I^2C or SPI bus operation. If this pin is left floating, the I^2C bus is enabled, otherwise the SPI bus is enabled.
SDA	I	7	**Serial Data Input.** Transfers data through this pin to the internal display and control registers. It has an internal 100 kΩ pull-up resistor.
SCK	I	8	**Serial Clock Input.** Used to synchronize the data transfer. It has an internal 100 kΩ pull-up resistor.
VDD	-	9	**Digital Power Supply.** Positive 5 V DC supply for internal digital circuitry and a 0.1uF decoupling capacitor should be connected across VDD and VSS.
VFLB	I	10	**Vertical Input.** Used to input the vertical synchronizing signal. It is negative triggered and has an internal pull-up resistor.
HTONE	O	11	**Half Tone Output.** Used to attenuate the external R, G, B amplifiers gain for the transparent windowing effect.
FBKG	O	12	**Fast Blanking Output.** Used to cut off the external R, G, B signals while this chip is displaying characters or windows.
BOUT	O	13	**Blue Color Output.** A blue color video signal output.
GOUT	O	14	**Green color output.** It is a green color video signal output.
ROUT	O	15	**Red Color Output.** A red color video signal output.
VSS	-	16	**Digital Ground.** Used for internal digital circuitry.

3.0 FUNCTIONAL DESCRIPTIONS

3.1 Serial Data Interface

The serial data interface receives data transmitted from an external controller. There are 2 types of bus that can be accessed through the serial data interface: SPI bus and I²C bus.

3.1.1 SPI Bus
While SSB pin is pulled to "high" or "low" level, the SPI bus operation is selected. A valid transmission should be started by pulling SSB to "low" level, enabling MTV016 in receiving mode, and retaining "low" level until the last cycle for a complete data packet transfer. The protocol is shown in Figure 2:

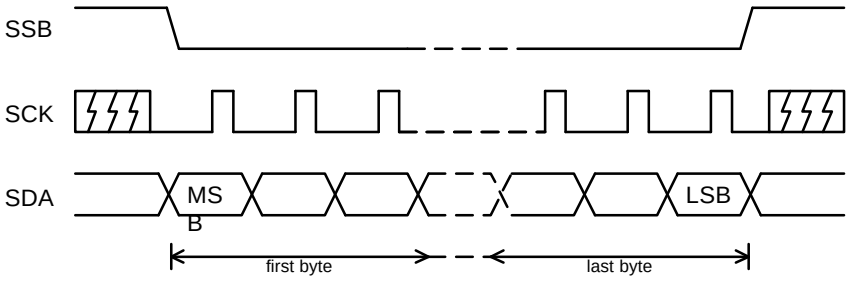


Figure 2. Data Transmission Protocol

There are 3 transmission formats as shown below:

Format (a) R - C - D → R - C - D → R - C - D .....
Format (b) R - C - D → C - D → C - D → C - D .....
Format (c) R - C - D → D → D → D → D → D .....

R=row address, C=column address, D=display data

3.1.2 I²C Bus
The I²C bus operation is only selected when the SSB pin is left floating. A valid transmission should begin by writing the slave address 7AH, which is the mask option, to MTV016. The protocol is shown in Figure 3:

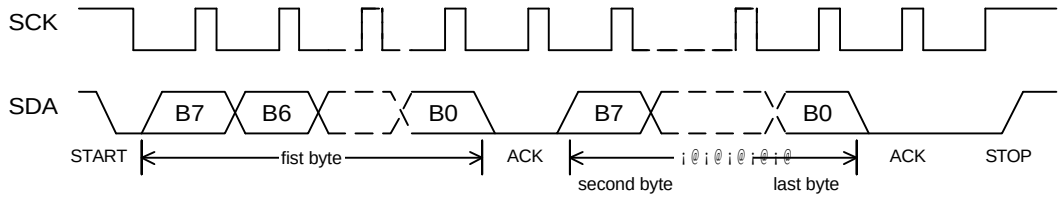


Figure 3. Data Transmission Protocol (I²C)

There are 3 transmission formats as shown below:

Format (a) S - R - C - D → R - C - D → R - C - D .....
Format (b) S - R - C - D → C - D → C - D → C - D .....
Format (c) S - R - C - D → D → D → D → D → D .....
S=slave address, R=row address, C=column address, D=display data

Each arbitrary length of data packet consists of 3 portions: row address (R), column address (C) and display data (D). Format (a) is suitable for updating small amounts of data, which will be allocated to different row and column addresses. Format (b) is recommended for updating data that has the same row address but a different column address. Massive data updating or a full screen data change should use format (c) to increase transmission efficiency. The row and column address will be incremented automatically when format (c) is applied. Furthermore, the undefined locations in display or font RAM should be filled with dummy data.

There are 2 types of data that should be accessed through the serial data interface: ADDRESS bytes and ATTRIBUTE bytes. The protocol is the same for both except for bit 6 of the row address. The MSB (b7) bit is used to distinguish row and column addresses when transferring data from the external controller. Bit 6 of the row address is used to distinguish the ADDRESS byte when it is set to "0" and the ATTRIBUTE byte when it is set to "1", or to differentiate the column address for formats (a), (b) and (c), respectively. The configuration of transmission formats is shown in Table 1:

Table 1. Configuration of Transmission Formats

	Address	b7	b6	b5	b4	b3	b2	b1	b0	Format
ADDRESS BYTES	Row	1	0	x	x	R3	R2	R1	R0	a,b,c
	$Column_{ab}$	0	0	x	C4	C3	C2	C1	C0	a,b
	$Column_{c}$	0	1	x	C4	C3	C2	C1	C0	c
ATTRIBUTE BYTES	Row	1	1	x	x	R3	R2	R1	R0	a,b,c
	$Column_{ab}$	0	0	x	C4	C3	C2	C1	C0	a,b
	$Column_{c}$	0	1	x	C4	C3	C2	C1	C0	c

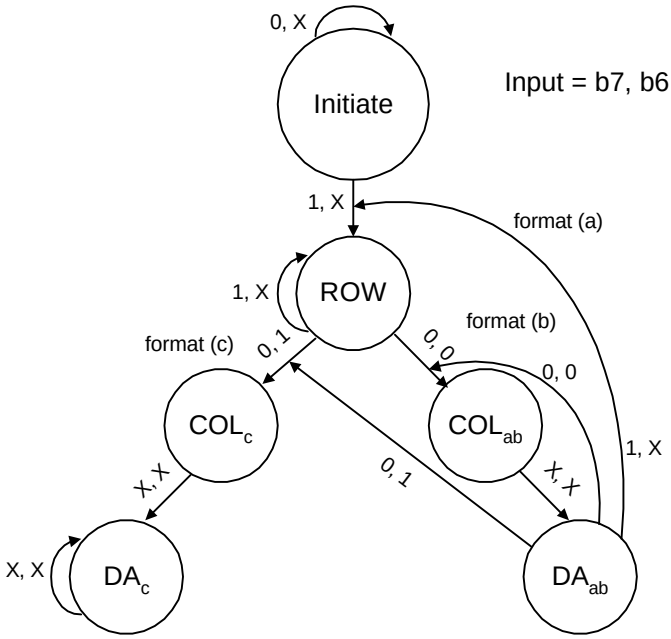


Figure 4. Transmission State Diagram

The data transmission is permitted to change from format (a) to formats (b) and (c), or from format (b) to format (a), but not from format (c) back to formats (a) and (b). The alternation between formats is configured as the state diagram shown in Figure 4.

3.2 Address Bus Administrator

The administrator manages bus address arbitration of internal registers during external data writing. The external data, which is written to registers through the serial data interface, must be synchronized by internal display timing. In addition, the administrator also provides automatic incrementing to the address bus when external writing using format (c).

3.3 Vertical Display Control

The vertical display control can generate different vertical display sizes for most display standards in current monitors. The vertical display size is calculated with the information of the double character height bit (CHS) and the vertical display height control register (CH6-CH0). The algorithm of repeating

character line displays is shown in Tables 2 and 3. The programmable vertical size range is 180 lines to a maximum of 1420 lines.

The vertical display center for a full screen display may be figured out according to the information of the vertical starting position register (VERTD) and VFLB input. The vertical delay starting from the leading edge of VFLB is calculated using the following equation:

vertical delay time = (VERTD * 4 + 1) * H
H = one horizontal line display time

Table 2. Repeat Line Weight of Character

CH6 - CH0	Repeat Line Weight
CH6,CH5=11	+18*3
CH6,CH5=10	+18*2
CH6,CH5=0x	+18
CH4=1	+16
CH3=1	+8
CH2=1	+4
CH1=1	+2
CH0=1	+1

Table 3. Repeat Line Number of Character

Repeat Line Weight	Repeat Line #																	
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
+1	-	-	-	-	-	-	-	-	v	-	-	-	-	-	-	-	-	-
+2	-	-	-	-	v	-	-	-	-	-	-	-	v	-	-	-	-	-
+4	-	-	v	-	-	-	v	-	-	-	v	-	-	-	v	-	-	-
+8	-	v	-	v	-	v	-	v	-	v	-	v	-	v	-	v	-	-
+16	-	v	v	v	v	v	v	v	v	v	v	v	v	v	v	v	v	-
+17	v	v	v	v	v	v	v	v	v	v	v	v	v	v	v	v	v	-
+18	v	v	v	v	v	v	v	v	v	v	v	v	v	v	v	v	v	v

Note:" v " means the nth line in the character would be repeated once, while " - " means the nth line in the character would not be repeated.

3.4 Horizontal Display Control

The horizontal display control is used to generate control timing for horizontal displays based on double character width bit (CWS), horizontal positioning register (HORD), horizontal resolution register (HORR) and HFLB input. A horizontal display line consists of (HORR*12) dots, including 288 dots for 24 display characters; the remaining dots are for a blank region. The horizontal delay starting from the HFLB leading edge is calculated using the following equation:

horizontal delay time = (HORD * 6 + 49) * P - phase error detection pulse width
P = one pixel display time = one horizontal line display time / (HORR*12)

3.5 Phase Lock Loop (PLL)

On-chip PLL generates system clock timing (VCLK) by tracking the input HFLB and horizontal resolution register (HORR). The frequency of VCLK is determined using the following equation:

VCLK Freq = HFLB Freq * HORR * 12

The VCLK frequency ranges from 5MHz to 90MHz and is selected by VCO1and VCO0. In addition, when HFLB input is not present for MTV016, the PLL will generate a specific system clock, approximately 2.5MHz, by a built-in oscillator to ensure data integrity.

3.6 Display & Row Control Registers

The internal RAM contains display and row control registers. The display registers have 240 locations that are allocated between row 0/column 0 and row 9/column 23, as shown in Figure 5. Each display register has a blink bit, and its corresponding character address on the ADDRESS byte and 2 color selection bits on the ATTRIBUTE bytes. The row control register is allocated between columns 28 and 31 for rows 0 to 9; it is used to set character size and color attribute for each respective row. If double width character is chosen, only even column characters may be displayed on-screen and the odd column characters will be hidden.

ROW #	**COLUMN #**		
	0 23	24 27	28 31
0 1 8 9	DISPLAY REGISTERS	RESERVED	ROW CTRL REG

ROW 10	**COLUMN #**				
	0 2	3 5	6 8	9 11	12 17
	WINDOW1	WINDOW2	WINDOW3	WINDOW4	FRAME CTRL REG

Figure 5. Memory Map

Register Descriptions

(i) Display Register

ADDRESS BYTE

b7	b6	b5	b4	b3	b2	b1	b0
BLINK	←			CRADDR			→

BLINK - Enables a blinking effect when this bit is set to " 1 ". The blinking alternates every 32 frames.
CRADDR - Defines the display character address and graphic symbols in ROM.

ATTRIBUTE BYTE

b7	b6	b5	b4	b3	b2	b1	b0
CCS1	CCS0	-	-	-	-	-	-

CCS1, CCS0 - These bits are used to select character color. Color 1 will be selected if these bits are set to 0/0, color 2 will be selected if these bits are set to 0/1, color 3 will be selected if these bits are set to 1/0 and color 4 will be selected if these bits are set to 1/1. Color 1, color 2, color 3 and color 4 are defined in the respective row control registers.

(ii) Row Control Registers

COLN 28	b7	b6	b5	b4	b3	b2	b1	b0
	R1	G1	B1	R2	G2	B2	CHS	CWS

b7 - 2 Color 1 is defined by R1, G1, B1 and color 2 by R2, G2, B2.
b1 CHS - Defines double height character to the respective row.
b0 CWS - Defines double width character to the respective row.

COLN 29	b7	b6	b5	b4	b3	b2	b1	b0
	R3	G3	B3	R4	G4	B4	-	-

b7 - 2 Color 3 is defined by R3, G3, B3 and color 4 by R4, G4, B4.

COLN 30	b7	b6	b5	b4	b3	b2	b1	b0
	R5	G5	B5	R6	G6	B6	-	-

b7 - 2 Color 5 and color 6 are defined by R5, G5, B5 and R6, G6, B6, respectively. When a window is overlapping with the character and the corresponding CCS2 is set to "1", color 5, color 6, color 7 and color 8 should be chosen.

COLN 31	b7	b6	b5	b4	b3	b2	b1	b0
	R7	G7	B7	R8	G8	B8	-	-

b7 - 2 Color 7 is defined by R7, G7, B7 and color 8 by R8, G8, B8.

3.7 Character ROM

The character ROM contains 128 built-in characters and symbols from address 0 to 127. Each character and symbol consists of a 12x18-dot matrix. The detailed pattern structures for each character and symbol are shown in **Section 10.0**.

3.8 Luminance & Border Generator

There are 2 shift registers included in the design that can shift out of luminance and border dots to the color encoder. The bordering and shadowing feature is configured in this block. For a bordering effect, the character will be enveloped with blackedge on 4 sides. For a shadowing effect, the character is enveloped with blackedge on the right and bottom sides only.

3.9 Window and Frame Control

The display frame position is completely controlled by the contents of VERTD and HORD. The window size and position control are specified in columns 0 to 11 on row 10 of the memory map, as shown in Figure 5. Window 1 has the highest priority and window 4 the least, when 2 windows are overlapping. More detailed information is described as follows:

(i) Window Control Registers

ROW 10

Column 0,3,6OR 9	b7	b6	b5	b4	b3	b2	b1	b0
	ROW START ADDR				ROW END ADDR			
	MSB			LSB	MSB			LSB

	b7	b6	b5	b4	b3	b2	b1	b0
Column 1,4,7OR 10	COL START ADDR					WEN	CCS2	-
	MSB				LSB			

	b7	b6	b5	b4	b3	b2	b1	b0
Column 2,5,8OR 11	COL END ADDR					R	G	B
	MSB				LSB			

START (END) ADDR - These addresses are used to specify the window size. It should be noted that when the start address is greater than the end address, the window will be disabled.
WEN - Enables the window display.
CCS2 - Extends the character color selection to include 8 colors.

(ii) Frame Control Registers

ROW 10

	b7	b6	b5	b4	b3	b2	b1	b0
Column 12				VERTD				
	MSB							LSB

VERTD - Specifies the starting position for the vertical display. The total number of steps is 256 and each step is incremented by 4 horizontal display lines. The initial value is 4 after power-up.

ROW 10

	b7	b6	b5	b4	b3	b2	b1	b0
Column 13				HORD				
	MSB							LSB

HORD - Defines the starting position for horizontal display. The total number of steps is 256 and each step is incremented by 6 dots. The initial value is 15 after power-up.

	b7	b6	b5	b4	b3	b2	b1	b0
Column14	-	CH6	CH5	CH4	CH3	CH2	CH1	CH0

CH6-CH0 - Defines the character vertical height; the height is programmable from 18 to 71 lines. The character vertical height is at least 18 lines if the content of CH6-CH0 is less than 18. For example, when the content is " 2 ", the character vertical height is regarded as equal to 20 lines. And if the content of CH4-CH0 is greater than or equal to 18, it will be regarded as equal to 17. See Tables 2 and 3 for a detailed description of this operation.

	b7	b6	b5	b4	b3	b2	b1	b0
Column15	-	HORR						
		MSB						LSB

HORR - Specifies the resolution of a horizontal display line, and the increment of each step is 12 dots. That is, the pixels' number per H line is equal to HORR*12. It is recommended that HORR be greater than or equal to 30 and smaller than 90M / (Hfreq*12). The initial value is 40 after power-up.

	b7	b6	b5	b4	b3	b2	b1	b0
Column16	OSDEN	BSEN	SHADOW	HSP	VSP	BLANK	RAMCLR	FBKGC

OSDEN - Activates the OSD operation when this bit is set to "1". The initial value is 0 after power-up.
BSEN - Enables the bordering and shadowing effect.

SHADOW - Activates the shadowing effect if this bit is set, otherwise the bordering is chosen.
VSP - = 1 ⇒ Accepts positive polarity VSYNC input.
= 0 ⇒ Accepts negative polarity VSYNC input.
HSP - = 1 ⇒ Accepts positive polarity HSYNC input.
= 0 ⇒ Accepts negative polarity HSYNC input.
BLANK - Forces the FBKG pin output to high while this bit is set to "1".
RAMCLR - Clears all ADDRESS bytes of display registers and WEN bits of window control registers when this bit is set to "1". The initial value is 0 after power-up.
FBKGC - Defines the output configuration for the FBKG pin. When it is set to "0", the FBKG outputs "high" during the display of characters or windows, otherwise it outputs "high" only during the display of characters.

Column17	b7	b6	b5	b4	b3	b2	b1	b0
	TEST	-	-	-	-	SELVCL	VCO1	VCO0

TEST - = 0 ⇒ Normal mode.
= 1 ⇒ Test mode, not allowed in applications.
SELVCL - Enables auto detection for horizontal and vertical SYNC input edge distortion when the bit is set to "1". The initial value is 1 after power-up.
VCO1, VCO0 - Selects the appropriate curve partitions of VCO frequency to voltage, based on HFLB input and horizontal resolution register (HORR).
= (0, 0) ⇒ 5MHz < HFLB Freq * HORR * 12 ≤ 30MHz
= (0, 1) ⇒ 30MHz < HFLB Freq * HORR * 12 ≤ 55MHz
= (1, 0) ⇒ 55MHz < HFLB Freq * HORR * 12 ≤ 75MHz
= (1, 1) ⇒ 75MHz < HFLB Freq * HORR * 12 ≤ 90MHz
The initial value is 0/0 after power-up.

3.11 Color Encoder

The decoder generates the video output to ROUT, GOUT and BOUT by integrating window color, border blackedge, luminance output and color selection output (CCS0, CCS1, CCS2) to form the desired video outputs.

4.0 ABSOLUTE MAXIMUM RATINGS

DC Supply Voltage (VDD, VDDA)	-0.3 to +7 V
Voltage with respect to Ground	-0.3 to VDD+0.3 V
Storage Temperature	-65 to +150 ^{O}C
Ambient Operating Temperature	0 to +70 ^{O}C

5.0 OPERATING CONDITIONS

DC Supply Voltage (VDD, VDDA)	+4.75 to +5.25 V
Operating Temperature	0 to +70 ^{O}C

6.0 ELECTRICAL CHARACTERISTICS (Under Operating Conditions)

Symbol	Parameter	Conditions(Notes)	Min.	Max.	Unit
V_{IH}	Input High Voltage	-	0.7 * VDD	VDD+0.3	V
V_{IL}	Input Low Voltage	-	VSS-0.3	0.3 * VDD (0.2 * VDD for SSB pin)	V
V_{OH}	Output High Voltage	$I_{OH} \leq$ -24 mA	VDD-0.8	-	V
V_{OL}	Output Low Voltage	$I_{OL} \leq$ 24 mA	-	0.5	V
I_{CC}	Supply Current	Vin = VDD, I_{load} = 0uA	-	25	mA

7.0 SWITCHING CHARACTERISTICS (Under Operating Conditions)

Symbol	Parameter	Min.	Typ.	Max.	Unit
f_{HFLB}	HFLB Input Frequency	15	-	100	KHz
T_r	Output Rise Time	-	-	5	ns
T_f	Output Fall Time	-	-	5	ns
t_{BCSU}	SSB to SCK Set-up Time	200	-	-	ns
t_{BCH}	SSB to SCK Hold Time	100	-	-	ns
t_{DCSU}	SDA to SCK Set-up Time	200	-	-	ns
t_{DCH}	SDA to SCK Hold Time	100	-	-	ns
t_{SCKH}	DCK High Time	500	-	-	ns
t_{SCKL}	DCK Low Time	500	-	-	ns
tSU: STA	START Condition Set-up Time	500	-	-	ns
tHD: STA	START Condition Hold Time	500	-	-	ns
tSU: STO	STOP Condition Set-up Time	500	-	-	ns
tHD: STO	STOP Condition Hold Time	500	-	-	ns

8.0 TIMING DIAGRAMS

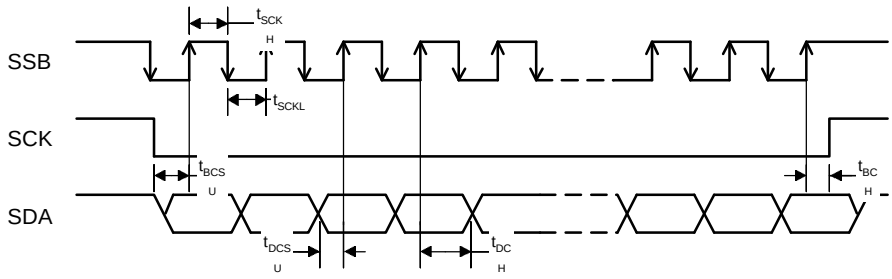


Figure 6. Data Interface Timing (SPI)

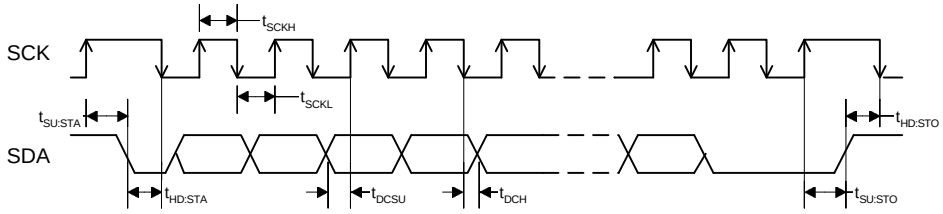


Figure 7. Data Interface Timing (I^2C)

9.0 CHARACTERS AND SYMBOL PATTERN

Please see attachment.

10.0 PACKAGE DIMENSION

16 Pin 300mil