

## The Wideband IC Line

# RF LDMOS Wideband Integrated Power Amplifiers

The MW4IC2020M wideband integrated circuit is designed for base station applications. It uses Motorola's newest High Voltage (26 to 28 Volts) LDMOS IC technology and integrates a multi-stage structure. Its wideband On-Chip design makes it usable from 1600 to 2400 MHz. The linearity performances cover all modulations for cellular applications: GSM, GSM EDGE, TDMA, CDMA and W-CDMA.

### Final Application

Typical Two-Tone Performance:  $V_{DD} = 26$  Volts,  $I_{DQ1} = 80$  mA,  $I_{DQ2} = 200$  mA,  $I_{DQ3} = 300$  mA,  $P_{out} = 20$  Watts PEP, Full Frequency Band

Power Gain — 29 dB

IMD — -32 dBc

Drain Efficiency — 26% (at 1805 MHz) and 20% (at 1990 MHz)

### Driver Applications

Typical GSM EDGE Performance:  $V_{DD} = 26$  Volts,  $I_{DQ1} = 80$  mA,  $I_{DQ2} = 230$  mA,  $I_{DQ3} = 230$  mA,  $P_{out} = 5$  Watts Avg., Full Frequency Band

Power Gain — 29 dB

Spectral Regrowth @ 400 kHz Offset = -66 dBc

Spectral Regrowth @ 600 kHz Offset = -77 dBc

EVM — 1% rms

Typical CDMA Performance:  $V_{DD} = 26$  Volts,  $I_{DQ1} = 80$  mA,  $I_{DQ2} = 240$  mA,  $I_{DQ3} = 250$  mA,  $P_{out} = 1$  Watt Avg., Full Frequency Band, IS-97 Pilot, Sync, Paging, Traffic Codes 8 through 13

Power Gain — 30 dB

ACPR @ 885 kHz Offset = -61 dBc @ 30 kHz Bandwidth

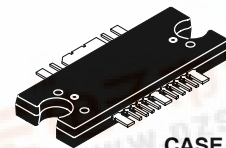
ALT1 @ 1.25 MHz Offset = -69 dBc @ 12.5 kHz Bandwidth

ALT2 @ 2.25 MHz Offset = -59 dBc @ 1 MHz Bandwidth

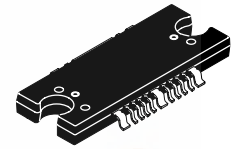
- Capable of Handling 3:1 VSWR, @ 26 Vdc, 1990 MHz, 8 Watts CW Output Power
- Characterized with Series Equivalent Large-Signal Impedance Parameters
- On-Chip Matching (50 Ohm Input, DC Blocked, >5 Ohm Output)
- Integrated Temperature Compensation with Enable/Disable Function
- On-Chip Current Mirror  $g_m$  Reference FET for Self Biasing Application (1)
- Integrated ESD Protection
- Also Available in Gull Wing for Surface Mount
- In Tape and Reel. R1 Suffix = 500 Units per 44 mm, 13 inch Reel

**MW4IC2020MBR1**  
**MW4IC2020GMBR1**

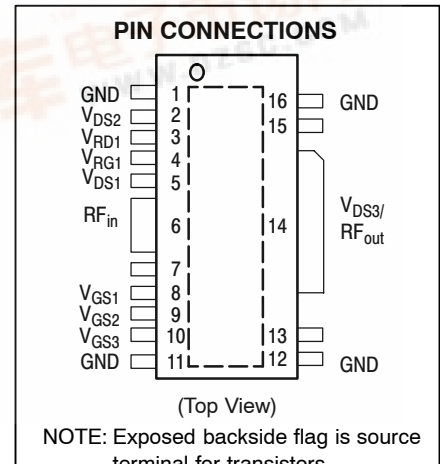
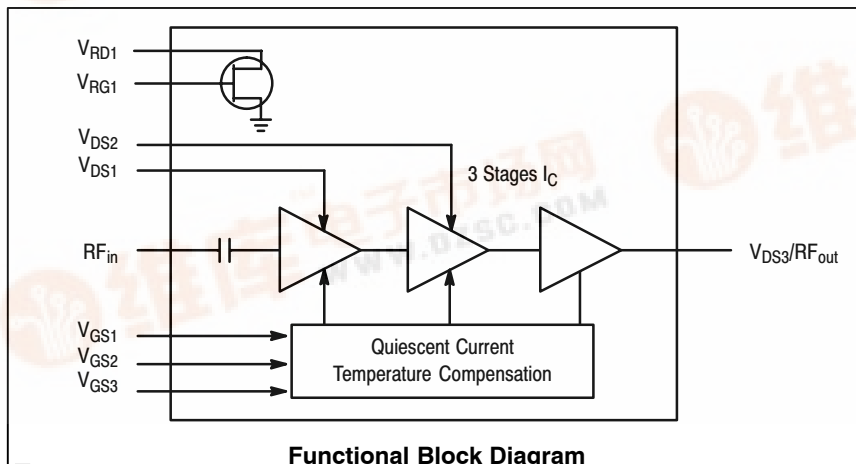
**1805-1990 MHz, 20 W, 26 V**  
**GSM/GSM EDGE, CDMA**  
**RF LDMOS WIDEBAND**  
**INTEGRATED POWER AMPLIFIERS**



CASE 1329-09  
 TO-272 WB-16  
 PLASTIC  
 MW4IC2020MBR1



CASE 1329A-03  
 TO-272 WB-16 GULL  
 PLASTIC  
 MW4IC2020GMBR1



Refer to AN1987/D, Quiescent Current Control for the RF Integrated Circuit Device Family. Go to <http://www.motorola.com/semiconductors/rf>.  
 Select Documentation/Application Notes - AN1987.



# Freescale Semiconductor, Inc.

## MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-Source Voltage	$V_{DSS}$	65	Vdc
Gate-Source Voltage	$V_{GS}$	-0.5, +15	Vdc
Storage Temperature Range	$T_{stg}$	-65 to +175	°C
Operating Junction Temperature	$T_J$	175	°C
Input Power	$P_{in}$	20	dBm

## THERMAL CHARACTERISTICS

Characteristic	Symbol	Value (1)	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	10.5 5.1 2.3	°C/W
		Stage 1	
		Stage 2	
		Stage 3	

## ESD PROTECTION CHARACTERISTICS

Test Conditions	Class
Human Body Model	2 (Minimum)
Machine Model	M3 (Minimum)
Charge Device Model	C5 (Minimum)

## MOISTURE SENSITIVITY LEVEL

Test Methodology	Rating
Per JESD 22-A113	3

## ELECTRICAL CHARACTERISTICS ( $T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
----------------	--------	-----	-----	-----	------

**FUNCTIONAL TESTS** (In Motorola Wideband 1805-1990 MHz Test Fixture, 50 ohm system)  $V_{DD} = 26$  Vdc,  $I_{DQ1} = 80$  mA,  $I_{DQ2} = 200$  mA,  $I_{DQ3} = 300$  mA,  $P_{out} = 20$  W PEP,  $f_1 = 1990$  MHz,  $f_2 = 1990.1$  MHz and  $f_1 = 1805$  MHz,  $f_2 = 1805.1$  MHz, Two-Tone CW

Power Gain	$G_{ps}$	27	29	—	dB
Drain Efficiency	$\eta_D$	24 18	26 20	—	%
		f1 = 1805 MHz, f2 = 1805.1 MHz			
		f1 = 1990 MHz, f2 = 1990.1 MHz			
Input Return Loss	IRL	—	—	-10	dB
Intermodulation Distortion	IMD	—	-32	-27	dBc
Stability (100 mW < $P_{out}$ < 8 W CW, Load VSWR = 3:1, All Phase Angles)		No Spurious > -60 dBc			

**TYPICAL PERFORMANCES** (In Motorola Test Fixture, 50 ohm system)  $V_{DD} = 26$  Vdc,  $I_{DQ1} = 80$  mA,  $I_{DQ2} = 200$  mA,  $I_{DQ3} = 300$  mA, 1805 MHz < Frequency < 1990 MHz, 1-Tone

Saturated Pulsed Output Power (f = 1 kHz, Duty Cycle 10%)	$P_{sat}$	—	33	—	Watts
Quiescent Current Accuracy over Temperature (-10 to 85°C)	$\Delta I_{QT}$	—	±5	—	%
Gain Flatness in 30 MHz Bandwidth @ $P_{out} = 1$ W CW	$G_F$	—	0.15	—	dB
Deviation from Linear Phase in 30 MHz Bandwidth @ $P_{out} = 1$ W CW 1805-1880 MHz 1930-1990 MHz	$\Phi$	—	±0.5 ±0.2	—	°
Delay @ $P_{out} = 1$ W CW Including Output Matching	Delay	—	1.8	—	ns
Part to Part Phase Variation @ $P_{out} = 1$ W CW	$\Phi_{\Delta}$	—	±10	—	°

(1) MTTF calculator available at <http://www.motorola.com/semiconductors/rf>. Select Tools/Software/Application Software/Calculators to access the MTTF calculators by product.

(continued)

# Freescale Semiconductor, Inc.

## ELECTRICAL CHARACTERISTICS — continued ( $T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
----------------	--------	-----	-----	-----	------

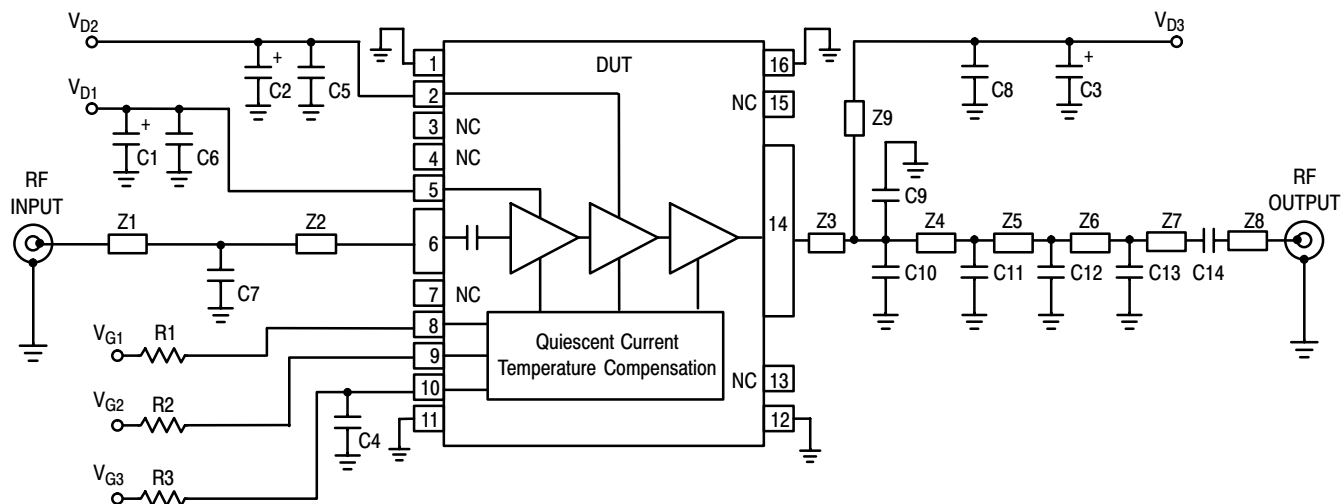
**TYPICAL CDMA PERFORMANCES** (In Modified CDMA Test Fixture, 50 ohm system)  $V_{DD} = 26\text{ Vdc}$ ,  $I_{DQ1} = 80\text{ mA}$ ,  $I_{DQ2} = 240\text{ mA}$ ,  $I_{DQ3} = 250\text{ mA}$ ,  $P_{out} = 1\text{ W Avg.}$ , 11930 MHz < Frequency < 1990 MHz, 1-Tone, 9 Channel Forward Model (Pilot, Paging, Sync, Traffic Codes 8 through 13). Peak/Avg. Ratio 9.8 dB @ 0.01% Probability on CCDF.

Power Gain	$G_{ps}$	—	30	—	dB
Drain Efficiency	$\eta_D$	—	5	—	%
Adjacent Channel Power Ratio ( $\pm 885\text{ kHz @ } 30\text{ kHz Bandwidth}$ )	ACPR	—	-61	—	dBc
Alternate 1 Channel Power Ratio ( $\pm 1.25\text{ MHz @ } 12.5\text{ kHz Bandwidth}$ )	ALT1	—	-69	—	dBc
Alternate 2 Channel Power Ratio ( $\pm 2.25\text{ MHz @ } 1\text{ MHz Bandwidth}$ )	ALT2	—	-59	—	dBc

**TYPICAL GSM EDGE PERFORMANCES** (In Modified GSM EDGE Test Fixture, 50 ohm system)  $V_{DD} = 26\text{ Vdc}$ ,  $I_{DQ1} = 80\text{ mA}$ ,  $I_{DQ2} = 230\text{ mA}$ ,  $I_{DQ3} = 230\text{ mA}$ ,  $P_{out} = 5\text{ W Avg.}$ , 1805 MHz < Frequency < 1990 MHz

Power Gain	$G_{ps}$	—	29	—	dB
Drain Efficiency	$\eta_D$	—	15	—	%
Error Vector Magnitude	EVM	—	1	—	% rms
Spectral Regrowth at 400 kHz Offset	SR1	—	-66	—	dBc
Spectral Regrowth at 600 kHz Offset	SR2	—	-77	—	dBc

# Freescale Semiconductor, Inc.



Z1	1.820" x 0.087" Microstrip	Z6	0.303" x 0.087" Microstrip
Z2	0.245" x 0.087" Microstrip	Z7	0.640" x 0.087" Microstrip
Z3	0.345" x 0.236" Microstrip	Z8	0.334" x 0.087" Microstrip
Z4	0.327" x 0.087" Microstrip	Z9	1.231" x 0.043" Microstrip
Z5	0.271" x 0.087" Microstrip	PCB	Taconic TLX8-0300, 0.030", $\epsilon_r = 2.55$

Figure 1. MW4IC2020MBR1(GMBR1) Test Circuit Schematic

Table 1. MW4IC2020MBR1(GMBR1) Test Circuit Component Designations and Values

Part	Description	Part Number	Manufacturer
C1, C2, C3	10 $\mu$ F, 35 V Tantalum Capacitors	TAJE226M035	AVX
C4	220 nF Chip Capacitor (1206)	12065C224K28	AVX
C5, C6, C8	6.8 pF 100B Chip Capacitors	100B6R8CW	ATC
C7	0.5 pF 100B Chip Capacitor	100B0R5BW	ATC
C9, C11	1.8 pF 100B Chip Capacitors	100B1R8BW	ATC
C10	2.2 pF 100B Chip Capacitor	100B2R2BW	ATC
C12	1 pF 100B Chip Capacitor	100B1R0BW	ATC
C13	0.3 pF 100B Chip Capacitor	100B0R3BW	ATC
C14	10 pF 100B Chip Capacitor	100B100GW	ATC
R1, R2, R3	1.8 k $\Omega$ Chip Resistors (1206)		

# Freescale Semiconductor, Inc.

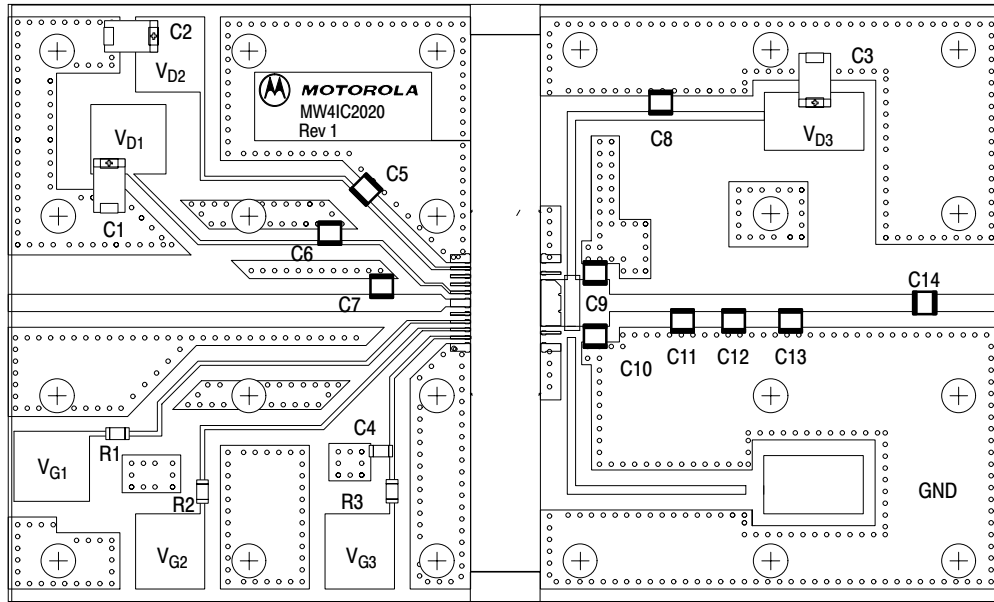


Figure 2. MW4IC2020MBR1(GMBR1) Test Circuit Component Layout

# Freescale Semiconductor, Inc.

## TYPICAL CHARACTERISTICS

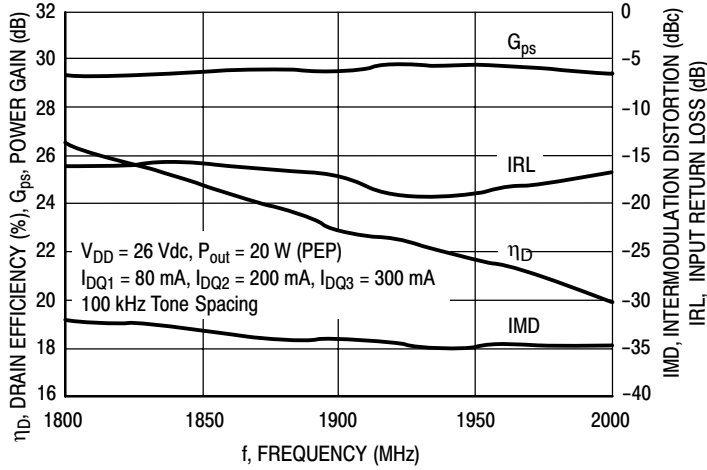


Figure 3. Two-Tone Wideband Performance

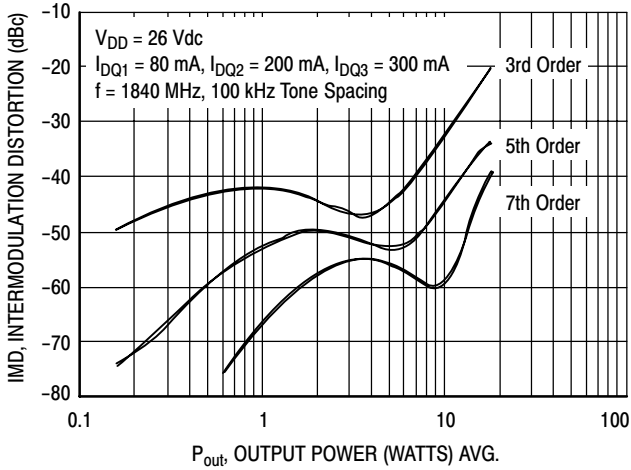


Figure 4. Intermodulation Distortion Products versus Output Power

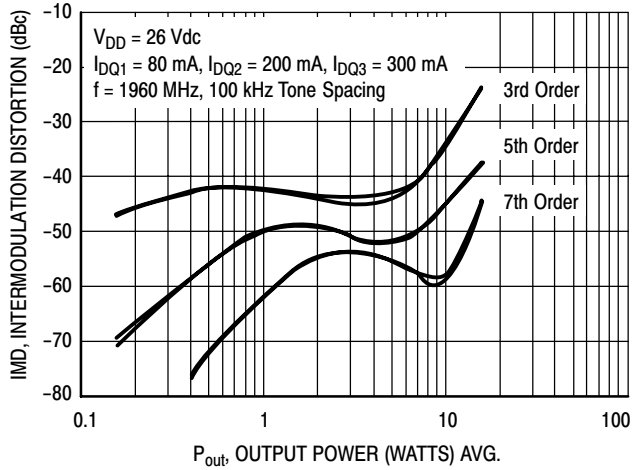


Figure 5. Intermodulation Distortion Products versus Output Power

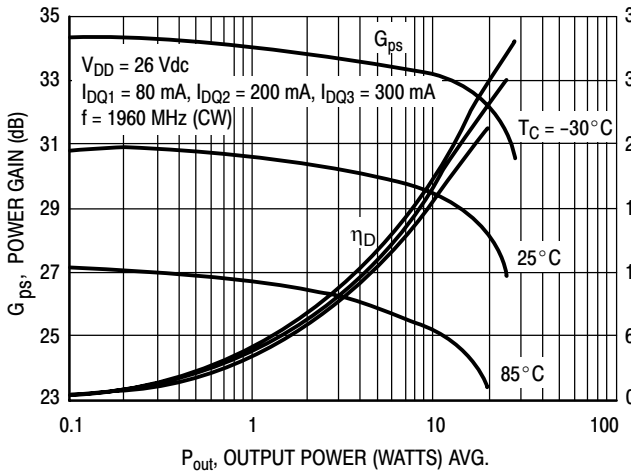


Figure 6. Power Gain and Drain Efficiency versus Output Power

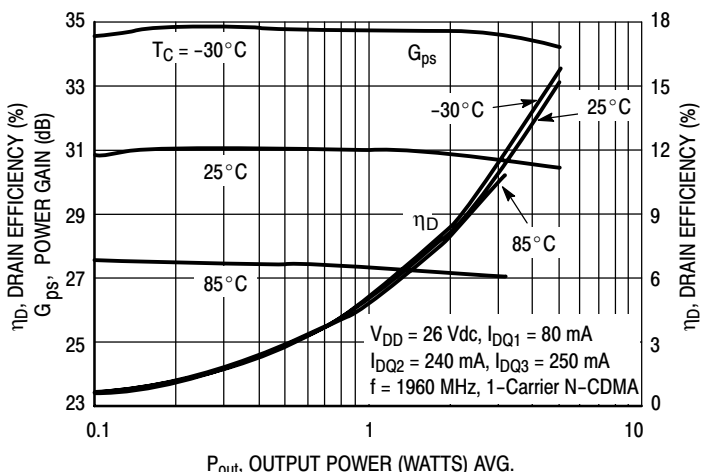
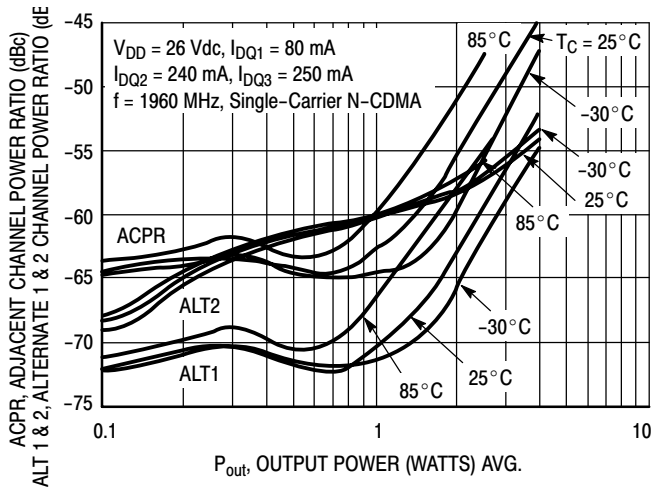


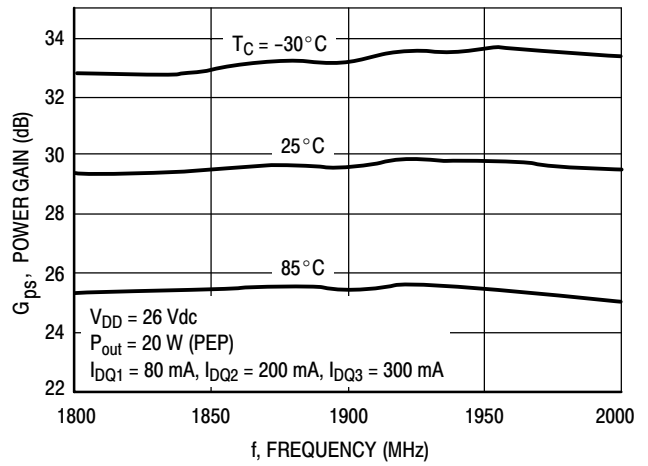
Figure 7. Power Gain and Drain Efficiency versus Output Power

# Freescale Semiconductor, Inc.

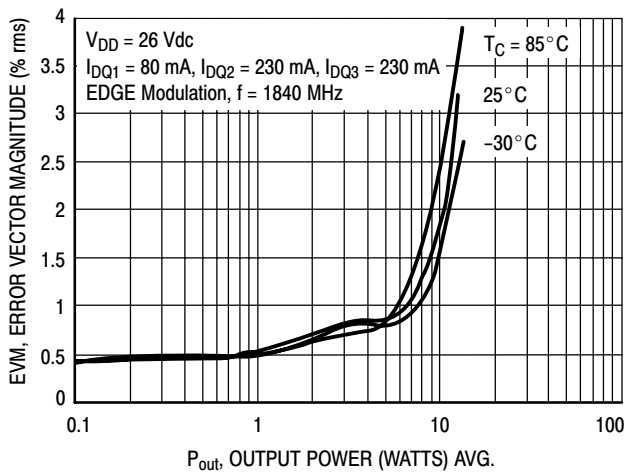
## TYPICAL CHARACTERISTICS



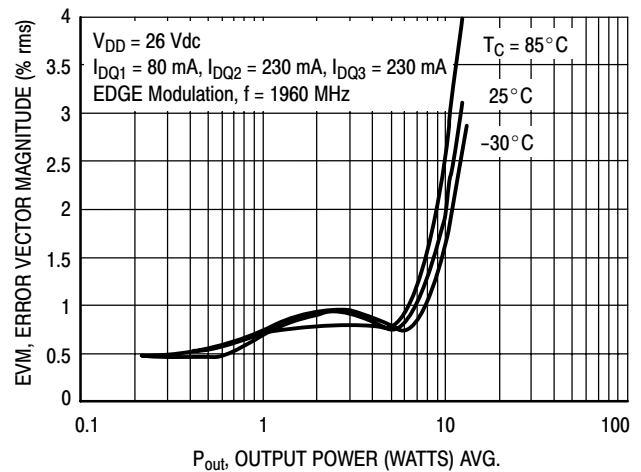
**Figure 8. Alternate Channel Power Ratio, Alternate 1 and 2 Channel Power Ratio versus Output Power**



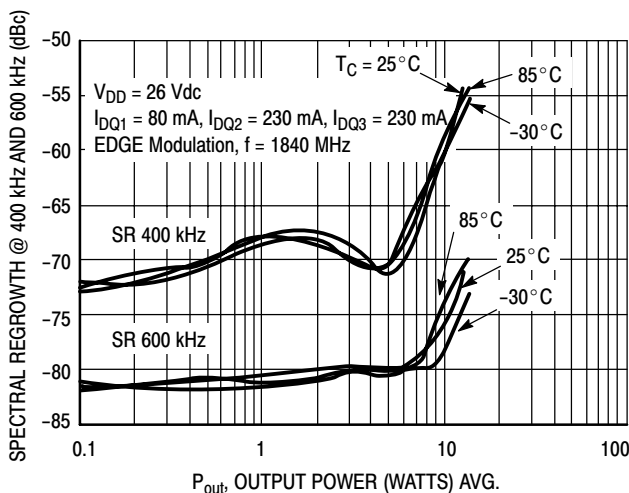
**Figure 9. Power Gain versus Frequency**



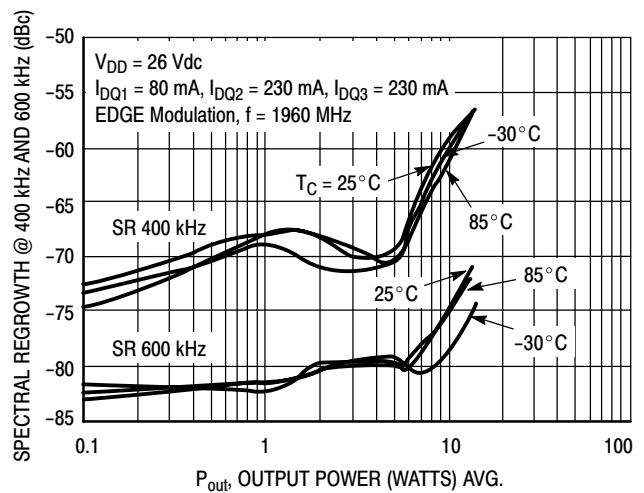
**Figure 10. Error Vector Magnitude versus Output Power**



**Figure 11. Error Vector Magnitude versus Output Power**



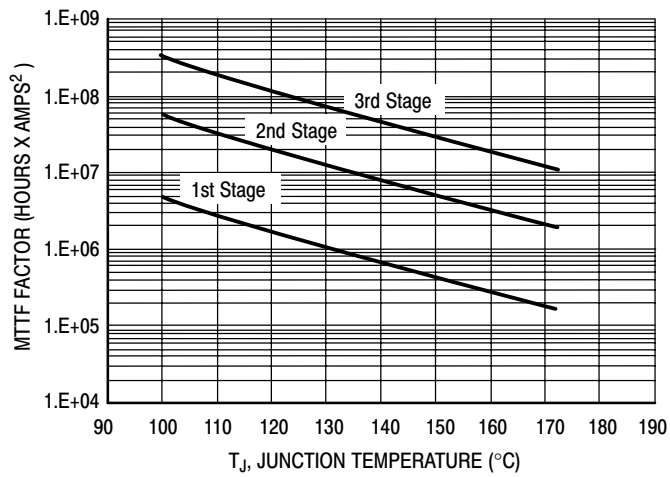
**Figure 12. Spectral Regrowth at 400 and 600 kHz versus Output Power**



**Figure 13. Spectral Regrowth at 400 and 600 kHz versus Output Power**

# Freescale Semiconductor, Inc.

## TYPICAL CHARACTERISTICS

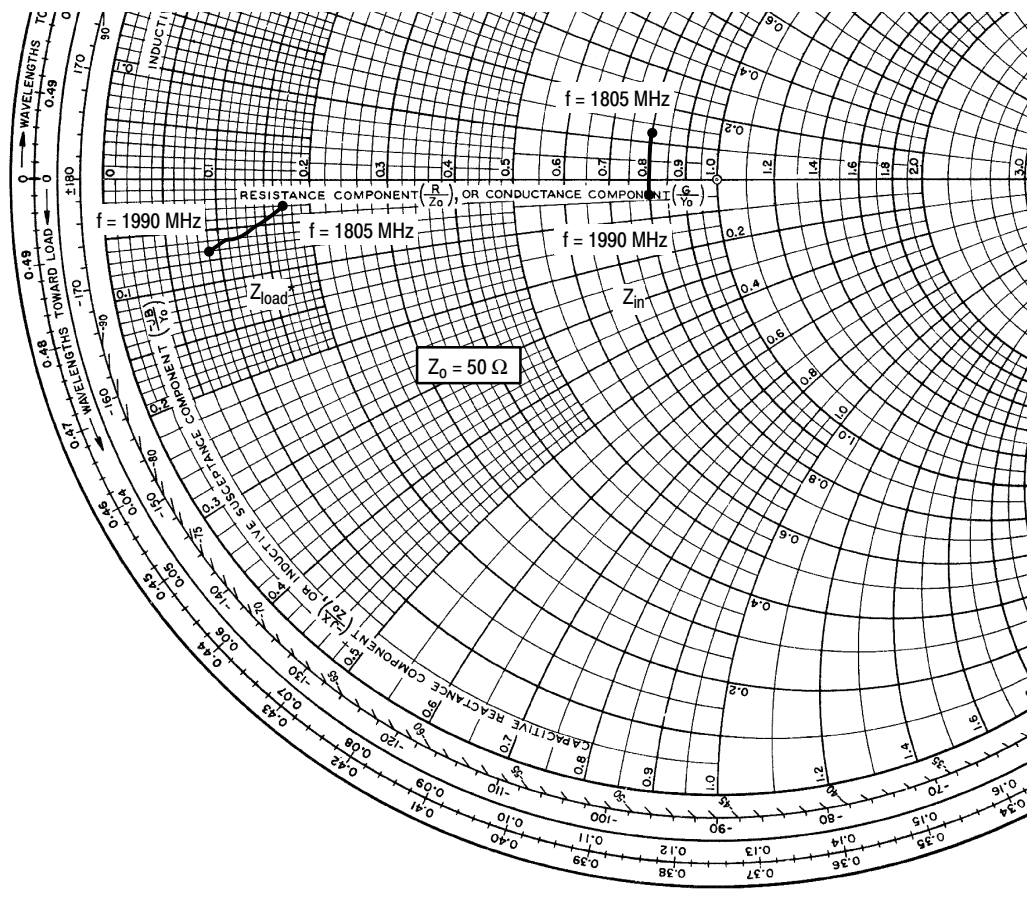


This above graph displays calculated MTTF in hours x ampere<sup>2</sup> drain current. Life tests at elevated temperatures have correlated to better than ±10% of the theoretical prediction for metal failure. Divide MTTF factor by  $I_D^2$  for MTTF in a particular application.

**Figure 14. MTTF Factor versus Junction Temperature**



# Freescale Semiconductor, Inc.



$V_{DD} = 26\text{ V}$ ,  $I_{DQ1} = 80\text{ mA}$ ,  $I_{DQ2} = 200\text{ mA}$ ,  $I_{DQ1} = 300\text{ mA}$ ,  $P_{out} = 20\text{ W PEP Two-Tone CW}$

f MHz	$Z_{in}$ $\Omega$	$Z_{load}$ $\Omega$
1805	$40.00 + j6.50$	$8.75 - j1.42$
1842	$40.00 + j2.00$	$7.00 - j2.70$
1880	$40.00 - j1.50$	$5.90 - j2.97$
1930	$40.00 - j1.80$	$5.46 - j3.20$
1960	$40.00 - j2.10$	$4.30 - j3.35$
1990	$40.00 - j2.60$	$4.45 - j3.30$

$Z_{in}$  = Device input impedance as measured from gate to ground.

$Z_{load}$  = Test circuit impedance as measured from drain to ground.

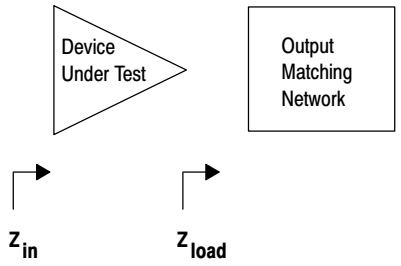
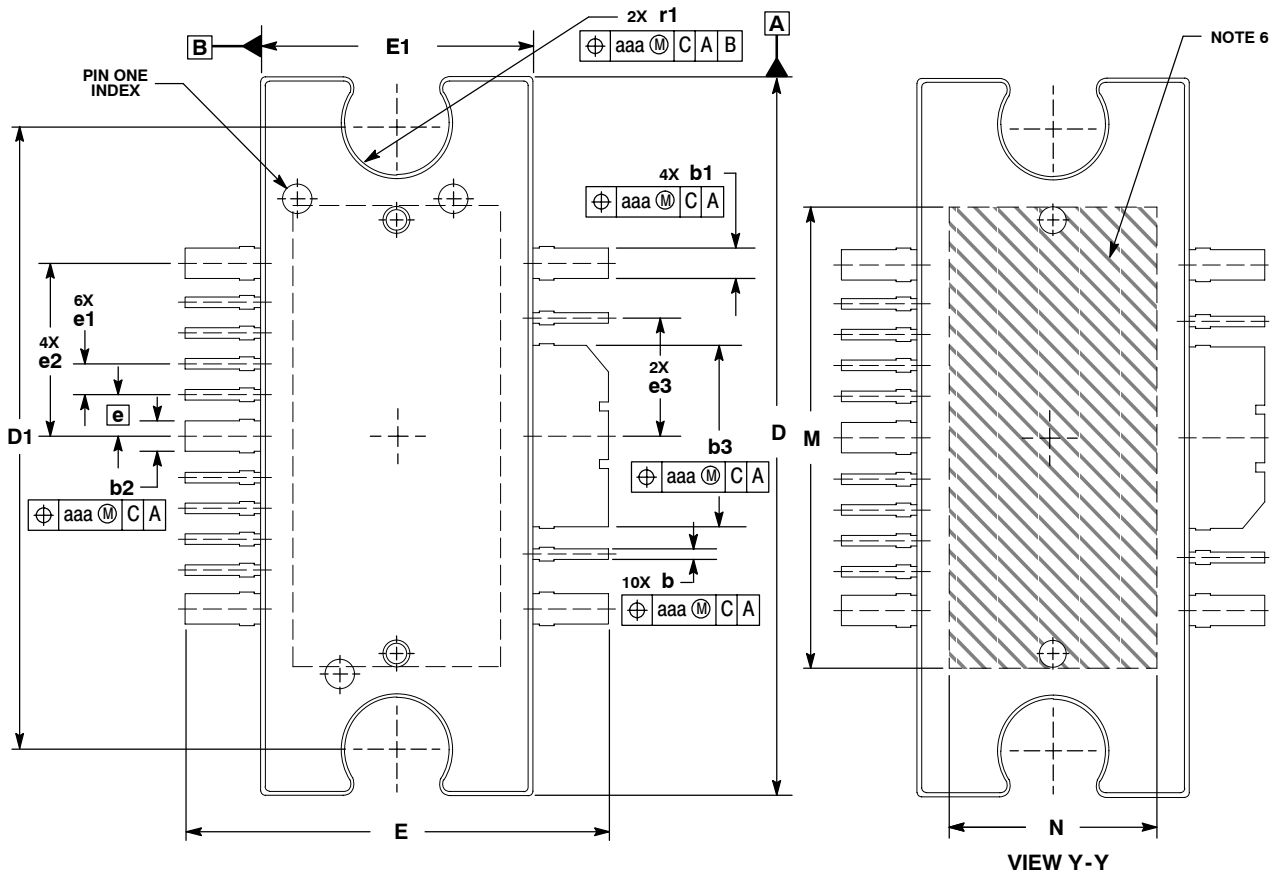


Figure 15. Series Equivalent Output Impedance

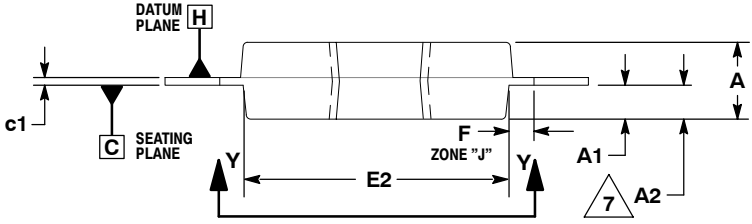
# Freescale Semiconductor, Inc.

## PACKAGE DIMENSIONS



NOTE 6

VIEW Y-Y



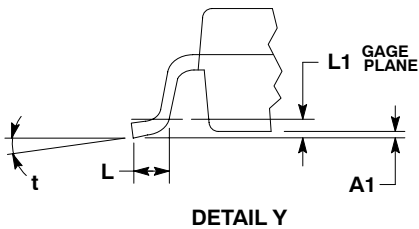
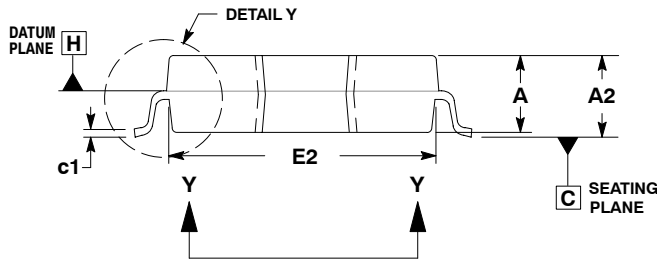
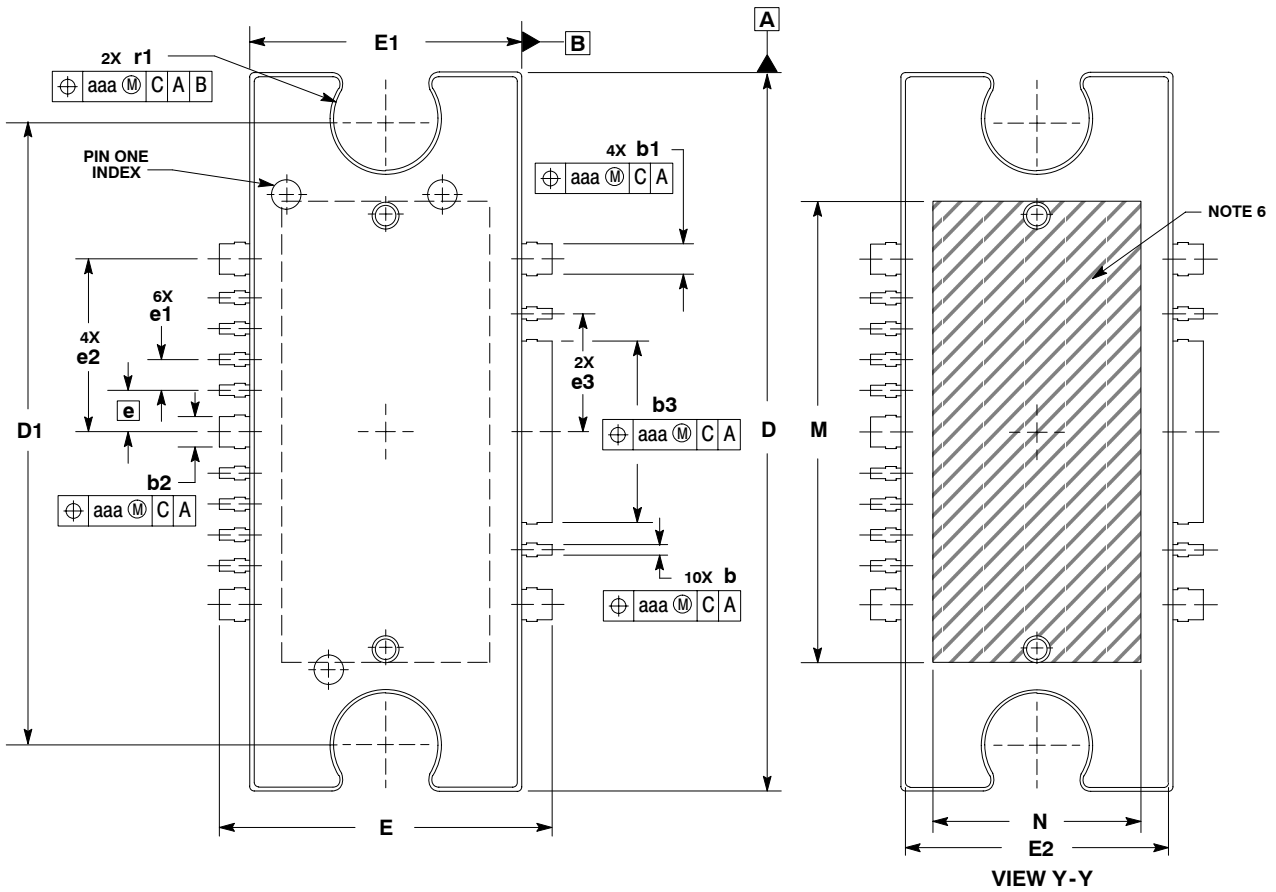
- NOTES:
1. CONTROLLING DIMENSION: INCH.
  2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M-1994.
  3. DATUM PLANE -H- IS LOCATED AT TOP OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE TOP OF THE PARTING LINE.
  4. DIMENSIONS "D" AND "E1" DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS .006 (0.15) PER SIDE. DIMENSIONS "D" AND "E1" DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE -H-.
  5. DIMENSIONS "b", "b1", "b2" AND "b3" DO NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE .005 (0.13) TOTAL IN EXCESS OF THE "b", "b1", "b2" AND "b3" DIMENSIONS AT MAXIMUM MATERIAL CONDITION.
  6. HATCHING REPRESENTS THE EXPOSED AREA OF THE HEAT SLUG.
  7. DIM A2 APPLIES WITHIN ZONE "J" ONLY.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.100	.104	2.54	2.64
A1	.038	.044	0.96	1.12
A2	.040	.042	1.02	1.07
D	.928	.932	23.57	23.67
D1	.810 BSC		20.57 BSC	
E	.551	.559	14.00	14.20
E1	.353	.357	8.97	9.07
E2	.346	.350	8.79	8.89
F	.025 BSC		0.64 BSC	
M	.600	---	15.24	---
N	.270	---	6.86	---
b	.011	.017	0.28	0.43
b1	.037	.043	0.94	1.09
b2	.037	.043	0.94	1.09
b3	.225	.231	5.72	5.87
c1	.007	.011	.18	.28
e	.054 BSC		1.37 BSC	
e1	.040 BSC		1.02 BSC	
e2	.224 BSC		5.69 BSC	
e3	.150 BSC		3.81 BSC	
r1	.063	.068	1.6	1.73
aaa	.004		.10	

**CASE 1329-09**  
**ISSUE J**  
**TO-272 WB-16**  
**PLASTIC**  
**MW4IC2020MBR1**

# Freescale Semiconductor, Inc.

Freescale Semiconductor, Inc.



- NOTES:
1. CONTROLLING DIMENSION: INCH.
  2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M-1994.
  3. DATUM PLANE -H- IS LOCATED AT TOP OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE TOP OF THE PARTING LINE.
  4. DIMENSIONS "D" AND "E1" DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS .006 (0.15) PER SIDE. DIMENSIONS "D" AND "E1" DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE -H-.
  5. DIMENSIONS "b", "b1", "b2" AND "b3" DO NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE .005 (0.13) TOTAL IN EXCESS OF THE "b", "b1", "b2" AND "b3" DIMENSIONS AT MAXIMUM MATERIAL CONDITION.
  6. HATCHING REPRESENTS THE EXPOSED AREA OF THE HEAT SINK.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.100	.104	2.54	2.64
A1	.001	.004	0.02	0.10
A2	.099	.110	2.51	2.79
D	.928	.932	23.57	23.67
D1	.810 BSC		20.57 BSC	
E	.429	.437	10.90	11.10
E1	.353	.357	8.97	9.07
E2	.346	.350	8.79	8.89
L	.018	.024	4.90	5.06
L1	.01 BSC		0.25 BSC	
M	.600	---	15.24	---
N	.270	---	6.86	---
b	.011	.017	0.28	0.43
b1	.037	.043	0.94	1.09
b2	.037	.043	0.94	1.09
b3	.225	.231	5.72	5.87
c1	.007	.011	.18	.28
e	.054 BSC		1.37 BSC	
e1	.040 BSC		1.02 BSC	
e2	.224 BSC		5.69 BSC	
e3	.150 BSC		3.81 BSC	
r1	.063	.068	1.6	1.73
t	2°	8°	2°	8°
aaa	.004		.10	

**CASE 1329A-03  
ISSUE B  
TO-272 WB-16 GULL  
PLASTIC  
MW4IC2020GMBR1**

# Freescale Semiconductor, Inc.

Information in this document is provided solely to enable system and software implementers to use Motorola products. There are no express or implied copyright licenses granted hereunder to design or fabricate any integrated circuits or integrated circuits based on the information in this document.

Motorola reserves the right to make changes without further notice to any products herein. Motorola makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does Motorola assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation consequential or incidental damages. "Typical" parameters that may be provided in Motorola data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals", must be validated for each customer application by customer's technical experts. Motorola does not convey any license under its patent rights nor the rights of others. Motorola products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the Motorola product could create a situation where personal injury or death may occur. Should Buyer purchase or use Motorola products for any such unintended or unauthorized application, Buyer shall indemnify and hold Motorola and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that Motorola was negligent regarding the design or manufacture of the part.

MOTOROLA and the Stylized M Logo are registered in the US Patent and Trademark Office. All other product or service names are the property of their respective owners. Motorola, Inc. is an Equal Opportunity/Affirmative Action Employer.

© Motorola Inc. 2004

## HOW TO REACH US:

### USA/EUROPE/LOCATIONS NOT LISTED:

Motorola Literature Distribution  
P.O. Box 5405, Denver, Colorado 80217  
1-800-521-6274 or 480-768-2130

**JAPAN:** Motorola Japan Ltd.; SPS, Technical Information Center,  
3-20-1, Minami-Azabu, Minato-ku, Tokyo 106-8573, Japan  
81-3-3440-3569

**ASIA/PACIFIC:** Motorola Semiconductors H.K. Ltd.; Silicon Harbour Centre,  
2 Dai King Street, Tai Po Industrial Estate, Tai Po, N.T., Hong Kong  
852-2668334

**HOME PAGE:** <http://motorola.com/semiconductors>