MX·COM, INC.

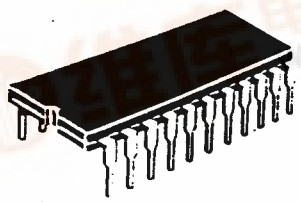
MX355
MX365

CTCSS ENCODER/DECODER

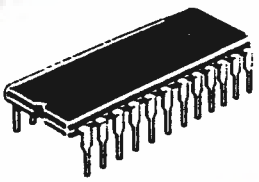
FEATURES:
- 38 CTCSS Tones + Notone
- TX/RX Audio Filters (MX365)
- TX Tone Phase Reversals
- Serial or Parallel Programming

BENEFITS:
- Scanning of any Channel
- Improved Sinad
- Squelch Tail Elimination
- Easy uP Interface

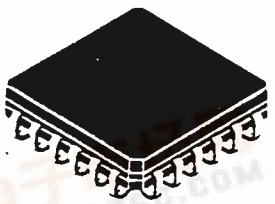
APPLICATIONS
- Mobile Radio Channel Sharing
- Wireless Intercom



MX355J (CDIP)
MX355P (PDIP)
22 pins

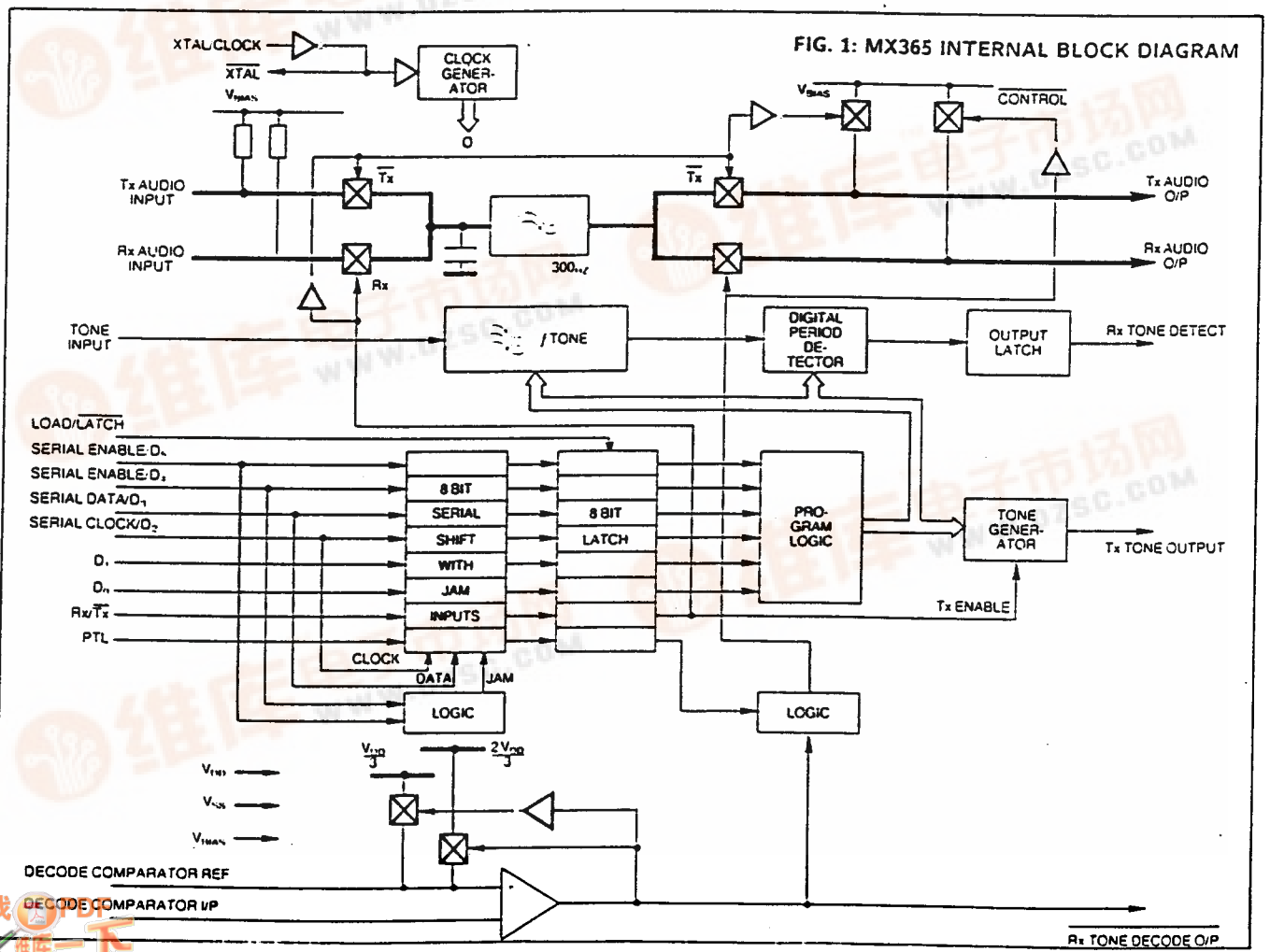


MX365J (CDIP)
MX365P (PDIP)
24 pins



MX355LH
MX365LH
(24p PLCC)

FIG. 1: MX365 INTERNAL BLOCK DIAGRAM



Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054
Doc.# 20480042.002

DESCRIPTION

Voice on shared radio channels is multiplexed with a subaudible CTCSS tone as a means of directing messages among user groups licensed on the same RF frequency. Continuous Tone Controlled Squelch Systems (CTCSS) modulate the transmitter with a discrete tone, taken from a field of 38 in the range of 67 to 250 Hz — according to EIA standard RS-220A. Groups of radio receivers, segregated by common interest and assigned tone, demodulate the voice/tone mixture for voice messages to be heard.

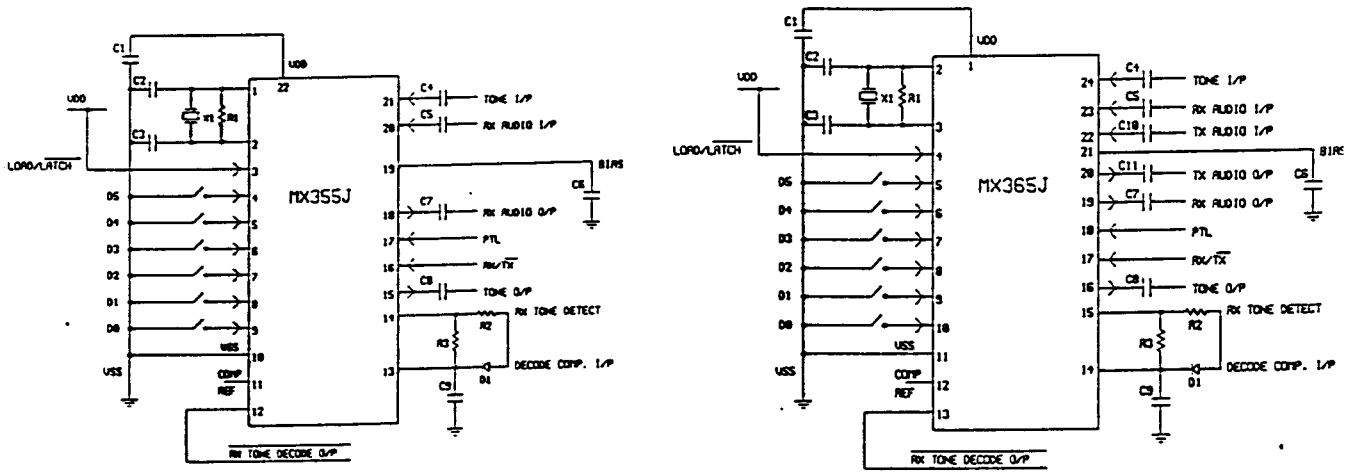
The MX365 CTCSS Encoder/Decoder enhances voice/tone multiplexing with an on-chip filter that attenuates TX speech 40dB at 250Hz, while passing signals >300Hz with only ±1dB of ripple.

Early CTCSS designs did not filter TX speech, depending instead on the host transmitter's preemphasis network. At only 6dB/octave, their attenuation of speech components at the higher CTCSS tones was only a couple of dB, inducing talk-off.

The MX365 adds serial or parallel tone and TX/RX control selection, and a new LOAD/LATCH pin. A NOTONE program code has been included to permit scanning channels without CTCSS. Operation of the PTL switch during TX reverses the phase of the transmitted CTCSS tone, used in some radios to eliminate squelch tails.

The MX365 is a CMOS integrated circuit requiring a single 5-volt supply and a 1 MHz clock or crystal. The MX355 offers a pinout similar to the earlier generation MX345.

MX355/MX365 EXTERNAL COMPONENT CONNECTIONS



COMPONENT VALUES:

R1: 1 Mohm	C1: 0.1 uF	C5: 0.1 uF	C9: 0.1 uF
R2: 560 Kohm	C2: 33 pF	C6: 0.47 uF	C10: 0.1 uF
R3: 820 Kohm	C3: 33 pF	C7: 0.1 uF	C11: 0.1 uF
X1: 1 MHz	C4: 0.1 uF	C8: 0.1 uF	D1: small signal

Tolerances:	Resistors	+/- 10%
	Capacitors	+/- 20%
	Xtal	+/- 0.1%

Figures 2 and 3: External Component Connection

Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054

MX355/365 PIN FUNCTION TABLE

PIN			FUNCTION/DESCRIPTION
MX355 J,P	MX355 LH	MX365 (all)	
22	24	1	**VDD:** Positive Supply.
1	1	2	**Xtal/Clock I/P:** Input to on chip inverter used with a 1MHz Xtal or external clock source.
2	2	3	**$\overline{\text{Xtal}}$:** Output of on chip inverter (clock output).
3	3	4	**Load/$\overline{\text{Latch}}$:** Controls 8 on chip latches and is used to latch Rx/$\overline{\text{Tx}}$, PTL, D0-D5. This pin is internally pulled to VDD. A logic '1' applied to this input puts the 8 latches in 'transparent' mode. A logic '0' applied to this input puts the 8 latches in the 'latched' mode. In parallel mode data is loaded and latched by logic 1 — 0 transition (see fig. 4). In serial mode data is loaded and latched by a 0 — 1 — 0 strobe pulse on this pin (see fig. 5).
4	4	5	**D5/Serial Enable 1:** Data input D5 (in parallel mode). A logic '1' applied to this input together with a logic '0' applied to D4/SERIAL/ENABLE 2 will put the device in 'Serial mode' (see fig. 5). This pin internally pulled to VDD.
5	5	6	**D4/Serial Enable 2:** Data input D4 (in parallel mode). A logic '0' applied to this input together with a logic '1' on pin 5 will place the device in 'serial mode' (see fig. 5). This pin internally pulled to VDD.
6	6	7	**D3/Serial Data:** Data input D3 (in parallel mode). In serial mode this pin becomes the serial data input for D5-D0, Rx/Tx, PTL (see fig. 5). D5 is clocked first and PTL last. This pin internally pulled to VDD.
7	7	8	**D2/Serial Clock:** Data D2 (in parallel mode). In serial mode this pin becomes the serial clock input. Data is clocked on the positive going edge (see fig. 5). This pin is internally pulled to VDD.
8	8	9	**D1:** Data D1 (in parallel mode). This pin internally pulled to VDD.
9	10	10	**D0:** Data D0 (in parallel mode). This pin internally pulled to VDD.
10	11	11	**VSS:** Negative supply.
11	12	12	**Decode Comparator Ref (I/P):** This pin is internally biased to VDD/3 or 2VDD/3 via 1M resistors depending on the logical state of the TONE DECODE O/P pin. TONE DEC O/P = 1 will bias this input 2VDD/3, a logic '0' will bias this input VDD/3. This input provides the decode comparator reference voltage, and switching of bias voltages provides hysterisis to reduce 'chatter' under marginal conditions.

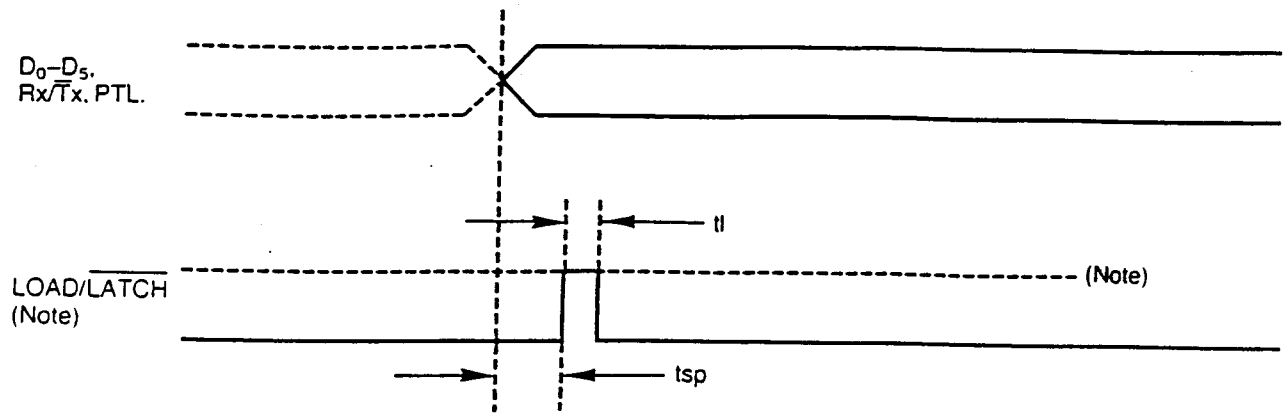
Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054

MX355/365 PIN FUNCTION TABLE (cont.)

PIN			FUNCTION/DESCRIPTION
MX355 J,P	MX355 LH	MX365 (all)	
12	13	13	**Rx Tone Decoder (O/P):** Gated output of the decode comparator. This output is used to gate the Rx Audio path. A logic '0' on this pin indicates a successful decode and that the 'decode comparator input' pin is more positive than the 'decode comparator ref' input (see table 1).
13	14	14	**Decode Comparator Input:** This is the inverting input of the decode comparator. This pin is normally connected to the integrated output of the 'rx tone detect' line.
14	16	15	**Rx Tone Detect (O/P):** In Rx mode this pin will go to logic '1' during a successful decode and must be externally integrated to control response and deresponse times (see table 1).
15	17	16	**Tx Tone O/P:** The CTCSS sinewave output appears on this pin under control of the Rx/$\overline{Tx}$ pin. This pin, when not transmitting a tone, may be biased to VDD-0.7V or O/C (see table 1). This pin is an emitter follower output with high impedance load, requiring capacitive coupling or a low impedance (<1KΩ) load to ground.
16	18	17	**Rx/$\overline{Tx}$:** This input (in parallel mode) selects Rx or Tx modes (see fig. 2). In serial mode this function is serially loaded. This pin is internally pulled to VDD via a 1M resistor.
17	19	18	**PTL:** In parallel Rx mode this pin operates as a 'press to listen' function by enabling the Rx audio path, thus overriding the tone squelch function. In parallel Tx mode this pin reverses the phase of the transmitted CTCSS tone (used for squelch tail elimination). In serial mode this function is serially loaded (see fig. 2).
18	20	19	**Rx Audio Out:** This is the high pass filtered Receive audio output pin. This pin outputs audio when Rx TONE DECODE = 0, or PTL = 1 or NOTONE is programmed (see table 2). In Tx mode this pin is biased to VDD/2.
N/A	N/A	20	**Tx Audio Out:** This is the high pass filtered Transmit audio output pin. In Tx mode this pin outputs audio present at the 'Tx AUDIO INPUT' pin. In Rx mode this pin is biased to VDD/2.
19	21	21	**Bias:** This pin is the output of an internally generated VDD/2 bias level and would normally be externally decoupled to VSS via C7.
N/A	N/A	22	**Tx Audio I/P:** This is the Tx Audio input pin. In Tx mode audio may be prefiltered, using the Tx audio path, thus helping to avoid talkoff due to intermodulation of speech frequencies with the transmitted CTCSS tone. This pin is internally biased to VDD/2.
20	22	23	**Rx Audio Input:** This is the input to the audio high pass filter in Rx mode. This pin is internally biased to VDD/2.
21	23	24	**Tone Input:** This is the input to the CTCSS tone detector and is internally biased to VDD/2.

Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054

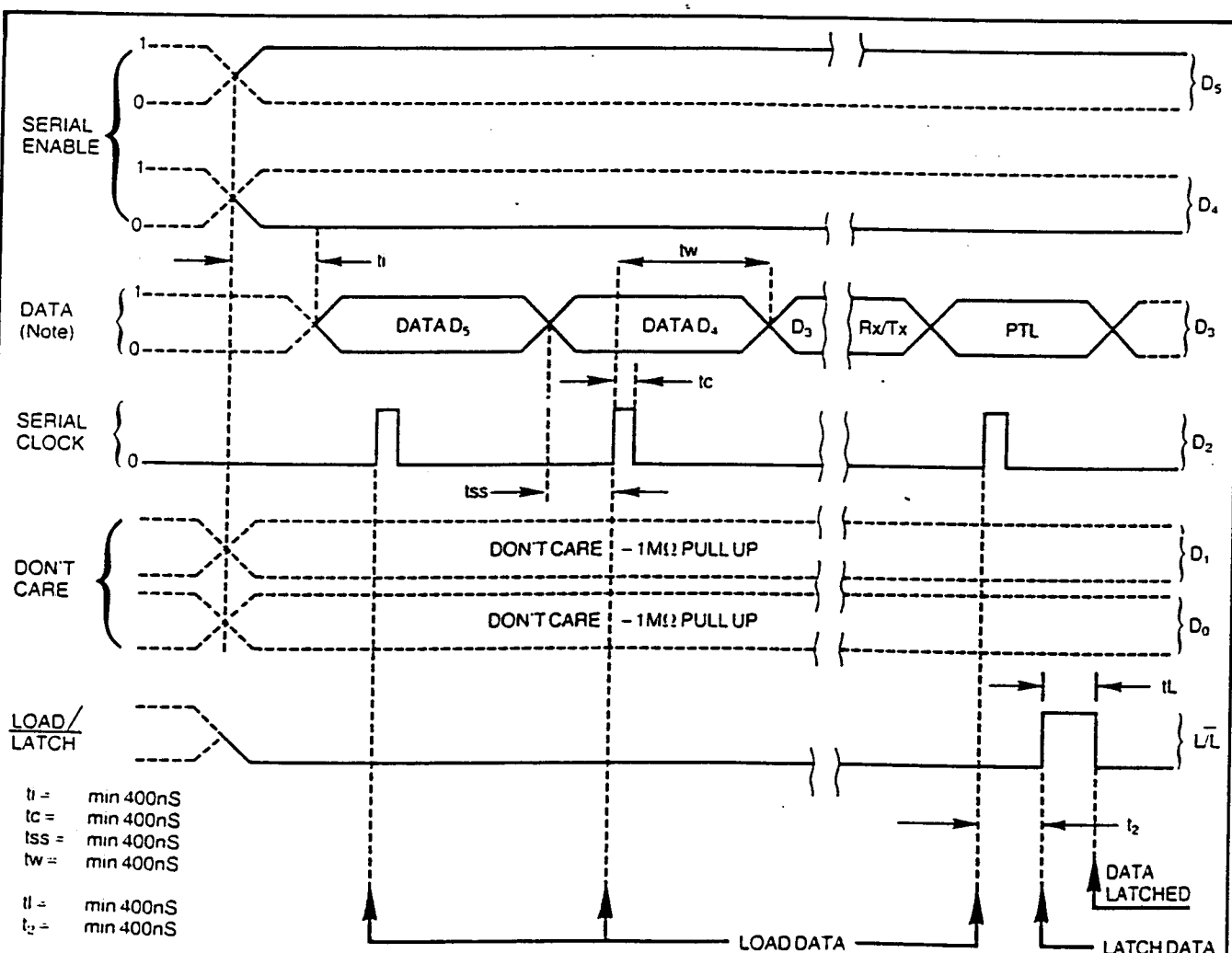
PARALLEL AND SERIAL MODE TIMING DIAGRAMS



Note: For wired, non microprocessor, applications load/latch should be connected to V_{DD}

tl min = 400ns
tsp min = 400ns

FIG. 4: PARALLEL MODE (NOT TO SCALE)



tl = min 400nS
tc = min 400nS
tss = min 400nS
tw = min 400nS

tl = min 400nS
t_2 = min 400nS

Note 1: Serial bit 1 through bit 8 = D_5, D_4, D_3, D_2, D_1, D_0, Rx/Tx and PTL respectively. Load bit 1 first, bit 8 last.

FIG. 5: SERIAL MODE (NOT TO SCALE)

Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054

Table 1 Truth table defining combinations of input/output conditions.

	Input Pin — Condition			Output Pin — Condition		Result/Function					
D_0-D_5	Rx/$\overline{Tx}$	PTL	Decode Comp Input	Rx Tone Detect	$\overline{\text{Tone Decode}}$	Tone Transmitter Enabled	Tx Tone Phase Reversed	Tx Audio Path Enabled	Tone Decoder Enabled	Rx Audio Path Enabled	Notes
Tone	0	0	x	0	1	Yes	No	Yes	No	No (bias)	1a
Tone	0	1	x	0	1	Yes	Yes	Yes	No	No (bias)	1b
No tone	0	x	x	0	1	No (bias)	x	Yes	No	No (bias)	2
Tone	1	0	0	0	1	No (o/c)	x	No	Yes	No (bias)	3a
Tone	1	1	0	0	1	No (o/c)	x	No	Yes	Yes	3b
Tone	1	x	1	1	0	No (o/c)	x	No	Yes	Yes	4
No tone	1	x	x	x	0	No (o/c)	x	No	Yes	Yes	5

Notes:

1a. Normal tone transmit condition.

1b. Tone transmit with phase reversed.

2. 'NOTONE' programmed in Tx mode, tone transmit O/P set to $V_{DD}/2 - 0.7V$. Tx audio path enabled.

3a. Normal decode standby.

3b. Normal decode standby with PTL used to enable audio.

4. Normal 'decode of correct CTCSS tone' condition, PTL has no effect.

5. 'NOTONE' programmed in Rx mode, tone transmit O/P (o/c), Rx audio path enabled.

Table 2 Tone programming Truth table

Nominal Freq. Hz	MX355/365 Frequency	Δf_o%	D_0	D_1	Program Inputs D_2	D_3	D_4	D_5
67.0	67.05	+.07	1	1	1	1	1	1
71.9	71.90	0.0	1	1	1	1	1	0
74.4	74.35	−.07	0	1	1	1	1	1
77.0	76.96	−.05	1	1	1	1	0	0
79.7	79.77	+.09	1	0	1	1	1	1
82.5	82.59	+.10	0	1	1	1	1	0
85.4	85.38	−.02	0	0	1	1	1	1
88.5	88.61	+.13	0	1	1	1	0	0
91.5	91.58	+.09	1	1	0	1	1	1
94.8	94.76	−.04	1	0	1	1	1	0
97.4	97.29	−0.11	0	1	0	1	1	1
100.0	99.96	−.04	1	0	1	1	0	0
103.5	103.43	−.07	0	0	1	1	1	0
107.2	107.15	−.05	0	0	1	1	0	0
110.9	110.77	−.12	1	1	0	1	1	0
114.8	114.64	−.14	1	1	0	1	0	0
118.8	118.80	0.0	0	1	0	1	1	0
123.0	122.80	−.17	0	1	0	1	0	0
127.3	127.08	−.17	1	0	0	1	1	0
131.8	131.67	−.10	1	0	0	1	0	0
136.5	136.61	+.08	0	0	0	1	1	0
141.3	141.32	+.02	0	0	0	1	0	0
146.2	146.37	+.12	1	1	1	0	1	0
151.4	151.09	−.20	1	1	1	0	0	0
156.7	156.88	+.11	0	1	1	0	1	0
162.2	162.31	+.07	0	1	1	0	0	0
167.9	168.14	+.14	1	0	1	0	1	0
173.8	173.48	−.19	1	0	1	0	0	0
179.9	180.15	+.14	0	0	1	0	1	0
186.2	186.29	+.05	0	0	1	0	0	0
192.8	192.86	+.03	1	1	0	0	1	0
203.5	203.65	+.07	1	1	0	0	0	0
210.7	210.17	−.25	0	1	0	0	1	0
218.1	218.58	+.22	0	1	0	0	0	0
225.7	226.12	+.18	1	0	0	0	1	0
233.6	234.19	+.25	1	0	0	0	0	0
241.8	241.08	−.30	0	0	0	0	1	0
250.3	250.28	−.01	0	0	0	0	0	0
Notone	Notone	—	0	0	0	0	1	1
Serial Input Mode			x	x	Clock	Data	0	1

Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054

MX355/365 ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings

Exceeding the maximum rating can result in device damage. Operation of the device outside the operating limits is not implied.

Supply voltage		−0.3V to 7.0V
Input voltage at any pin (ref V_{SS} = OV)		−0.3V to (V_{DD} + 0.3V)
Output sink/source current (total)		20mA
Operating temperature range:	MX365J, MX355J	−30°C to +85°C
	MX365P/LH, MX355P/LH	−30°C to +70°C
Storage temperature range:	MX365J/MX355J	−55°C to +125°C
	MX365P/LH, MX355P/LH	−40°C to +85°C
Maximum device dissipation		100mW

Operating Limits

V_{DD} = 5V, T_{amb} = +25°C, 0dB ref = 300mVrms, Composite signal = 0dB 1kHz tone, −12dB noise (band limited 6kHz gaussian white noise), −20dBf_o CTCSS tone.

Characteristic	See note	Min	Typ	Max	Unit
Static Characteristics					
Supply volts		4.5	5.0	5.5	V
Supply current (Tx)			3.5	—	mA
Supply current (Rx)			3.5	—	mA
Tone input impedance			1	—	MΩ
Audio input impedance			1	—	MΩ
Audio output impedance			1	—	kΩ
Digital input impedance	1	—	1	—	MΩ
Input logic '1'	1	70% V_{DD}	—	—	V
Input logic '0'	1	—	—	30% V_{DD}	V
Logic '1' output 1' source = 0.1mA	2	80% V_{DD}	—	—	V
Logic '0' output 1' sink − 0.1mA	2	—	—	20% V_{DD}	V
Dynamic Characteristics					
Decoder					
Decode input signal level	3	−20	—	—	dB
Decode response time	3,6,8	—	—	250	ms
Deresponse time	3,6,8	—	180	250	ms
Decode selectivity	3	±0.5	—	±3	%f_o
Encoder					
Tone output level (relative 775mVrms)		−3	0	—	dB
Tone frequency accuracy (f_o error)		−0.3		+0.3	%f_o
Risetime to 90% nominal o/p:					
f_o>100Hz	4	—	15	—	ms
f_o<100Hz	4	—	45	—	ms
Tone output load current		—	—	5	mA
Total harmonic distortion		—	2	5	%
Output level variation between tones		—	0.1	—	dB
Audio Filter					
Total harmonic distortion	5	—	2	5	%
Output noise level (input a.c. short circuit, audio switch enabled)		—	−60	−50	dB

Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054

Characteristics	See Note	Min	Typ	Max	Unit
Audio Filter					
Cutoff frequency		—	300	—	Hz
Bandpass ripple (300 — 3000 Hz)	5	−1	—	+1	dB
Stopband attenuation <250 Hz	5	36	40	—	dB
Passband gain 1kHz		—	0	—	dB
Audio Switch					
Isolation	5	—	60	—	dB
Serial Parallel Inputs					
Parallel set up time tsp	7	400	—	—	ns
Load/Latch pulse width tl	7	400	—	—	ns
Serial Clock pulse width tc	7	400	—	—	ns
Serial set up time tss	7	400	—	—	ns
Serial Clock frequency	7	—	1	—	MHz

Notes

1. *Refers to Rx/Tx, PTL, Decode Comparator Input, D_0, D_1, D_2, D_3, D_4, D_5.*
2. *All logic outputs.*
3. *Composite Signal Test Condition.*
4. *Any programme tone and RL = 600, CL = 15pF. Includes response to a phase reversal instruction.*
5. *1kHz References = 0dB.*
6. *f_o>100Hz, (for 100Hz>f_o>67Hz:*

$$t = \frac{100}{f_o Hz} \times 250ms)$$

7. *See Figs. 6 & 7.*
8. *See Fig. 4.*

Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054

CML Microcircuits
COMMUNICATION SEMICONDUCTORS

CML Product Data

In the process of creating a more global image, the three standard product semiconductor companies of CML Microsystems Plc *(Consumer Microcircuits Limited (UK), MX-COM, Inc (USA) and CML Microcircuits (Singapore) Pte Ltd)* have undergone name changes and, whilst maintaining their separate new names *(CML Microcircuits (UK) Ltd, CML Microcircuits (USA) Inc and CML Microcircuits (Singapore) Pte Ltd*), now operate under the single title **CML Microcircuits**.
These companies are all 100% owned operating companies of the CML Microsystems Plc Group and these changes are purely changes of name and do not change any underlying legal entities and hence will have no effect on any agreements or contacts currently in force.

CML Microcircuits Product Prefix Codes

Until the latter part of 1996, the differentiator between products manufactured and sold from MXCOM, Inc. and Consumer Microcircuits Limited were denoted by the prefixes MX and FX respectively. These products use the same silicon etc. and today still carry the same prefixes. In the latter part of 1996, both companies adopted the common prefix: CMX.

This notification is relevant product information to which it is attached.

CML Microcircuits (USA) [formerly MX-COM, Inc.] Product Textual Marking

On CML Microcircuits (USA) products, the **'MX-COM'** textual logo is being replaced by a **'CML'** textual logo.

Company contact information is as below:

CML Microcircuits (UK) Ltd
COMMUNICATION SEMICONDUCTORS

Oval Park, Langford, Maldon,
Essex, CM9 6WG, England
Tel: +44 (0)1621 875500
Fax: +44 (0)1621 875600
uk.sales@cmlmicro.com
www.cmlmicro.com

CML Microcircuits (USA) Inc.
COMMUNICATION SEMICONDUCTORS

4800 Bethania Station Road,
Winston-Salem, NC 27105, USA
Tel: +1 336 744 5050,
0800 638 5577
Fax: +1 336 744 5054
us.sales@cmlmicro.com
www.cmlmicro.com

CML Microcircuits (Singapore) Pte Ltd
COMMUNICATION SEMICONDUCTORS

No 2 Kallang Pudding Road, 09-05/
06 Mactech Industrial Building,
Singapore 349307
Tel: +65 7450426
Fax: +65 7452917
sg.sales@cmlmicro.com
www.cmlmicro.com