
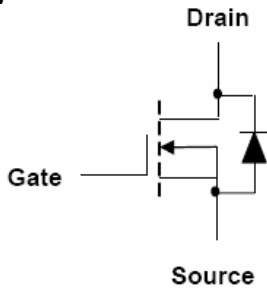
	<h1 style="margin: 0;">TSM35N03</h1> <h2 style="margin: 0;">N-Channel Enhancement Mode MOSFET</h2>	<p style="font-size: 1.2em; margin: 0;">Preliminary</p>
<p>TO-252</p> 	<p>Pin assignment:</p> <ol style="list-style-type: none"> 1. Gate 2. Drain 3. Source 	<p>$V_{DS} = 30V$</p> <p>$I_D = 50A$</p> <p>$R_{DS(on)}, V_{GS} @ 10V, I_{DS} @ 30A = 8.5m\Omega$</p> <p>$R_{DS(on)}, V_{GS} @ 4.5V, I_{DS} @ 30A = 13m\Omega$</p>

Features

- ✧ Advanced trench process technology
- ✧ High Density Cell Design for Ultra Low On-Resistance
- ✧ Fully Characterized Avalanche Voltage and Current
- ✧ Specially Designed for DC/DC Converters and Motor Drivers

Block Diagram



Ordering Information

Part No.	Packing	Package
TSM35N03CP	Tape & Reel	TO-252

Absolute Maximum Rating ($T_A = 25^\circ C$ unless otherwise noted)

Parameter	Symbol	Limit	Unit	
Drain-Source Voltage	V_{DS}	30	V	
Gate-Source Voltage	V_{GS}	± 20	V	
Continuous Drain Current	I_D	50	A	
Pulsed Drain Current	I_{DM}	350		
Maximum Power Dissipation	P_D	$T_A = 25^\circ C$	57	W
		$T_A = 100^\circ C$	23	$W/^\circ C$
Operating Junction Temperature	T_J	+150	$^\circ C$	
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 to +150	$^\circ C$	
Single Pulse Drain to Source Avalanche Energy ($V_{DD} = 100V, V_{GS} = 10V, I_{AS} = 2A, L = 10mH, R_G = 25\Omega$)	E_{AS}	300	mJ	

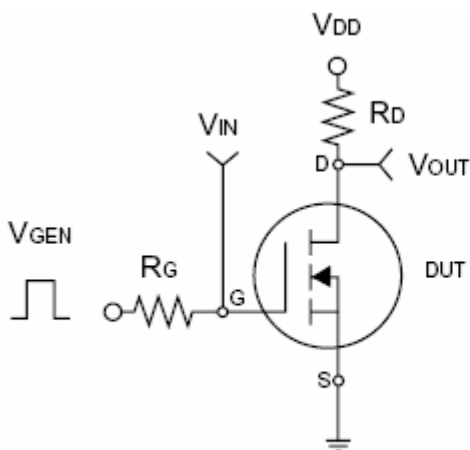
Thermal Performance

Parameter	Symbol	Limit	Unit
Lead Temperature (1/8" from case)	T_L	10	S
Junction-to-case Thermal Resistance	$R_{\theta jc}$	2.2	$^\circ C/W$
Junction to Ambient Thermal Resistance (PCB mounted)	$R_{\theta ja}$	50	

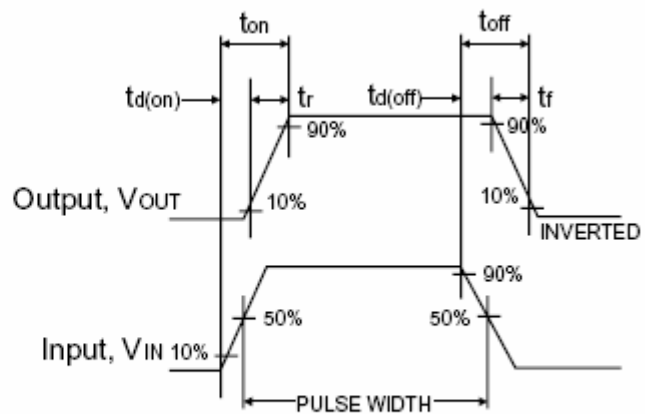
Note: 1. Maximum DC current limited by the package
 2. 1-in² 2oz Cu PCB board

Electrical Characteristics						
$T_J = 25^\circ\text{C}$, unless otherwise noted						
Parameter	Conditions	Symbol	Min	Typ	Max	Unit
Static						
Drain-Source Breakdown Voltage	$V_{GS} = 0\text{V}, I_D = 250\mu\text{A}$	BV_{DSS}	30	--	--	V
Drain-Source On-State Resistance	$V_{GS} = 4.5\text{V}, I_D = 30\text{A}$	$R_{DS(ON)}$	--	10.0	13.0	$\text{m}\Omega$
Drain-Source On-State Resistance	$V_{GS} = 10\text{V}, I_D = 30\text{A}$	$R_{DS(ON)}$	--	6.5	8.5	$\text{m}\Omega$
Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\mu\text{A}$	$V_{GS(TH)}$	1.0	1.6	3.0	V
Zero Gate Voltage Drain Current	$V_{DS} = 24\text{V}, V_{GS} = 0\text{V}$	I_{DSS}	--	--	1.0	μA
Gate Body Leakage	$V_{GS} = \pm 20\text{V}, V_{DS} = 0\text{V}$	I_{GSS}	--	--	± 100	nA
Gate Resistance		R_g	--	--	--	
Forward Transconductance	$V_{DS} = 10\text{V}, I_D = 35\text{A}$	g_{fs}	--	--	--	S
Dynamic						
Total Gate Charge	$V_{DS} = 15\text{V}, I_D = 35\text{A},$ $V_{GS} = 10\text{V}$	Q_g	--	24	--	nC
Gate-Source Charge		Q_{gs}	--	5.4	--	
Gate-Drain Charge		Q_{gd}	--	4.0	--	
Turn-On Delay Time	$V_{DD} = 15\text{V}, R_L = 15\Omega,$ $I_D = 1\text{A}, V_{GEN} = 10\text{V},$ $R_G = 24\Omega$	$t_{d(on)}$	--	15	--	nS
Turn-On Rise Time		t_r	--	3.2	--	
Turn-Off Delay Time		$t_{d(off)}$	--	36	--	
Turn-Off Fall Time		t_f	--	4.8	--	
Input Capacitance	$V_{DS} = 15\text{V}, V_{GS} = 0\text{V},$ $f = 1.0\text{MHz}$	C_{iss}	--	1940	--	pF
Output Capacitance		C_{oss}	--	312	--	
Reverse Transfer Capacitance		C_{rss}	--	122	--	
Source-Drain Diode						
Max. Diode Forward Current		I_S	--	--	50	A
Diode Forward Voltage	$I_S = 20\text{A}, V_{GS} = 0\text{V}$	V_{SD}	--	0.87	1.5	V

Note: 1. pulse test: pulse width $\leq 300\mu\text{s}$, duty cycle $\leq 2\%$
 2. Negligible, Dominated by circuit inductance.

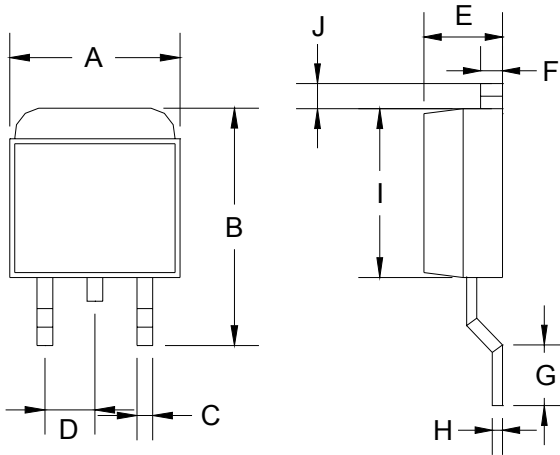


Switching Test Circuit



Switchin Waveforms

TO-252 Mechanical Drawing



TO-252 DIMENSION				
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	6.570	6.840	0.259	0.269
B	9.250	10.400	0.364	0.409
C	0.550	0.700	0.022	0.028
D	2.560	2.670	0.101	0.105
E	2.300	2.390	0.090	0.094
F	0.490	0.570	0.019	0.022
G	1.460	1.580	0.057	0.062
H	0.520	0.570	0.020	0.022
I	5.340	5.550	0.210	0.219
J	1.460	1.640	0.057	0.065

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