

## 2N3957, 2N3958

### N-Channel Dual Silicon Junction Field-Effect Transistor

- Low and Medium Frequency Differential Amplifiers
- High Input Impedance Amplifiers

#### Absolute maximum ratings at $T_A = 25^\circ\text{C}$

Reverse Gate Source & Reverse Gate Drain Voltage	- 50 V
Gate Current	50 mA
Total Device Power Dissipation (each side) @ 85°C Case Temperature (both sides)	250 mW 500 mW
Power Derating (both sides)	4.3 mW/°C

At 25°C free air temperature:

#### Static Electrical Characteristics

		2N3957		2N3958		Unit	Process NJ16	
		Min	Max	Min	Max		Test Conditions	
Gate Source Breakdown Voltage	$V_{(BR)GSS}$	- 50		- 50		V	$I_G = - 1 \mu\text{A}, V_{DS} = \emptyset\text{V}$	
Gate Reverse Current	$I_{GSS}$		- 100		- 100	pA	$V_{GS} = - 30\text{V}, V_{DS} = \emptyset\text{V}$	
			- 500		- 500	nA	$V_{GS} = - 30\text{V}, V_{DS} = \emptyset\text{V}$ $T_A = 125^\circ\text{C}$	
Gate Operating Current	$I_G$		- 50		- 50	pA	$V_{DS} = 20\text{V}, I_D = 200 \mu\text{A}$	
			- 250		- 250	nA	$V_{DS} = 20\text{V}, I_D = 200 \mu\text{A}$ $T_A = 125^\circ\text{C}$	
Gate Source Voltage	$V_{GS}$		- 4.2		- 4.2	V	$V_{DS} = 20\text{V}, I_D = 50 \mu\text{A}$	
		- 0.5	- 4	- 0.5	- 4	V	$V_{DS} = 20\text{V}, I_D = 200 \mu\text{A}$	
Gate Source Cutoff Voltage	$V_{GS(OFF)}$	- 1	- 4.5	- 1	- 4.5	V	$V_{DS} = 20\text{V}, I_D = 1 \text{nA}$	
Gate Source Forward Voltage	$V_{GS(F)}$		2		2	V	$V_{DS} = \emptyset, I_G = 1 \text{mA}$	
Drain Saturation Current (Pulsed)	$I_{DSS}$	0.5	5	0.5	5	mA	$V_{DS} = 20\text{V}, V_{GS} = \emptyset\text{V}$	

#### Dynamic Electrical Characteristics

Common Source Forward Transconductance	$g_{fs}$	1000	3000	1000	3000	$\mu\text{S}$	$V_{DS} = 20\text{V}, V_{GS} = \emptyset\text{V}$	$f = 1 \text{kHz}$
		1000		1000		$\mu\text{S}$	$V_{DS} = 20\text{V}, V_{GS} = \emptyset\text{V}$	$f = 200 \text{MHz}$
Common Source Output Conductance	$g_{os}$		35		35	$\mu\text{S}$	$V_{DS} = 20\text{V}, V_{GS} = \emptyset\text{V}$	$f = 1 \text{kHz}$
Common Source Input Capacitance	$C_{iss}$		4		4	pF	$V_{DS} = 20\text{V}, V_{GS} = \emptyset\text{V}$	$f = 1 \text{MHz}$
Drain Gate Capacitance	$C_{dgo}$		1.5		1.5	pF	$V_{DS} = 10\text{V}, I_S = \emptyset\text{A}$	$f = 1 \text{MHz}$
Common Source Reverse Transfer Capacitance	$C_{rss}$		1.2		1.2	pF	$V_{DS} = 20\text{V}, V_{GS} = \emptyset\text{V}$	$f = 1 \text{MHz}$
Noise Figure	NF		0.5		0.5	dB	$V_{DS} = 20\text{V}, V_{GS} = \emptyset\text{V}$ $R_G = 10\text{M}\Omega$	$f = 100 \text{Hz}$
Differential Gate Current	$ I_{G1} - I_{G2} $		10		10	nA	$V_{DS} = 20\text{V}, I_D = 200 \mu\text{A}$	$T_A = 125^\circ\text{C}$
Saturation Drain Current Ratio	$I_{DSS1} / I_{DSS2}$	0.9	1	0.85	1		$V_{DS} = 20\text{V}, V_{GS} = \emptyset\text{V}$	
Differential Gate Source Voltage	$ V_{GS1} - V_{GS2} $		20		25	mV	$V_{DS} = 20\text{V}, I_D = 200 \mu\text{A}$	
Differential Gate Source Voltage with Temperature	$\frac{\Delta V_{GS1} - V_{GS2}}{\Delta T}$		6		8	mV	$V_{DS} = 20\text{V}, I_D = 200 \mu\text{A}$	$T_A = 25^\circ\text{C}$ to $- 55^\circ\text{C}$
			7.5		10	mV	$V_{DS} = 20\text{V}, I_D = 200 \mu\text{A}$	$T_A = 25^\circ\text{C}$ to $125^\circ\text{C}$
Transconductance Ratio	$g_{fs1} / g_{fs2}$	0.9	1	0.85	1		$V_{DS} = 20\text{V}, I_D = 200 \mu\text{A}$	$f = 1 \text{kHz}$

 **InterFET Corporation**  
1000 N. Shiloh Road, Garland, TX 75042  
(972) 487-1287 FAX (972) 276-3375

**TO-71 Package**  
See Section G for Outline Dimensions

**Pin Configuration**  
1 Source, 2 Drain, 3 Gate, 5 Source,  
6 Drain, 7 Gate

[www.interfet.com](http://www.interfet.com)

WWW.ALLDATASHEET.COM

Copyright © Each Manufacturing Company.

All Datasheets cannot be modified without permission.

This datasheet has been download from :

[www.AllDataSheet.com](http://www.AllDataSheet.com)

100% Free DataSheet Search Site.

Free Download.

No Register.

Fast Search System.

[www.AllDataSheet.com](http://www.AllDataSheet.com)