查询SN65508供应商

ADVANCE INFORMATION

SN65508, SN75508
AC PLASMA DISPLAY DRIVERS

D2924, DECEMBER 1985—REVISED OCTOBER 1986

- Controls 32 Electrodes
- Very Low Steady-State Power Consumption
- Rugged DMOS Outputs
- CMOS-Compatible Inputs
- Dependable Texas Instruments Quality and Reliability

description

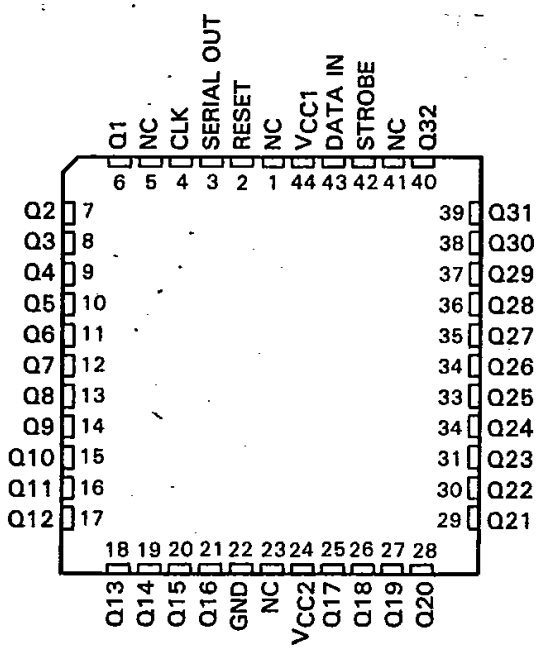
The SN65508 and SN75508 are monolithic BIDFET† integrated circuits designed to provide the serial-to-parallel conversion and level translation of data in a matrix-addressable display. All inputs are CMOS compatible and all outputs are totem-pole DMOS structures.

If the strobe input is at a high logic level, all outputs are high. When the strobe input goes low, any output whose associated register bit contains a low will go low. All outputs whose associated register bit contains a high will remain high. When the reset input is low, all register bits are low. In this condition, all outputs will go low when the strobe input goes low. The serial data output from the shift register may be used to cascade additional devices. This output is not affected by the Strobe input.

The SN65508 is characterized for operation from −40°C to 85°C. The SN75508 is characterized for operation from 0°C to 70°C.

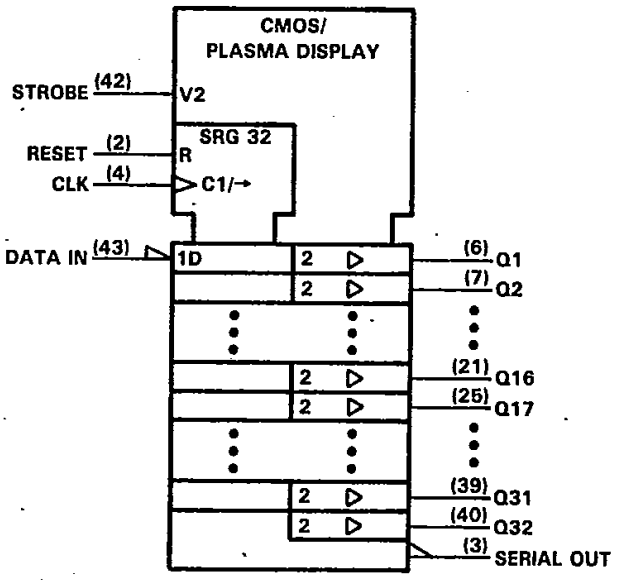
FN PACKAGE
(TOP VIEW)

T-52-13-09



NC—No internal connection

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1094 and IEC Publication 617-12.

†BIDFET—Bipolar, double-diffused, N-channel and P-channel MOS transistors on same chip — patented process

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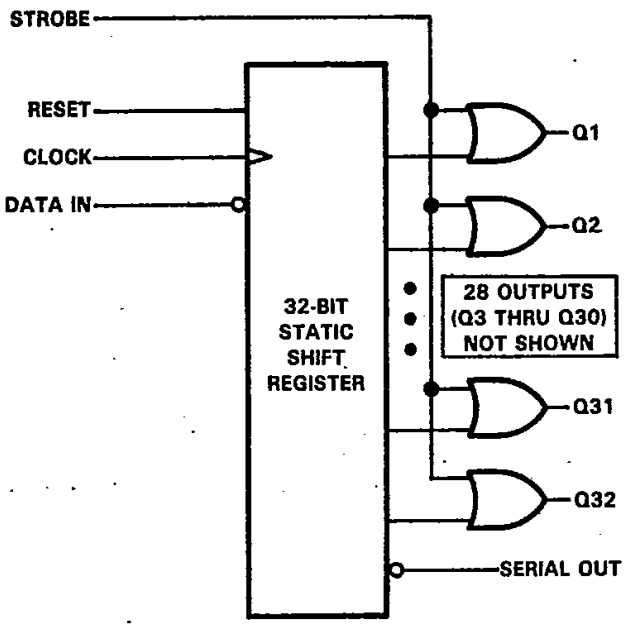
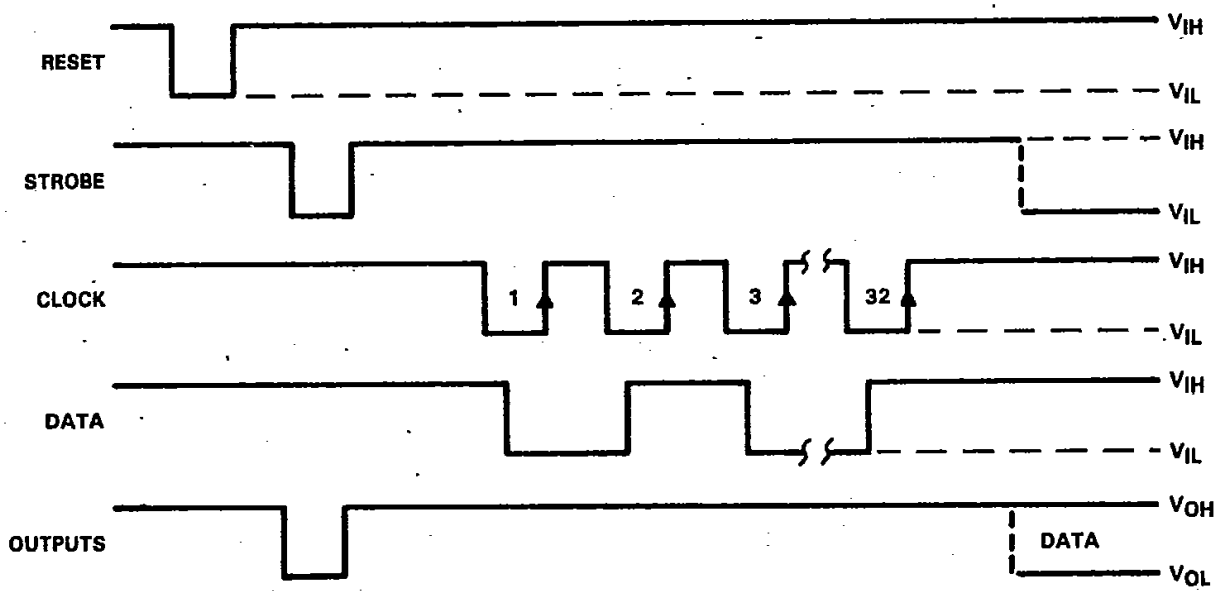
functional block diagram



typical operating sequence



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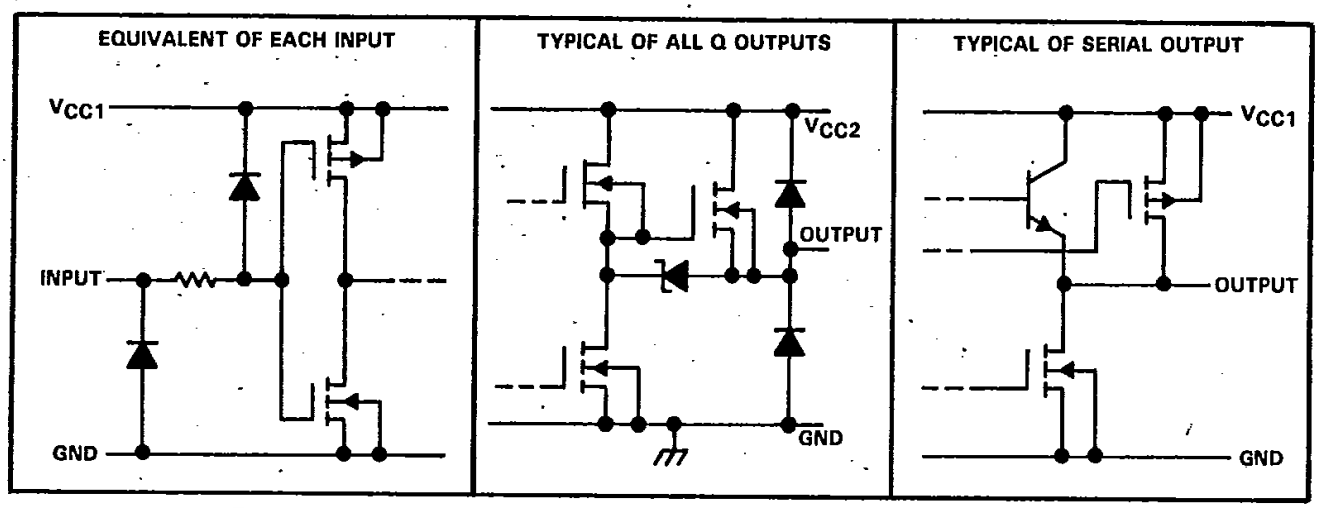
schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC1} (see Note 1)	15 V
Supply voltage, V_{CC2}	95 V
Input voltage, V_I	−0.3 V to V_{CC} + 0.3 V
High-level output voltage, V_{OH}	95 V
High-level output current, I_{OH}	−3 mA
Continuous total power dissipation at (or below) 25°C free-air temperature (see Note 2)	1700 mW
Operating free-air temperature range: SN65508	−40°C to 85°C
SN75508	0°C to 70°C
Storage temperature range	−65°C to 150°C
Case temperature for 10 seconds	260°C

NOTES: 1. Voltage values are with respect to network ground terminal.
2. For operation above 25°C free-air temperature, derate linearly to 1088 mW at 70°C at the rate of 13.6 mW/°C.

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recommended operating conditions

		MIN	MAX	UNIT
Supply voltage, V_{CC1}		7.65	9.35	V
Supply voltage, V_{CC2}		V_{CC1}	90	V
High-level input voltage, V_{IH}	V_{CC1} = 9.35 V	7	V_{CC1}	V
	V_{CC1} = 7.65 V	5.75	V_{CC1}	
Low-level input voltage, V_{IL}	V_{CC1} = 9.35 V	0	2.3	V
	V_{CC1} = 7.65 V	0	1.9	
Output current, I_O ($t_W \leq 1\ \mu s$)			80	mA
Clock frequency, f_{clock}			4	MHz
Setup time, data before clock↓, t_{su}		100		ns
Hold time, data after clock↓, t_h		62		ns
Pulse duration, clock high or low, t_{wCLK}		125		ns
Operating free-air temperature, T_A	SN65508	−40	85	°C
	SN75508	0	70	

electrical characteristics over recommended operating free-air temperature range, V_{CC1} = 9.35 V, V_{CC2} = 90 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	MAX	UNIT
V_{OH}	High-level output voltage	Q outputs	V_{CC1} = 7.65 V,	I_{OH} = −3 mA	83	87	V
		Serial output	V_{CC1} = 7.65 V,	I_{OH} = −50 μA	6.8	7.65	
V_{OL}	Low-level output voltage	Q outputs	V_{CC1} = 7.65 V,	I_{OL} = 10 mA	1.4	2.4	V
		Serial output	V_{CC1} = 7.65 V,	I_{OL} = 50 μA	0	0.8	
V_{OK}	Output clamp voltage		V_{CC2} = 0	I_O = 100 mA, $t_W \leq 1\ \mu s$		2.5	V
				I_O = −100 mA, $t_W \leq 1\ \mu s$		−2.7	
I_{IH}	High-level input current		V_I = 9.35 V			1	μA
I_{IL}	Low-level input current		V_I = 0.4 V			−1	μA
I_{OS}	Short-circuit output current		V_O = 0			−20	mA
I_{CC1}	Supply current from V_{CC1}					500	μA
I_{CC2}	Supply current from V_{CC2}		Output high			500	μA
			Output low			8.5	mA

switching characteristics, V_{CC1} = 7.65 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
t_{wRSTL}	Pulse duration, reset low		125		ns
t_{d1}	Delay time, V_{CC2} to Q outputs (10%−10%)	R_L = 100 kΩ, C_L = 100 pF		800	ns
t_{d2}	Delay time, V_{CC2} to Q outputs (90%−90%)	R_L = 100 kΩ, C_L = 100 pF		800	ns

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PARAMETER MEASUREMENT INFORMATION

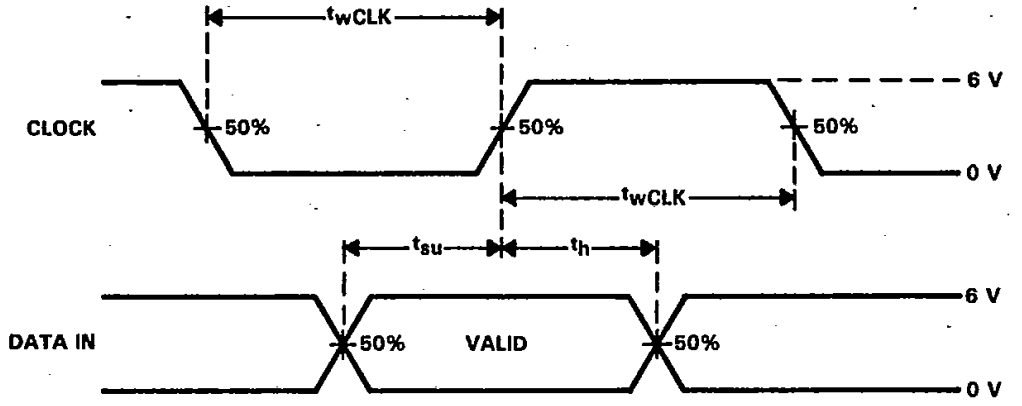

FIGURE 1. INPUT TIMING VOLTAGE WAVEFORMS

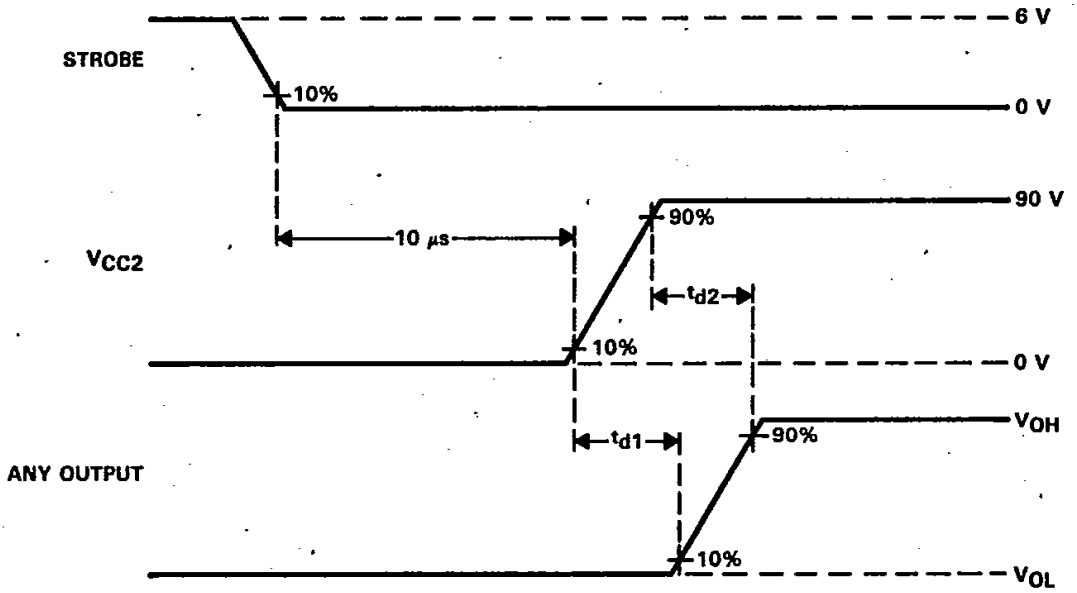

FIGURE 2. VOLTAGE WAVEFORMS FOR OUTPUT DELAY TIMES

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