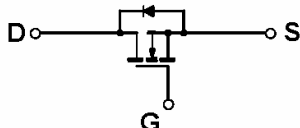


TSC 		TSM2N7002 60V N-Channel Enhancement Mode MOSFET																																						
SOT-23 		Pin assignment: 1. Gate 2. Source 3. Drain	$V_{DS} = 60V$ $R_{DS\ (on)}, V_{GS}\ @\ 10V, I_{ds}\ @\ 500mA = 7.5\Omega$ $R_{DS\ (on)}, V_{GS}\ @\ 5V, I_{ds}\ @\ 50mA = 13.5\Omega$																																					
Features ✧ Advanced trench process technology ✧ High density cell design for low on-resistance ✧ High input impedance ✧ High speed switching ✧ No minority carrier storage time ✧ CMOS logic compatible input ✧ No secondary breakdown ✧ Compact and low profile SOT-23 package																																								
Block Diagram 		Ordering Information <table><tr><th>Part No.</th><th>Packing</th><th>Package</th></tr><tr><td>TSM2N7002CX</td><td>Tape & Reel</td><td>SOT-23</td></tr></table>		Part No.	Packing	Package	TSM2N7002CX	Tape & Reel	SOT-23																															
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Absolute Maximum Rating (Ta = 25°C unless otherwise noted) <table><tr><th>Parameter</th><th>Symbol</th><th>Limit</th><th>Unit</th></tr><tr><td>Drain-Source Voltage</td><td>V_{DS}</td><td>60</td><td>V</td></tr><tr><td>Gate-Source Voltage</td><td>V_{GS}</td><td>± 20</td><td>V</td></tr><tr><td>Continuous Drain Current</td><td>I_D</td><td>115</td><td>mA</td></tr><tr><td>Pulsed Drain Current</td><td>I_{DM}</td><td>800</td><td>mA</td></tr><tr><td rowspan="2">Maximum Power Dissipation</td><td>Ta = 25 °C</td><td>P_D</td><td>225</td><td>mW</td></tr><tr><td>Ta > 25 °C</td><td></td><td>1.8</td><td>MW/°C</td></tr><tr><td>Operating Junction Temperature</td><td>T_J</td><td>+150</td><td>°C</td></tr><tr><td>Operating Junction and Storage Temperature Range</td><td>T_J, T_{STG}</td><td>- 55 to +150</td><td>°C</td></tr></table>				Parameter	Symbol	Limit	Unit	Drain-Source Voltage	V_{DS}	60	V	Gate-Source Voltage	V_{GS}	± 20	V	Continuous Drain Current	I_D	115	mA	Pulsed Drain Current	I_{DM}	800	mA	Maximum Power Dissipation	Ta = 25 °C	P_D	225	mW	Ta > 25 °C		1.8	MW/°C	Operating Junction Temperature	T_J	+150	°C	Operating Junction and Storage Temperature Range	T_J, T_{STG}	- 55 to +150	°C
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Note: Surface mounted on FR4 board $t \leq 5\text{sec}$.

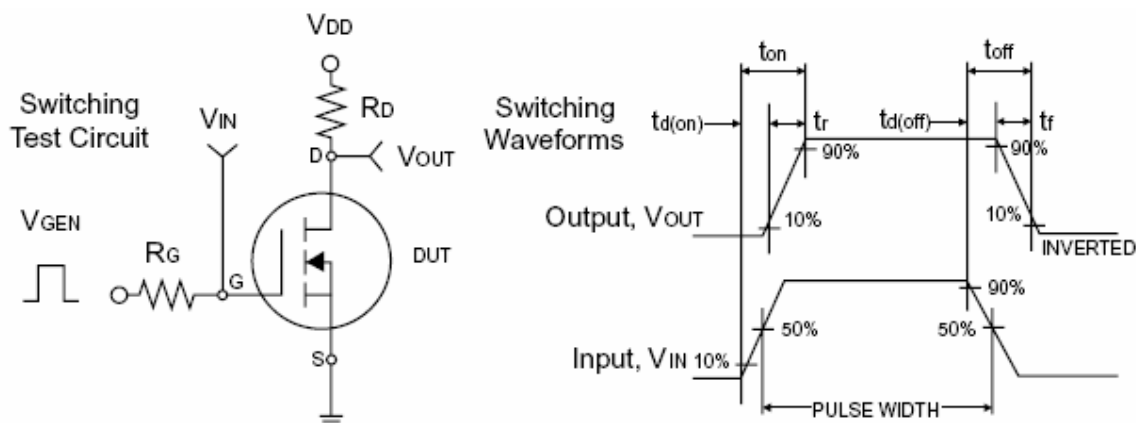


Electrical Characteristics

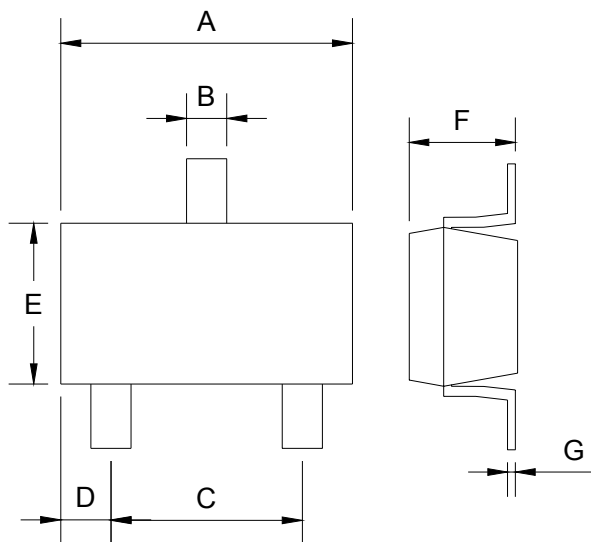
T_j = 25 °C unless otherwise noted

Parameter	Conditions	Symbol	Min	Typ	Max	Unit
Static						
Drain-Source Breakdown Voltage	$V_{GS} = 0V, I_D = 10\mu A$	BV_{DSS}	60	--	--	V
Drain-Source On-State Resistance	$V_{GS} = 10V, I_D = 500mA$	$R_{DS(ON)}$	--	--	7.5	Ω
Drain-Source On-State Resistance	$V_{GS} = 5V, I_D = 50mA$	$R_{DS(ON)}$	--	--	13.5	
Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\mu A$	$V_{GS(TH)}$	1.0	--	2.5	V
Zero Gate Voltage Drain Current	$V_{DS} = 60V, V_{GS} = 0V$	I_{DSS}	--	--	1.0	μA
Gate Body Leakage	$V_{GS} = \pm 20V, V_{DS} = 0V$	I_{GSS}	--	--	± 100	nA
On-State Drain Current	$V_{DS} \square 2V, V_{GS} = 10V$	$I_{D(ON)}$	500	--	--	mA
Dynamic						
Turn-On Rise Time	$V_{DD} = 25V, R_L = 50\Omega,$ $I_D = 500mA, V_{GEN} = 10V,$ $R_G = 25\Omega$	t_r	--	--	20	nS
Turn-Off Fall Time		t_f	--	--	40	
Input Capacitance	$V_{DS} = 25V, V_{GS} = 0V,$ $f = 1.0MHz$	C_{iss}	--	50	--	pF
Output Capacitance		C_{oss}	--	25	--	
Reverse Transfer Capacitance		C_{rss}	--	5	--	
Source-Drain Diode						
Max. Diode Forward Current		I_S	--	--	115	mA
Diode Forward Voltage	$I_S = 115mA, V_{GS} = 0V$	V_{SD}	--	1.3	1.5	V

Note : pulse test: pulse width ≤ 300uS, duty cycle ≤ 2%



SOT-23 Mechanical Drawing



SOT-23 DIMENSION				
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	2.88	2.91	0.113	0.115
B	0.39	0.42	0.015	0.017
C	1.78	2.03	0.070	0.080
D	0.51	0.61	0.020	0.024
E	1.50	1.70	0.061	0.069
F	1.04	1.08	0.041	0.043
G	0.07	0.09	0.003	0.004

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