# DATA SHEET

## 74F258A

Quad 2-line to 1-line selector/multiplexer, inverting (3-State)

Product specification

1996 Jan 05

IC15 Data Handbook





## **Quad 2-line to 1-line selector/multiplexer, inverting** (3-State)

74F258A

#### **FEATURES**

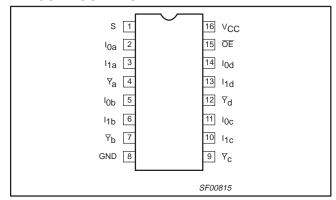
- Multifunction capability
- Non-inverting data path
- 3-State outputs
- See 74F257A for non-inverting version

#### **DESCRIPTION**

The 74F258A has four identical 2-input multiplexers with 3-State outputs which select 4 bits of data from two sources under control of a common Select (S) input. The  $I_{0n}$  inputs are selected when the Select input is Low and the  $I_{1n}$  inputs are selected when the Select input is High. Data appears at the outputs in inverted form.

The 74F258A is the logical implementation of a 4-pole, 2-position switch where the position of the switch is determined by the logic level supplied to the Select input. Outputs are forced to a High impedance "off" state when the Output Enable input  $(\overline{OE})$  is High. All but one device must be in the High impedance state to avoid currents that would exceed the maximum ratings if outputs are tied together. Design of the output signals must ensure that there is no overlap when outputs of 3-State devices are tied together.

#### **PIN CONFIGURATION**



	TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
I	74F258A	3.5ns	14mA

#### ORDERING INFORMATION

	ORDER CODE	
DESCRIPTION	COMMERCIAL RANGE $V_{CC}$ = 5V ±10%, $T_{amb}$ = 0°C to +70°C	PKG. DWG.#
16-pin plastic DIP	N74F258AN	SOT38-4
16-pin plastic SO	N74F258AD	SOT109-1

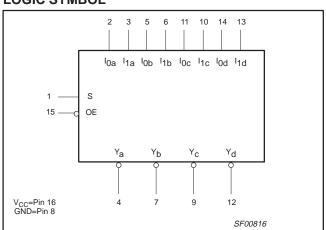
#### INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
I <sub>0n</sub> , I <sub>1n</sub>	Data inputs	1.0/1.0	20μA/0.6mA
S	Common select input	1.0/1.0	20μA/0.6mA
ŌĒ	Output Enable input (active Low)	1.0/1.0	20μA/0.6mA
$\overline{Y}_a - \overline{Y}_d$	Data outputs	150/40	3.0mA/24mA

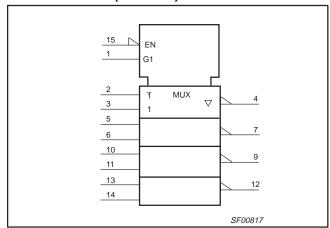
#### NOTE:

One (1.0) FAST Unit Load is defined as:  $20\mu A$  in the High state and 0.6mA in the Low state.

#### **LOGIC SYMBOL**



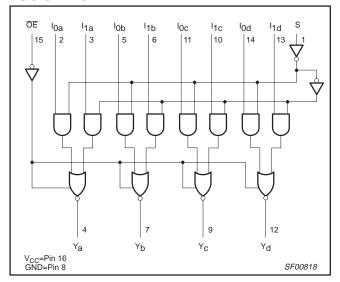
#### LOGIC SYMBOL (IEEE/IEC)



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#### **LOGIC DIAGRAM**



#### **FUNCTION TABLE**

	INP	UTS		OUTPUT
ŌĒ	S	I <sub>0</sub>	I <sub>1</sub>	Y
Н	Х	Х	Х	Z
L	Н	Х	L	Н
L	Н	X	Н	L
L	L	L	X	Н
L	L	Н	X	L

H = High voltage level
L = Low voltage level

X = Don't care Z = High impedance "off" state

#### **ABSOLUTE MAXIMUM RATINGS**

(Operation beyond the limit set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V <sub>CC</sub>	Supply voltage	-0.5 to +7.0	V
V <sub>IN</sub>	Input voltage	-0.5 to +7.0	V
I <sub>IN</sub>	Input current	-30 to +5	mA
V <sub>OUT</sub>	Voltage applied to output in High output state	–0.5 to V <sub>CC</sub>	V
I <sub>OUT</sub>	Current applied to output in Low output state	48	mA
T <sub>amb</sub>	Operating free-air temperature range	0 to +70	°C
T <sub>stg</sub>	Storage temperature range	-65 to +150	°C

#### **RECOMMENDED OPERATING CONDITIONS**

SYMBOL	PARAMETER		LIMITS		UNIT
STWIBOL	TANAMETER	MIN	NOM	MAX	UNIT
V <sub>CC</sub>	Supply voltage	4.5	5.0	5.5	V
V <sub>IH</sub>	High-level input voltage	2.0			V
V <sub>IL</sub>	Low-level input voltage			0.8	V
I <sub>IK</sub>	Input clamp current			-18	mA
I <sub>OH</sub>	High-level output current			-3	mA
I <sub>OL</sub>	Low-level output current			24	mA
T <sub>amb</sub>	Operating free-air temperature range	0		70	°C

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#### DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER			TEST			LIMITS		UNIT
STWIBOL	PARAMETER			CONDITIONS <sup>1</sup>	MIN	TYP <sup>2</sup>	MAX	UNIT	
V <sub>OH</sub>	High-level output voltage		V <sub>CC</sub> = MIN, V	IL = MAX,	2.4			V	
			V <sub>IH</sub> = MIN, I <sub>O</sub>	L = MAX	±5%V <sub>CC</sub>	2.7	3.3		V
V <sub>OL</sub>	Low-level output voltage		V <sub>CC</sub> = MIN, V	IL = MAX,	±10%V <sub>CC</sub>		0.30	0.50	V
			V <sub>IH</sub> = MIN, I <sub>O</sub>	L = MAX	±5%V <sub>CC</sub>		0.35	0.50	V
$V_{IK}$	Input clamp voltage		$V_{CC} = MIN, I_I$	= I <sub>IK</sub>			-0.73	-1.2	V
I <sub>I</sub>	Input current at maximum input voltage		V <sub>CC</sub> = MAX, V	V <sub>I</sub> = 7.0V			100	μΑ	
I <sub>IH</sub>	High-level input current		V <sub>CC</sub> = MAX, V	$V_1 = 2.7V$			20	μΑ	
$I_{\rm IL}$	Low-level input current		V <sub>CC</sub> = MAX, \	V <sub>I</sub> = 0.5V			-0.6	mA	
I <sub>OZH</sub>	Off-state output current, High-level voltage	applied	V <sub>CC</sub> = MAX, V	√ <sub>O</sub> = 2.7V			50	μΑ	
I <sub>OZL</sub>	Off-state output current, High-level voltage	applied	V <sub>CC</sub> = MAX, V	√ <sub>O</sub> = 0.5V				-50	μΑ
I <sub>OS</sub>	Short-circuit output current <sup>3</sup>		V <sub>CC</sub> = MAX			-60		-150	mA
		I <sub>CCH</sub>		I <sub>1n</sub> =4.5V, <del>OE</del> =I <sub>0</sub>	<sub>n</sub> =S=GND		8.5	11.5	mA
I <sub>CC</sub>	Supply current (total)	V <sub>CC</sub> = MAX	$V_{CC} = MAX$ $I_{1n}=S=4.5V, \overline{OE}=I_{0n}=GND$			17	23	mA	
		I <sub>CCZ</sub>		I <sub>1n</sub> = <del>OE</del> =4.5V,I <sub>0n</sub>	=S=GND		16	22	mA

#### NOTES:

- 1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- 2. All typical values are at  $V_{CC}$  = 5V,  $T_{amb}$  = 25°C.

#### **AC ELECTRICAL CHARACTERISTICS**

SYMBOL	PARAMETER	TEST CONDITIONS	v	<sub>amb</sub> = +25° ′ <sub>CC</sub> = +5.0 60pF, R <sub>L</sub> =	V	$T_{amb} = -55^{\circ}$ $V_{CC} = +5.$ $C_{L} = 50pF,$	UNIT	
			MIN	TYP	MAX	MIN	MAX	
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation delay $I_n$ to $\overline{Y}_n$	Waveform 1	3.0 1.0	4.5 2.5	6.0 4.0	2.5 1.0	7.0 4.5	ns ns
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation delay S to $\overline{Y}_n$	Waveform 2	3.5 2.5	6.5 6.0	8.0 8.0	3.5 2.5	9.0 9.0	ns ns
t <sub>PZH</sub> t <sub>PZL</sub>	Output enable time to High or Low level	Waveform 3 Waveform 4	4.0 4.0	6.0 5.5	7.5 7.5	3.5 3.5	8.5 8.5	ns ns
t <sub>PHZ</sub> t <sub>PLZ</sub>			2.0 2.0	3.5 3.5	5.5 5.5	2.0 2.0	6.5 6.0	ns ns

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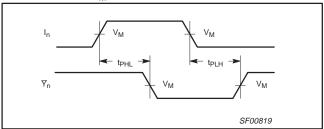
<sup>3.</sup> Not more than one output should be shorted at a time. For testing I<sub>OS</sub>, the use of High-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I<sub>OS</sub> tests should be performed last.

## Quad 2-line to 1-line selector/multiplexer, inverting (3-State)

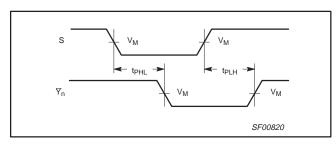
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#### **AC WAVEFORMS**

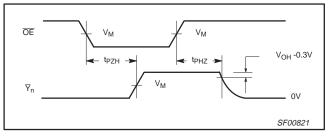
For all waveforms,  $V_M = 1.5V$ .



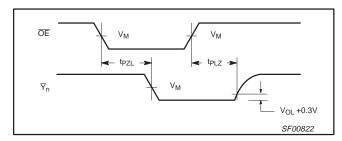
Waveform 1. Propagation Delay Data and Select to Output



Waveform 2. Propagation Delay Select to Output

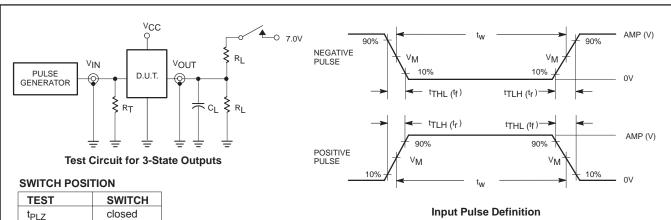


Waveform 3. 3-State Output Enable Time to High Level and Output Disable Time from High Level



Waveform 4. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

#### **TEST CIRCUIT AND WAVEFORM**



 $t_{PZL}$ 

All other

**DEFINITIONS:** R<sub>L</sub> = Load resistor;

see AC electrical characteristics for value.

closed

open

 $\begin{array}{ll} C_L &=& Load \ capacitance \ includes \ jig \ and \ probe \ capacitance; \\ & see \ AC \ electrical \ characteristics \ for \ value. \end{array}$ 

R<sub>T</sub> = Termination resistance should be equal to Z<sub>OUT</sub> of pulse generators.

family	INP	INPUT PULSE REQUIREMENTS											
family	amplitude	V <sub>M</sub>	rep. rate	t <sub>w</sub>	t <sub>TLH</sub>	t <sub>THL</sub>							
74F	3.0V	1.5V	1MHz	500ns	2.5ns	2.5ns							

SF00777

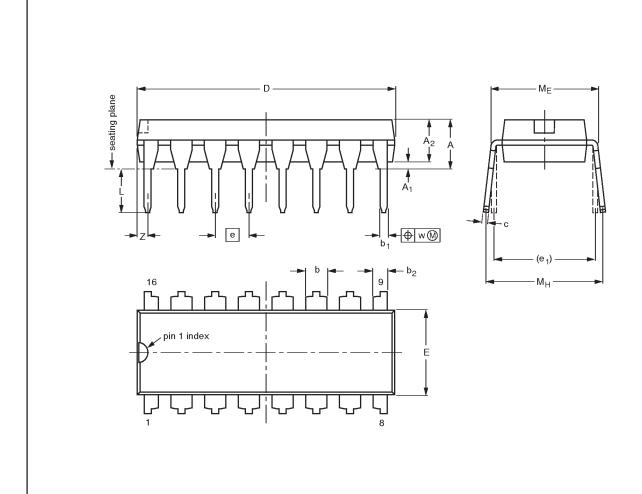
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### Quad 2-line to 1-line selector/multiplexer, inverting (3-State)

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#### DIP16: plastic dual in-line package; 16 leads (300 mil)

SOT38-4



#### DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A <sub>1</sub> min.	A <sub>2</sub> max.	b	b <sub>1</sub>	b <sub>2</sub>	С	D <sup>(1)</sup>	E <sup>(1)</sup>	е	e <sub>1</sub>	L	ME	M <sub>H</sub>	w	Z <sup>(1)</sup> max.
mm	4.2	0.51	3.2	1.73 1.30	0.53 0.38	1.25 0.85	0.36 0.23	19.50 18.55	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	0.76
inches	0.17	0.020	0.13	0.068 0.051	0.021 0.015	0.049 0.033	0.014 0.009	0.77 0.73	0.26 0.24	0.10	0.30	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.030

scale

10 mm

#### Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE		REFER	EUROPEAN	ISSUE DATE			
VERSION	IEC	JEDEC	EIAJ		PROJECTION	ISSUE DATE	
SOT38-4						<del>92-11-17</del> 95-01-14	

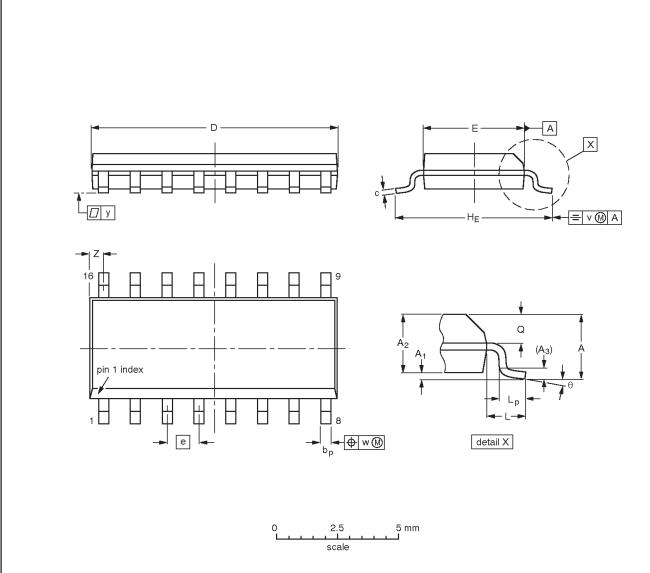
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### Quad 2-line to 1-line selector/multiplexer, inverting (3-State)

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#### SO16: plastic small outline package; 16 leads; body width 3.9 mm

SOT109-1



#### DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	bp	c	D <sup>(1)</sup>	E <sup>(1)</sup>	е	HE	L	Lp	Q	v	w	у	Z <sup>(1)</sup>	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	10.0 9.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8°
inches	0.069	0.010 0.004	0.057 0.049	0.01		0.0100 0.0075	0.39 0.38	0.16 0.15	0.050	0.244 0.228	0.041	0.039 0.016		0.01	0.01	0.004	0.028 0.012	0°

#### Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE	REFERENCES				EUROPEAN	ISSUE DATE
VERSION	IEC	JEDEC	EIAJ		PROJECTION	ISSUE DATE
SOT109-1	076E07S	MS-012AC				<del>95-01-23</del> 97-05-22

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### Quad 2-line to 1-line selector/multiplexer, inverting (3-State)

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DEFINITIONS					
Data Sheet Identification	Product Status	Definition			
Objective Specification	Formative or in Design	This data sheet contains the design target or goal specifications for product development. Specifications may change in any manner without notice.			
Preliminary Specification	Preproduction Product	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.			
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