

DATA SHEET

74F50728

Synchronizing cascaded dual positive
edge-triggered D-type flip-flop

Positive specification

1990 Sep 14

IC15 Data Handbook

Synchronizing cascaded dual positive edge-triggered D-type flip-flop

74F50728

FEATURES

- Metastable immune characteristics
- Output skew less than 1.5ns
- See 74F5074 for synchronizing dual D-type flip-flop
- See 74F50109 for synchronizing dual J-K positive edge-triggered flip-flop
- See 74F50729 for synchronizing dual dual D-type flip-flop with edge-triggered set and reset
- Industrial temperature range available (-40°C to +85°C)

DESCRIPTION

The 74F50728 is a cascaded dual positive edge-triggered D-type featuring individual data, clock, set and reset inputs; also true and complementary outputs.

Set ($\bar{S}D_n$) and reset ($\bar{R}D_n$) are asynchronous active low inputs and operate independently of the clock (CP_n) input. They set and reset both flip-flops of a cascaded pair simultaneously. Data must be stable just one setup time prior to the low-to-high transition of the clock for guaranteed propagation delays.

ORDERING INFORMATION

| DESCRIPTION | ORDER CODE | | PKG DWG # |
|--------------------|--|--|-----------|
| | COMMERCIAL RANGE $V_{CC} = 5V \pm 10\%$, $T_{amb} = 0^\circ C$ to $+70^\circ C$ | INDUSTRIAL RANGE $V_{CC} = 5V \pm 10\%$, $T_{amb} = -40^\circ C$ to $+85^\circ C$ | |
| 14-pin plastic DIP | N74F50728N | I74F50728N | SOT27-1 |
| 14-pin plastic SO | N74F50728D | I74F50728D | SOT108-1 |

INPUT AND OUTPUT LOADING AND FAN OUT TABLE

| PINS | DESCRIPTION | 74F (U.L.) HIGH/ LOW | LOAD VALUE HIGH/ LOW |
|---------------------------------|-----------------------------------|-------------------------|-------------------------|
| D0, D1 | Data inputs | 1.0/0.417 | 20 μ A/250 μ A |
| CP0, CP1 | Clock inputs (active rising edge) | 1.0/1.0 | 20 μ A/20 μ A |
| $\bar{S}D_0$, $\bar{S}D_1$ | Set inputs (active low) | 1.0/1.0 | 20 μ A/20 μ A |
| $\bar{R}D_0$, $\bar{R}D_1$ | Reset inputs (active low) | 1.0/1.0 | 20 μ A/20 μ A |
| Q0, Q1, $\bar{Q}0$, $\bar{Q}1$ | Data outputs | 50/33 | 1.0mA/20mA |

NOTE: One (1.0) FAST unit load is defined as: 20 μ A in the high state and 0.6mA in the low state.

Clock triggering occurs at a voltage level and is not directly related to the transition time of the positive-going pulse. Following the hold time interval, data at the D_n input may be changed without affecting the levels of the output. Data entering the 74F50728 requires two clock cycles to arrive at the outputs.

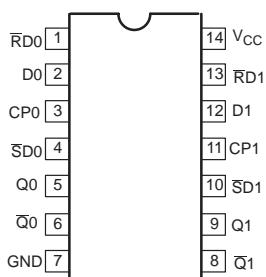
The 74F50728 is designed so that the outputs can never display a metastable state due to setup and hold time violations. If setup time and hold time are violated the propagation delays may be extended beyond the specifications but the outputs will not glitch or display a metastable state. Typical metastability parameters for the 74F50728 are: $\tau \equiv 135\text{ps}$ and $T_0 \equiv 9.8 \times 10^6 \text{ sec}$ where τ represents a function of the rate at which a latch in a metastable state resolves that condition and T_0 represents a function of the measurement of the propensity of a latch to enter a metastable state.

| TYPE | TYPICAL f_{max} | TYPICAL SUPPLY CURRENT (TOTAL) |
|----------|-------------------|--------------------------------|
| 74F50728 | 145 MHz | 23mA |

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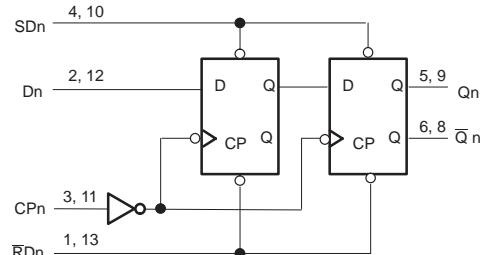
74F50728

PIN CONFIGURATION



SF00605

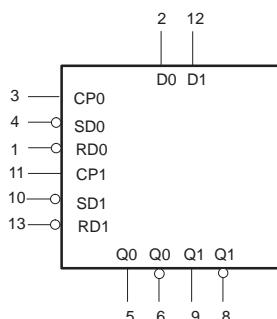
LOGIC DIAGRAM



SF00608

NOTE: Data entering the flip-flop requires two clock cycles to arrive at the output.

LOGIC SYMBOL



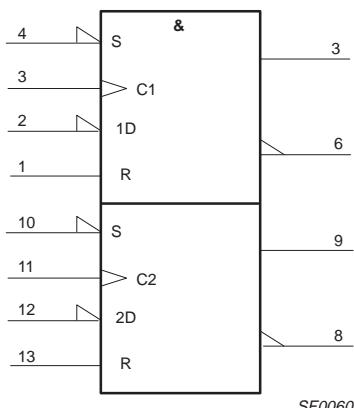
V_{CC} = Pin 14
GND = Pin 7

SF00606

SYNCHRONIZING SOLUTIONS

Synchronizing incoming signals to a system clock has proven to be costly, either in terms of time delays or hardware. The reason for this is that in order to synchronize the signals a flip-flop must be used to "capture" the incoming signal. While this is perhaps the only way to synchronize a signal, to this point, there have been problems with this method. Whenever the flop's setup or hold times are violated the flop can enter a metastable state causing the outputs in turn to glitch, oscillate, enter an intermediate state or change state in some abnormal fashion. Any of these conditions could be responsible for causing a system crash. To minimize this risk, flip-flops are often cascaded so that the input signal is captured on the first clock pulse and released on the second clock pulse (see Fig.1). This gives the first flop about one clock period minus the flop delay and minus the second flop's clock-to-Q setup time to resolve any metastable condition. This method greatly reduces the probability of the outputs of the synchronizing device displaying an abnormal state but the trade-off is that one clock cycle is lost to synchronize the incoming data and two separate flip-flops are required to produce the cascaded flop circuit. In order to assist the designer of synchronizing circuits Philips Semiconductors is offering the 74F50728.

IEC/IEEE SYMBOL



SF00607

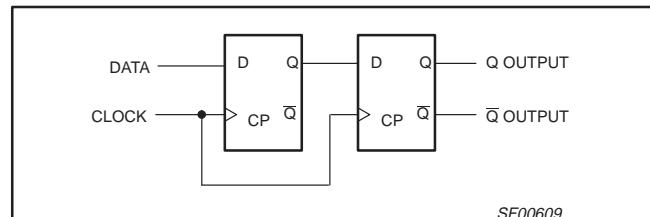


Figure 1.

The 50728 consists of two pair of cascaded D-type flip-flops with metastable immune features and is pin compatible with the 74F74. Because the flops are cascaded on a single part the metastability

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characteristics are greatly improved over using two separate flops that are cascaded. The pin compatibility with the 74F74 allows for plug-in retrofitting of previously designed systems.

Because the probability of failure of the 74F50728 is so remote, the metastability characteristics of the part were empirically determined based on the characteristics of its sister part, the 74F5074. The table below shows the 74F5074 metastability characteristics.

Having determined the T_0 and τ of the flop, calculating the mean time between failures (MTBF) for the 74F50728 is simple. It is, however, somewhat different than calculating MTBF for a typical part because data requires two clock pulses to transit from the input to the output. Also, in this case a failure is considered of the output beyond the normal propagation delay.

Suppose a designer wants to use the flop for synchronizing asynchronous data that is arriving at 10MHz (as measured by a frequency counter), and is using a clock frequency of 50MHz. He simply plugs his number into the equation below:

$$MTBF = e^{(t'/t)} / T_0 f_C f_I$$

In this formula, f_C is the frequency of the clock, f_I is the average input event frequency, and t' is the period of the clock input (20 nanoseconds). In this situation the f_I will be twice the data frequency of 20 MHz because input events consist of both of low and high data transitions. From Fig. 2 it is clear that the MTBF is greater than 10^{41} seconds. Using the above formula the actual MTBF is 2.23×10^{42} seconds or about 7×10^{34} years.

TYPICAL VALUES FOR τ AND T_0 AT VARIOUS V_{CC} S AND TEMPERATURES

| | $T_{amb} = 0^\circ C$ | | $T_{amb} = 25^\circ C$ | | $T_{amb} = 70^\circ C$ | |
|-----------------|-----------------------|--------------------------|------------------------|-----------------------|------------------------|-----------------------|
| | τ | T_0 | τ | T_0 | τ | T_0 |
| $V_{CC} = 5.5V$ | 125ps | 1.0×10^9 sec | 138ps | 5.4×10^6 sec | 160ps | 1.7×10^5 sec |
| $V_{CC} = 5.0V$ | 115ps | 1.3×10^{10} sec | 135ps | 9.8×10^6 sec | 167ps | 3.9×10^4 sec |
| $V_{CC} = 4.5V$ | 115ps | 3.4×10^{13} sec | 132ps | 5.1×10^8 sec | 175ps | 7.3×10^4 sec |

MEAN TIME BETWEEN FAILURES VERSUS DATA FREQUENCY AT VARIOUS CLOCK FREQUENCY

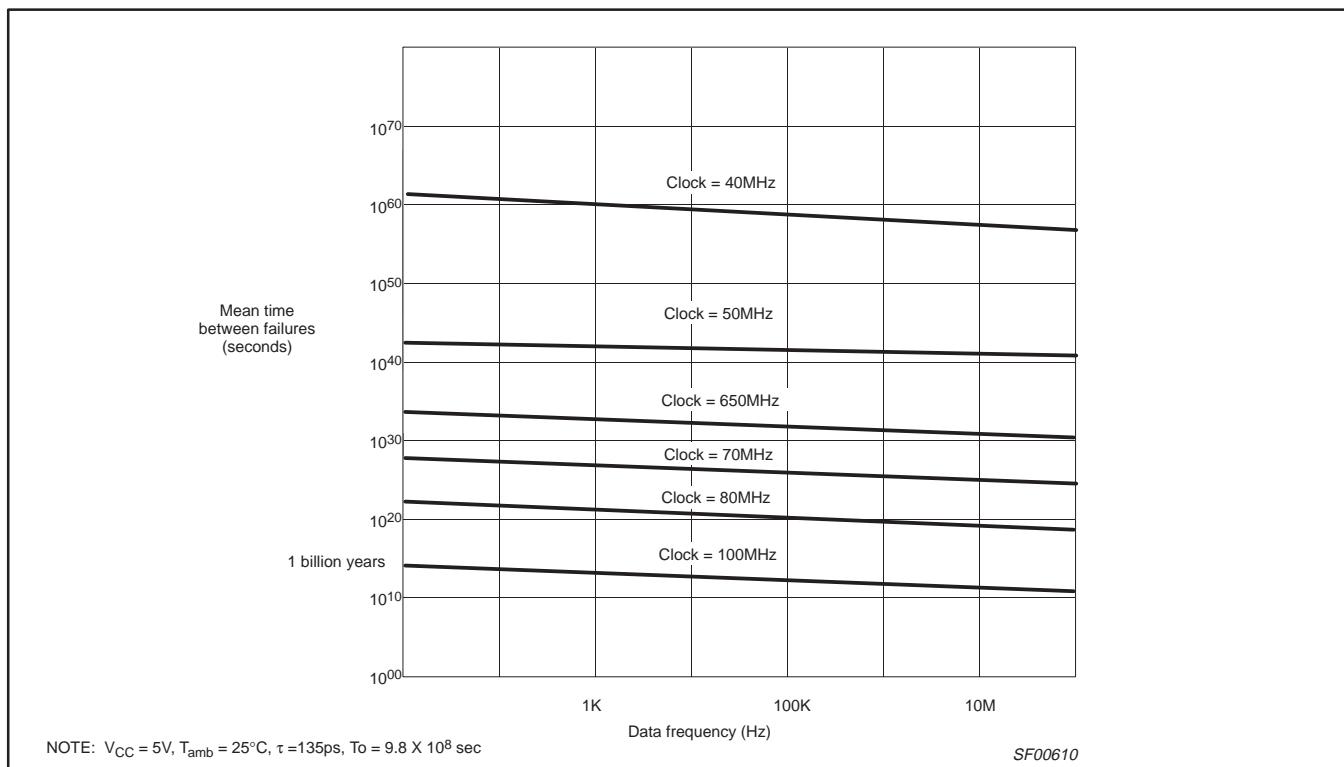


Figure 2.

Synchronizing cascaded dual positive edge-triggered D-type flip-flop

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FUNCTION TABLE

| INPUTS | | | | INTERNAL REGISTER | OUTPUTS | | OPERATING MODE |
|--------------|--------------|--------|-------|----------------------|---------|-------------|--------------------|
| $\bar{S}D_n$ | $\bar{R}D_n$ | CP_n | D_n | Q | Q_n | \bar{Q}_n | |
| L | H | X | X | H | H | L | Asynchronous set |
| H | L | X | X | L | L | H | Asynchronous reset |
| L | L | X | X | X | H | H | Undetermined* |
| H | H | ↑ | h | h | H | L | Load "1" |
| H | H | ↑ | l | l | L | H | Load "0" |
| H | H | L | X | NC | NC | NC | Hold |

NOTES:

H = High voltage level

h = High voltage level one setup time prior to low-to-high clock transition

L = Low voltage level

l = Low voltage level one setup time prior to low-to-high clock transition

NC = No change from the previous setup

X = Don't care

* = This setup is unstable and will change when either set of reset return to the high-level

↑ = Low-to-high clock transition.

** = Data entering the flip-flop requires two clock cycles to arrive at the output (see logic diagram)

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limit set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free air temperature range.)

| SYMBOL | PARAMETER | RATING | | UNIT |
|-----------|--|------------------|------------|------|
| | | MIN | NOM | |
| V_{CC} | Supply voltage | -0.5 to +7.0 | | V |
| V_{IN} | Input voltage | -0.5 to +7.0 | | V |
| I_{IN} | Input current | -30 to +5 | | mA |
| V_{OUT} | Voltage applied to output in high output state | -0.5 to V_{CC} | | V |
| I_{OUT} | Current applied to output in low output state | 40 | | mA |
| T_{amb} | Operating free air temperature range | Commercial range | 0 to +70 | °C |
| | | Industrial range | -40 to +85 | °C |
| T_{stg} | Storage temperature range | -65 to +150 | | °C |

RECOMMENDED OPERATING CONDITIONS

| SYMBOL | PARAMETER | LIMITS | | | UNIT |
|-----------|--------------------------------------|------------------|-----|-----|------|
| | | MIN | NOM | MAX | |
| V_{CC} | Supply voltage | 4.5 | 5.0 | 5.5 | V |
| V_{IH} | High-level input voltage | 2.4 | | | V |
| V_{IL} | Low-level input voltage | | | 0.8 | V |
| I_{Ik} | Input clamp current | | | -18 | mA |
| I_{OH} | High-level output current | | | -3 | mA |
| I_{OL} | Low-level output current | | | 20 | mA |
| T_{amb} | Operating free air temperature range | Commercial range | 0 | +70 | °C |
| | | Industrial range | -40 | +85 | °C |

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DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

| SYMBOL | PARAMETER | TEST CONDITIONS ¹ | | | LIMITS | | | UNIT |
|-----------------|---|--|--|---|--------|------------------|------|------|
| | | | | | MIN | TYP ² | MAX | |
| V _{OH} | High-level output voltage | V _{CC} = MIN, V _{IH} = MIN V _{IL} = MAX, | I _{OH} = MAX | ±10%V _{CC} ±5%V _{CC} | 2.5 | | | V |
| | | | | | 2.7 | 3.4 | | V |
| V _{OL} | Low-level output voltage | V _{CC} = MIN, V _{IL} = MAX, V _{IH} = MIN | I _{OL} = MAX | ±10%V _{CC} ±5%V _{CC} | | 0.30 | 0.50 | V |
| | | | | | | 0.30 | 0.50 | V |
| V _{IK} | Input clamp voltage | V _{CC} = MIN, I _I = I _{IK} | | | | -0.73 | -1.2 | V |
| I _I | Input current at maximum input voltage | V _{CC} = MAX, V _I = 7.0V | | | | | 100 | µA |
| I _{IH} | High-level input current | V _{CC} = MAX, V _I = 2.7V | | | | | 20 | µA |
| I _{IL} | Low-level input current | D _n CP _n , SD _n , RD _n | V _{CC} = MAX, V _I = 0.5V | | | | -250 | µA |
| | | | | | | | -20 | µA |
| I _{OS} | Short-circuit output current ³ | V _{CC} = MAX, V _O = 2.25V | | | -60 | | -150 | mA |
| I _{CC} | Supply current ⁴ (total) | V _{CC} = MAX | | | | 23 | 34 | mA |

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
4. Measure I_{CC} with the clock input grounded and all outputs open, then with Q and \bar{Q} outputs high in turn.

AC ELECTRICAL CHARACTERISTICS

| SYMBOL | PARAMETER | TEST CONDITION | LIMITS | | | | | | UNIT | | |
|--------------------------------------|---|----------------|--|------------|------------|--|------------|--|--------------|----|--|
| | | | T _{amb} = +25°C | | | T _{amb} = 0°C to +70°C | | T _{amb} = -40°C to +85°C | | | |
| | | | V _{CC} = +5.0V C _L = 50pF, R _L = 500Ω | | | V _{CC} = +5.0V ± 10% C _L = 50pF, R _L = 500Ω | | V _{CC} = +5.0V ± 10% C _L = 50pF, R _L = 500Ω | | | |
| | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | | |
| f _{max} | Maximum clock frequency | Waveform 1 | 100 | 145 | | 85 | | 70 | | ns | |
| t _{PLH} t _{PHL} | Propagation delay CP _n to Q _n or \bar{Q}_n | Waveform 1 | 2.0 2.0 | 3.8 3.8 | 6.0 6.0 | 1.5 2.0 | 6.5 6.5 | 1.5 2.0 | 7.5 7.0 | ns | |
| | | | | | | | | | | | |
| t _{PLH} t _{PHL} | Propagation delay SD _n RD _n to Q _n or \bar{Q}_n | Waveform 2 | 3.5 3.5 | 5.0 5.0 | 8.0 8.0 | 3.0 3.0 | 9.0 8.5 | 3.0 3.0 | 10.5 10.0 | ns | |
| | | | | | | | | | | | |
| t _{sk(0)} | Output skew ^{1, 2} | Waveform 4 | | | 1.5 | | 1.5 | | 1.5 | ns | |

NOTES TO AC ELECTRICAL CHARACTERISTICS

1. | t_{PLH} actual - t_{PHL} actual | for any one output compare to any other output where N and M are either LH or HL.
2. Skew lines are valid only under same conditions (temperature, V_{CC}, loading, etc.,).

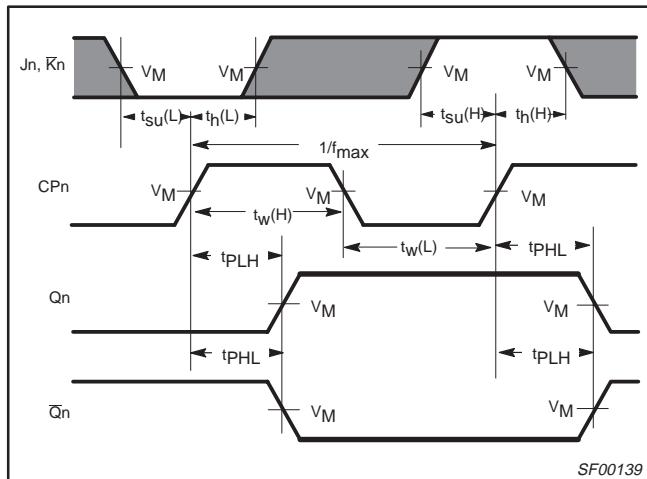
Synchronizing cascaded dual positive edge-triggered D-type flip-flop

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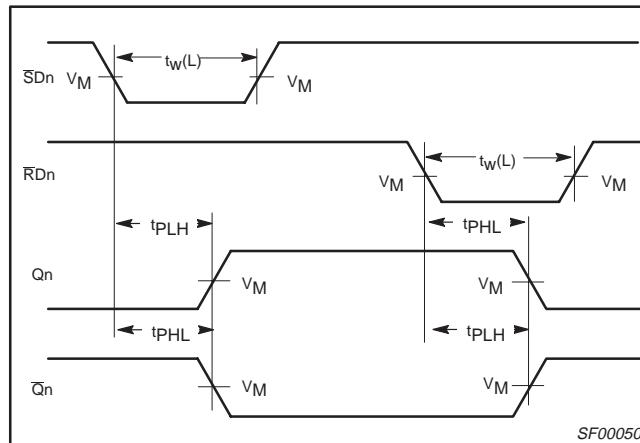
AC SETUP REQUIREMENTS

| SYMBOL | PARAMETER | TEST CONDITION | LIMITS | | | | | | UNIT | | |
|--|--------------------------------------|----------------|--------------------------|---|-------------------------------|---|-------------------------------|---|------|--|--|
| | | | T _{amb} = +25°C | | | T _{amb} = 0°C to +70°C | | T _{amb} = -40°C to +85°C | | | |
| | | | V _{CC} = +5.0V | C _L = 50pF, R _L = 500Ω | V _{CC} = +5.0V ± 10% | C _L = 50pF, R _L = 500Ω | V _{CC} = +5.0V ± 10% | C _L = 50pF, R _L = 500Ω | | | |
| t _{su} (H) t _{su} (L) | Setup time, high or low Dn to CPn | Waveform 1 | 1.5 1.5 | | 2.0 2.0 | | 2.0 2.0 | | ns | | |
| t _h (H) t _h (L) | Hold time, high or low Dn to CPn | Waveform 1 | 0.0 0.0 | | 1.5 1.5 | | 1.5 1.5 | | ns | | |
| t _w (H) t _w (L) | CPn pulse width, high or low | Waveform 2 | 3.0 4.0 | | 3.5 5.0 | | 4.0 5.5 | | ns | | |
| t _w (L) | SDn, RDn pulse width, low | Waveform 2 | 4.5 | | 4.0 | | 4.5 | | ns | | |
| t _{rec} | Recovery time SDn, RDn to CPn | Waveform 3 | 3.5 | | 3.5 | | 3.5 | | ns | | |

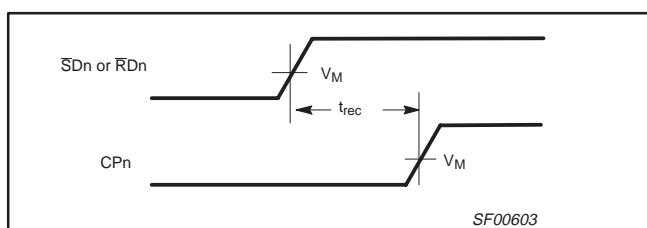
AC WAVEFORMS



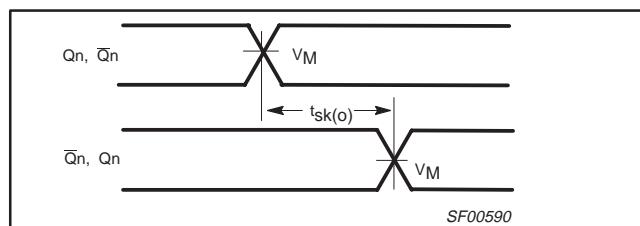
Waveform 1. Propagation delay for data to output, data setup time and hold times, and clock width, and maximum clock frequency



Waveform 2. Propagation delay for set and reset to output, set and reset pulse width



Waveform 3. Recovery time for set or reset to output



Waveform 4. Output skew

NOTES:

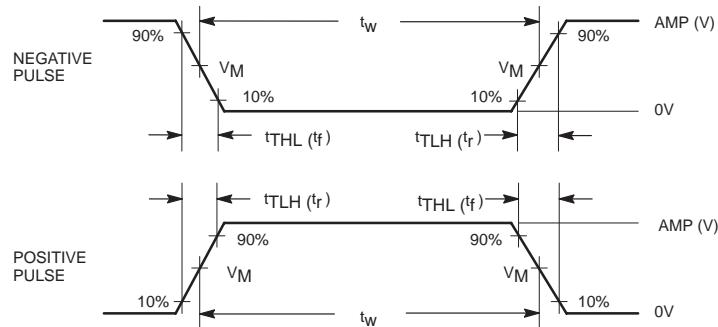
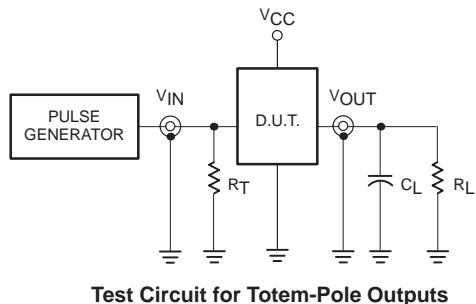
For all waveforms, V_M = 1.5V.

The shaded areas indicate when the input is permitted to change for predictable output performance.

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TEST CIRCUIT AND WAVEFORMS



DEFINITIONS:

R_L = Load resistor;
see AC ELECTRICAL CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance;
see AC ELECTRICAL CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of
pulse generators.

Input Pulse Definition

| family | INPUT PULSE REQUIREMENTS | | | | | |
|--------|--------------------------|-------|-----------|-------|-----------|-----------|
| | amplitude | V_M | rep. rate | t_W | t_{TLH} | t_{THL} |
| 74F | 3.0V | 1.5V | 1MHz | 500ns | 2.5ns | 2.5ns |

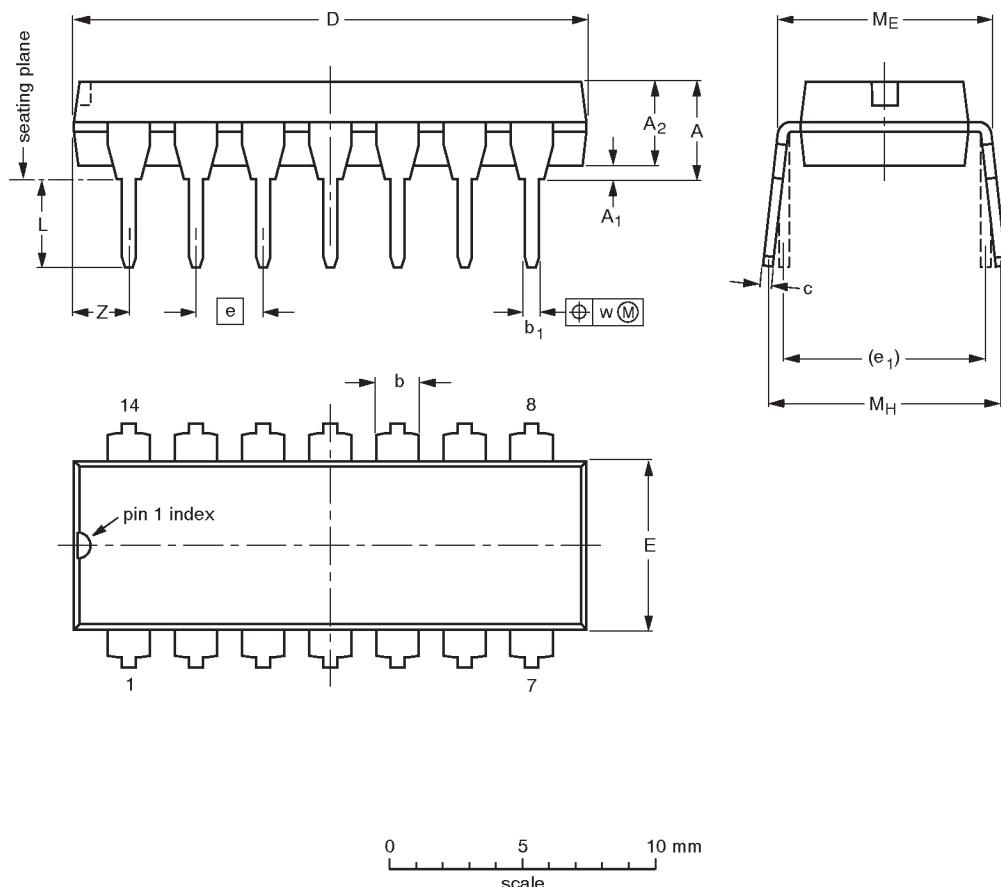
SF00006

Synchronizing cascaded dual positive edge-triggered D-type flip-flop

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DIP14: plastic dual in-line package; 14 leads (300 mil)

SOT27-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

| DIMENSIONS (Inch dimensions are derived from the original mm dimensions) | | | | | | | | | | | | | | | |
|--|--------|---------------------|---------------------|----------------|----------------|----------------|------------------|------------------|------|----------------|--------------|----------------|----------------|-------|-----------------------|
| UNIT | A max. | A ₁ min. | A ₂ max. | b | b ₁ | c | D ⁽¹⁾ | E ⁽¹⁾ | e | e ₁ | L | M _E | M _H | w | Z ⁽¹⁾ max. |
| mm | 4.2 | 0.51 | 3.2 | 1.73 1.13 | 0.53 0.38 | 0.36 0.23 | 19.50 18.55 | 6.48 6.20 | 2.54 | 7.62 | 3.60 3.05 | 8.25 7.80 | 10.0 8.3 | 0.254 | 2.2 |
| inches | 0.17 | 0.020 | 0.13 | 0.068 0.044 | 0.021 0.015 | 0.014 0.009 | 0.77 0.73 | 0.26 0.24 | 0.10 | 0.30 | 0.14 0.12 | 0.32 0.31 | 0.39 0.33 | 0.01 | 0.087 |

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

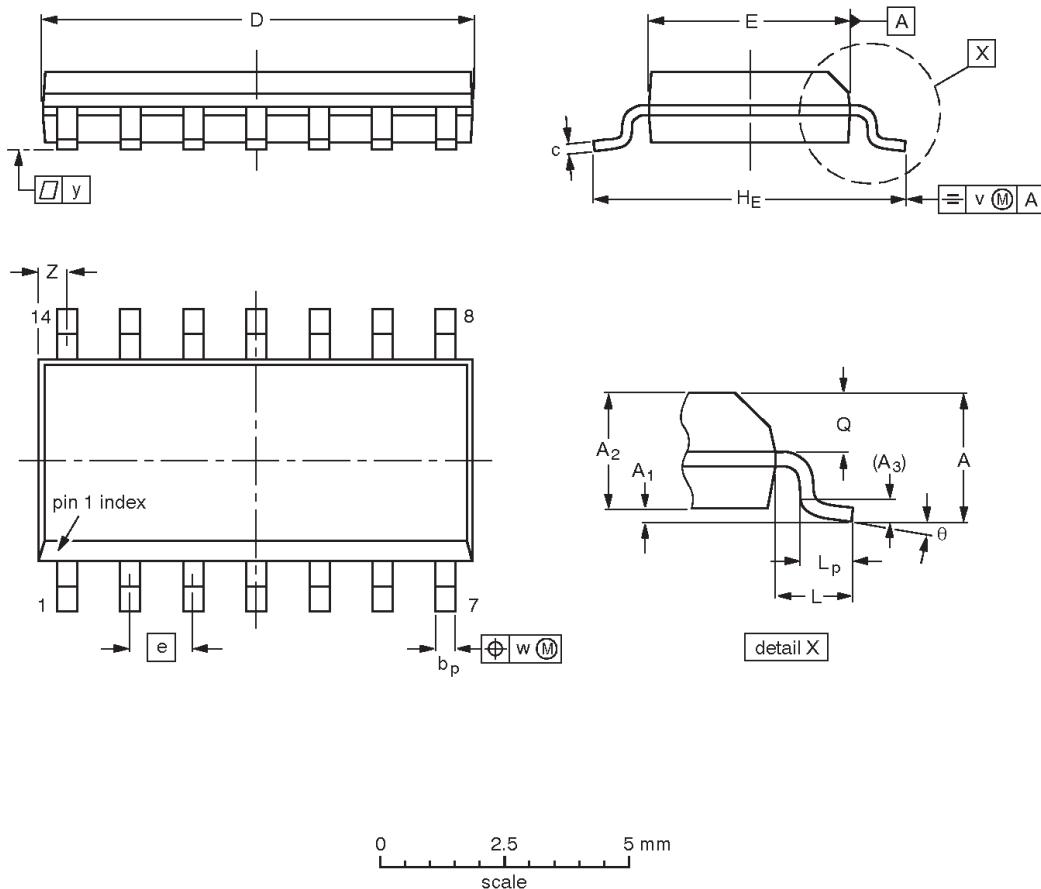
| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|-----------------|------------|----------|------|--|---|----------------------|
| | IEC | JEDEC | EIAJ | | | |
| SOT27-1 | 050G04 | MO-001AA | | |   | 92-11-17 95-03-11 |

Synchronizing cascaded dual positive edge-triggered D-type flip-flop

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SO14: plastic small outline package; 14 leads; body width 3.9 mm

SOT108-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

| UNIT | A max. | A ₁ | A ₂ | A ₃ | b _p | c | D ⁽¹⁾ | E ⁽¹⁾ | e | H _E | L | L _p | Q | v | w | y | Z ⁽¹⁾ | θ |
|--------|----------------|----------------|----------------|----------------|----------------|------------------|------------------|------------------|-------|----------------|-------|----------------|----------------|------|------|-------|------------------|----------|
| mm | 1.75 0.10 | 0.25 1.25 | 1.45 | 0.25 | 0.49 0.36 | 0.25 0.19 | 8.75 8.55 | 4.0 3.8 | 1.27 | 6.2 5.8 | 1.05 | 1.0 0.4 | 0.7 0.6 | 0.25 | 0.25 | 0.1 | 0.7 0.3 | 8° 0° |
| inches | 0.069 0.004 | 0.010 0.049 | 0.057 | 0.01 | 0.019 0.014 | 0.0100 0.0075 | 0.35 0.34 | 0.16 0.15 | 0.050 | 0.244 0.228 | 0.041 | 0.039 0.016 | 0.028 0.024 | 0.01 | 0.01 | 0.004 | 0.028 0.012 | |

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|--------------------|------------|----------|------|--|------------------------|-----------------------|
| | IEC | JEDEC | EIAJ | | | |
| SOT108-1 | 076E06S | MS-012AB | | | | -95-01-23 97-05-22 |

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NOTES

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Data sheet status

| Data sheet status | Product status | Definition [1] |
|---------------------------|----------------|--|
| Objective specification | Development | This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice. |
| Preliminary specification | Qualification | This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product. |
| Product specification | Production | This data sheet contains final specifications. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product. |

[1] Please consult the most recently issued datasheet before initiating or completing a design.

Definitions

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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811 East Arques Avenue
P.O. Box 3409
Sunnyvale, California 94088-3409
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