

FAN8620B

12V Spindle Motor and Voice Coil Motor Driver

Features

Spindle Motor Driver

- Soft commutation
- Spindle brake after retract
- Adjustable brake delay time
- 1.5A max. current power driver
- Low output saturation voltage: 1V typical @1.2A
- PWM decoder & filter for soft commutation
- The external circuit (ASIC) based start-up, commutation and motor speed control

Voice Coil Motor Driver

- Trimmed low offset current
- 1.2A max. current power driver
- Gain selection and adjustable gain
- Automatic power failure retract function
- Class AB linear amplifier with no dead zone
- Low output saturation voltage: 0.8V typical @1.0A
- Internal full bridge with V_{PNP} (Vertical PNP) & NPN transistors

Power Monitoring

- Power on reset with delay
- Hysteresis on both power comparators
- Over temperature & over current shut down
- 5V and 12V power monitor threshold accuracy $\pm 2\%$

Others

- Can be used with 5Volt and 3.3Volt control signals(CNTL1,CNTL2 & CNTL3) for ASIC Interface

Package

- 48QFPH (48 pin quad flat package heat-sink)

Typical Application

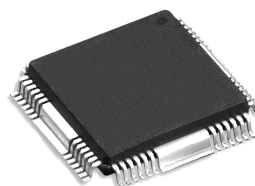
- Hard disk drive (HDD)

Description

The FAN8620B is an ASIC combination chip, designed for the HDD application, it includes the following functions: spindle motor drive, voice coil motor drive, retract and power management.

To drive and control the spindle, the external ASIC provides the appropriate control signals (Start up, commutation, speed control) to the FAN8620B. The spindle motor condition is monitored by the FG output and the motor speed control is accomplished via the PWMSP input. The ASIC controls the voice coil motor current via PWMH and PWML inputs and the power management circuit always monitors the power supply voltages.

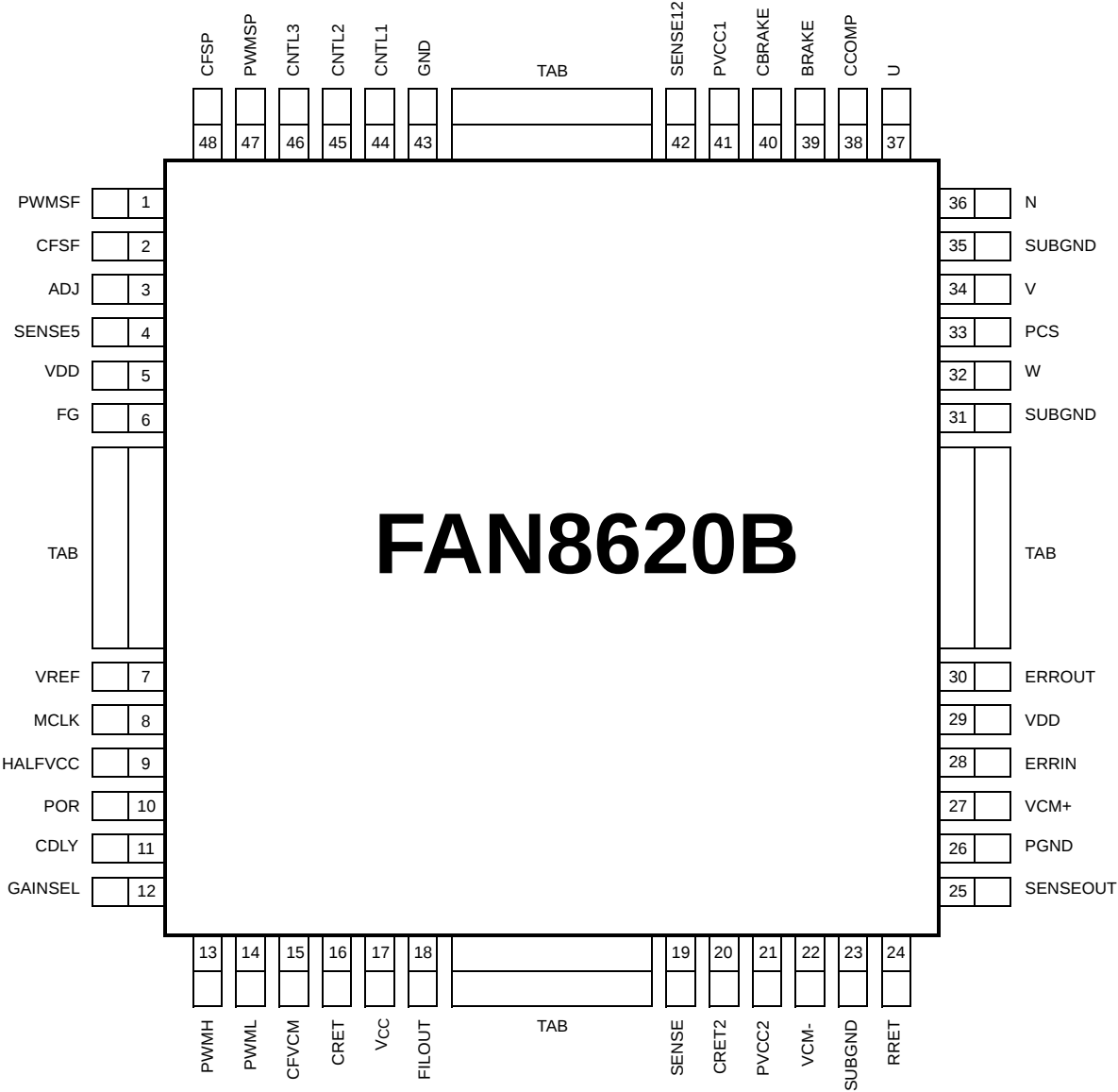
48-QFPH-1414



Ordering Information

Device	Package	Operating Temp.
FAN8620B	48-QFPH-1414	0 ~ 70°C

Pin Assignments



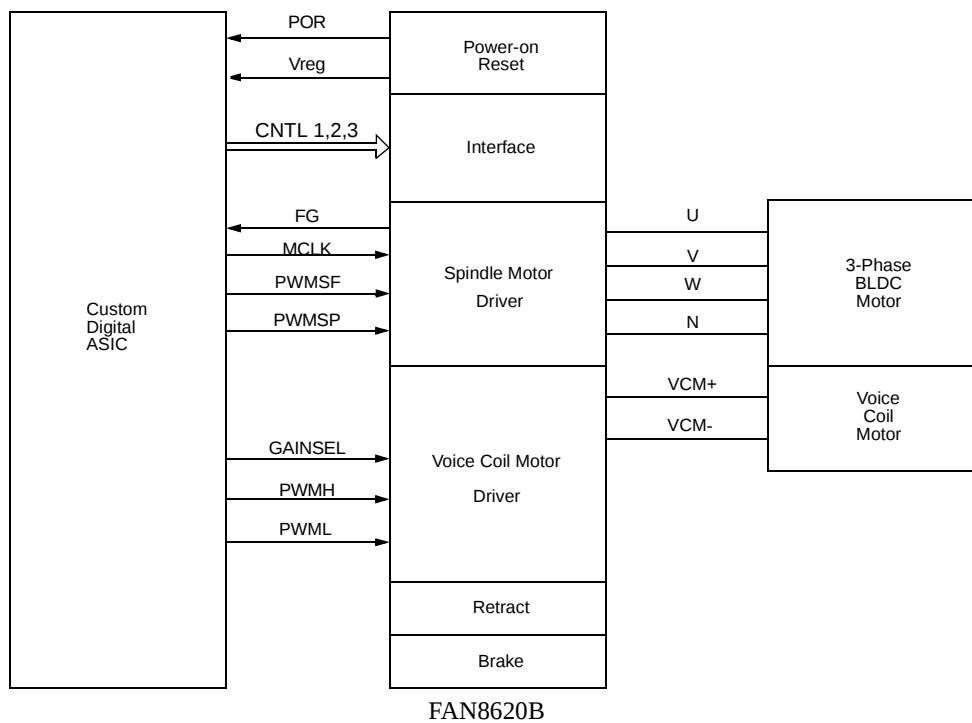
Pin Definitions

Pine Number	Pin Name	I/O	Pin Function Description
1	PWMSF	I	PWM input for spindle soft commutation
2	CFSF	-	Capacitor for spindle PWM soft commutation filter
3	ADJ	-	Reference voltage adjustable
4	SENSE5	-	Adjustable threshold voltage to 5V
5	VDD	-	5V power supply
6	FG	O	Frequency generation to spindle speed
7	VREF	O	Voltage reference output for ASIC power
8	MCLK	I	Clock from ASIC for commutation
9	HALFVCC	O	1/2 VCC pin
10	POR	O	Fault output(Power On Reset & Thermal Shut Down)
11	CDLY	-	Delay capacitor for power on reset
12	GAINSEL	I	VCM current Amplifier gain selection
13	PWMH	I	PWM signal input (MSB)
14	PWML	I	PWM signal input (LSB)
15	CFVCM	-	Filter capacitor for VCM PWM control
16	CRET	-	Delay capacitor for retract
17	VCC	-	12V power line
18	FILOUT	O	VCM PWM output
19	SENSE	I	VCM current sense Amplifier input
20	CRET2	-	Power for VCM retract
21	PVCC2	-	12V power line for VCM output
22	VCM(-)	O	VCM negative output
23	SUBGND	-	Ground
24	RRET	-	Adjustable maximum retract current
25	SENSEOUT	O	VCM current sense Amplifier output
26	PGND	-	Ground
27	VCM(+)	O	VCM positive output
28	ERRIN	I	VCM error Amplifier negative input
29	VDD	-	5V power supply
30	ERROUT	O	VCM error Amplifier output
31	SUBGND	-	Ground
32	W	O	Spindle motor W phase output

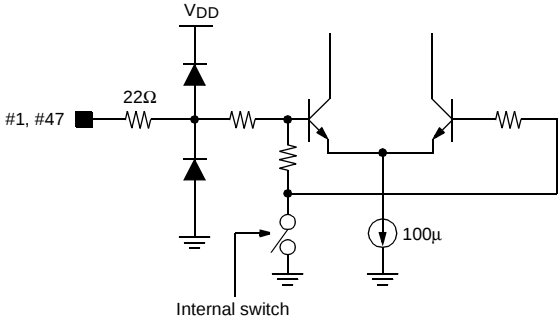
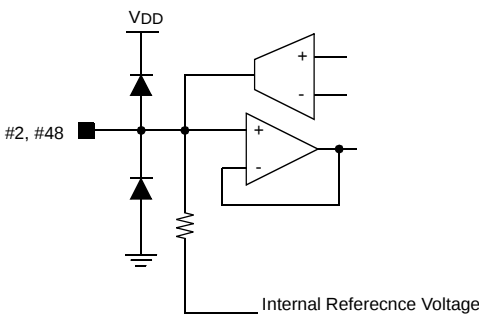
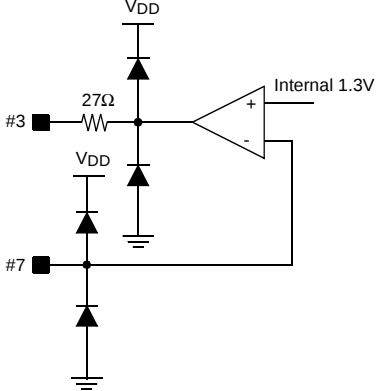
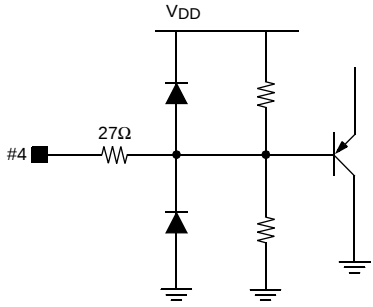
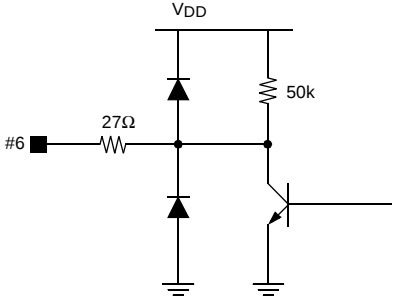
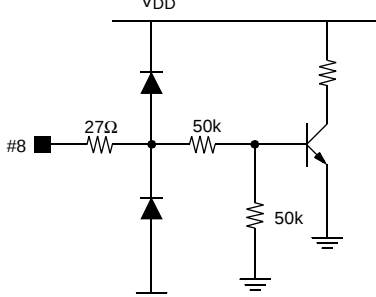
Pin Definitions (Continued)

Pine Number	Pin Name	I/O	Pin Function Description
33	PCS	O	Spindle output current sensing
34	V	O	Spindle motor V phase output
35	SUBGND	-	Ground
36	N	-	Spindle motor neutral point
37	U	O	Spindle motor U phase output
38	CCOMP	-	Spindle output control compensation
39	BRAKE	O	Dynamic brake
40	CBRAKE	-	Back-EMF charging capacitor for brake power
41	PVCC1	-	12V power line for spindle
42	SENSE12	-	Adjustable for threshold voltage to 12V
43	GND	-	Ground
44	CNTL1	I	Control input for spindle and brake
45	CNTL2	I	Control input for start-up clock and soft commutation
46	CNTL3	I	Control input for VCM Amplifier & retract
47	PWMSP	I	PWM input for spindle speed control
48	CFSP	-	Filter capacitor for spindle PWM control

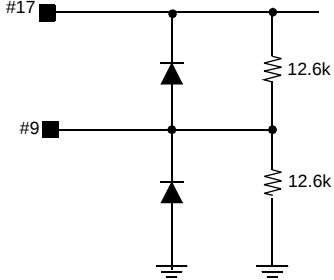
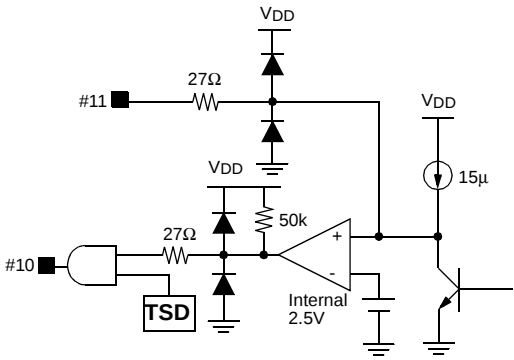
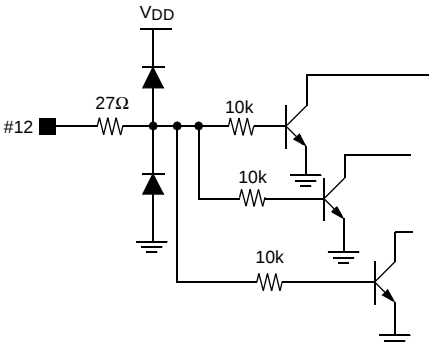
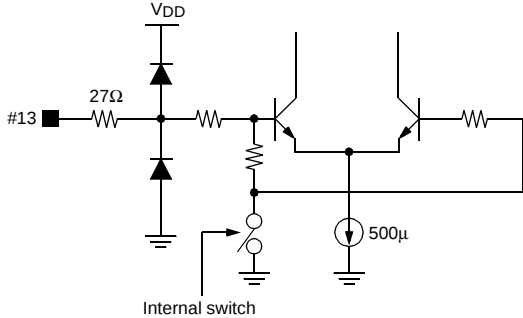
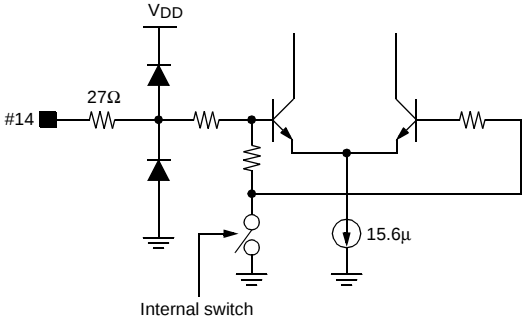
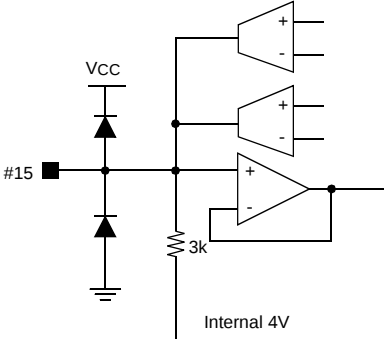
Internal Block Diagram



Equivalent Circuits

PWM decoder filter input of Spindle part 	PWM decoder filter Capacitor of Spindle part 
Regulator part 	Sense5 input 
FG output 	MCLK input 

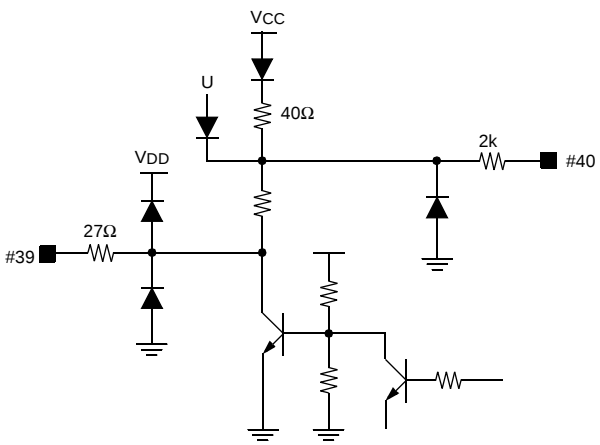
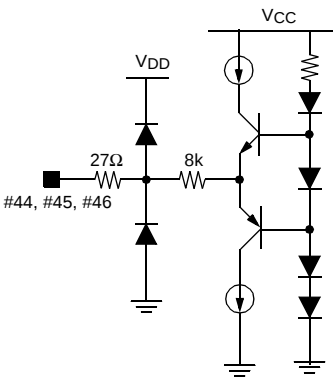
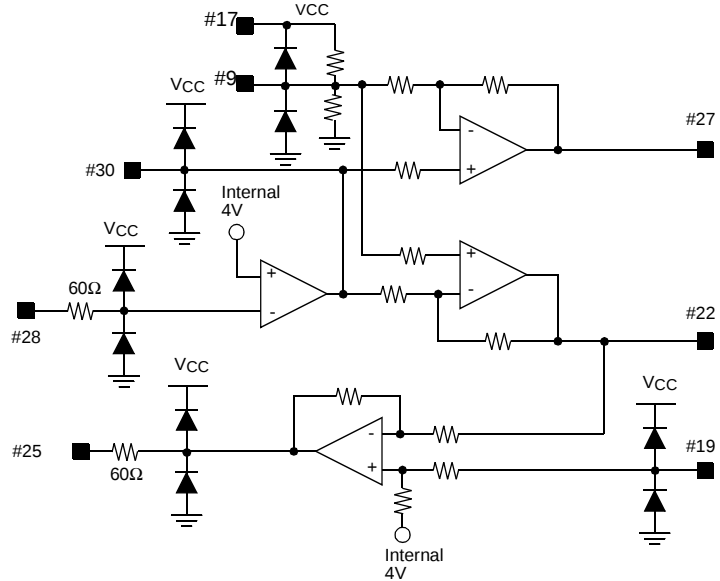
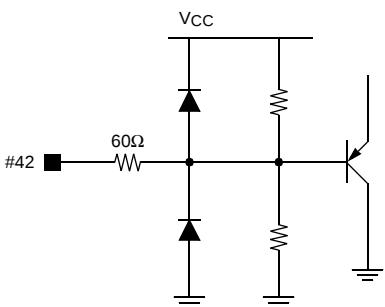
Equivalent Circuits (Continued)

VCM power amplifier reference 	Power on reset part 
VCM gain selection input 	VCM PWM high input 
VCM PWM low input 	VCM PWM filter Capacitor 

Equivalent Circuits (Continued)

Filtered VCM PWM command output	VCM current sense input
Capacitor for retract power	Maximum retract current set input
Spindle motor output compensation Capacitor	Spindle motor output and Back-EMF sensing part

Equivalent Circuits (Continued)

Dynamic brake part	CNTL1, 2, 3 input
	
VCM output and control part	Sense12 input
	

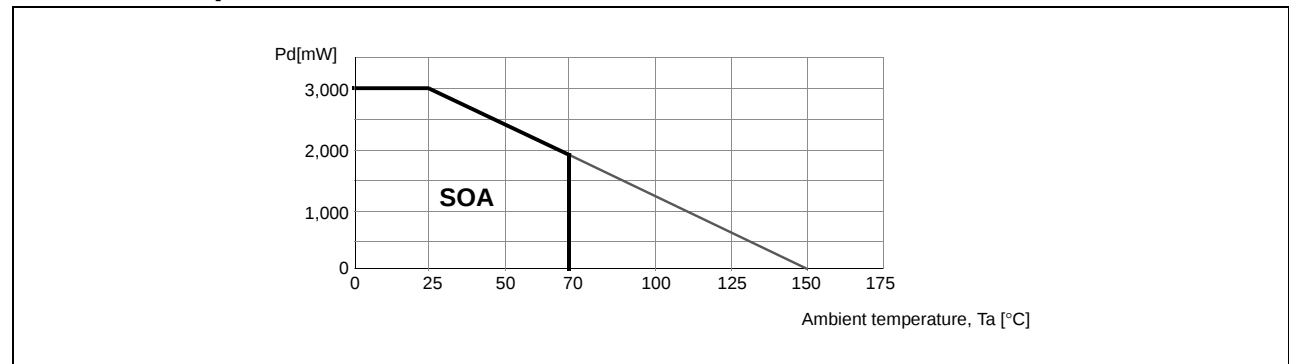
Absolute Maximum Ratings (Ta = 25°C)

Parameter	Symbol	Value	Unit
Maximum signal block supply voltage for 5V line	VDDMAX	6.0	V
Maximum signal block supply voltage for 12V line	VCCMAX	15.0	V
Maximum power block supply voltage for 12V line	PVCCMAX	15.0	V
Maximum output current of Spindle motor	ISOMAX	2.0	A
Maximum output current of VCM	IVOMAX	1.2	A
Power dissipation	PD	3.0 ^{note}	W
Storage temperature	TSTG	-55 ~ 125	°C
Maximum junction temperature	TJMAX	150	°C
Operating ambient temperature	TA	0 ~ 70	°C

Notes:

1. Power dissipation is reduced 16mW / °C for using above Ta=25°C.
2. Do not exceed Pd and SOA(Safe Operating Area).

Power Dissipation Curve



Recommended Operating Conditions (Ta = 25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	VCC, PVCC1, PVCC2	10.8	12.0	13.2	V
Supply voltage for logic circuit	VDD	4.5	5.0	5.5	V

Electrical Characteristics

(Ta=25°C, unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Units
SUPPLY CURRENT⁽¹⁾						
5V line supply current 1	IDD1	Brake Mode (CNTL1= Low)	–	55	65	mA
5V line supply current 2	IDD2	Stand by	–	20	25	mA
5V line supply current 3	IDD3	Normal Mode (CNTL1 = CNTL3 = High)	–	20	25	mA
5V line supply current 4	IDD4	Retract Mode (CNTL3=Low)	–	20	25	mA
12V line supply current 1	ICC1	Brake Mode (CNTL1 =Low)	–	7	12	mA
12V line supply current 2	ICC2	Stand by	–	9	15	mA
12V line supply current 3	ICC3	Normal Mode (CNTL1 = CNTL3 = High)	–	30	50	mA
12V line supply current 4	ICC4	Retract Mode (CNTL3 =Low)	–	9	14	mA
POWER MONITOR						
Threshold voltage level for 12V	VTH12	VCC=Sweep, VDD=5V	9.1	9.45	9.8	V
Hysteresis on 12V comparator	VHYS12	VCC=Sweep, VDD=5V	100	200	300	mV
Adjustable pin voltage for 12V	V12	VCC=12V, VDD=5V	3.0	3.2	3.4	V
Threshold voltage level for 5V	VTH5	VCC=12V, VDD=Sweep	3.6	3.95	4.3	V
Hysteresis on 5V comparator	VHYS5	VCC=12V, VDD=Sweep	50	100	150	mV
Adjustable pin voltage for 5V	V5	VCC=12V, VDD=5V	2.90	3.23	3.55	V
POWER ON RESET GENERATOR						
Charging current for POR Capacitor	ICPOR	VCC=12V, VDD=5V	-17.0	-13.5	-10.0	uA
POR threshold voltage	VTHPOR	CDLY=Sweep	2.3	2.5	2.7	V
Output high voltage	VPOH	VCC=12V, VDD=5V	4.5	–	VDD	V
Output low voltage	VPOL	VCC=12V, VDD=5V	0	–	0.5	V
Power on reset delay ⁽²⁾	TdPOR	CDLY=220nF	–	40	–	ms
CONTROL INPUT⁽³⁾						
Logic control input 1 HIGH voltage	VCTL1H	-	2.07	–	–	V
Logic control input 1 HIGH current	ICTL1H	CNTL1 = High	65	100	160	uA
Logic control input 1 LOW voltage	VCTL1L	-	–	–	1.43	V
Logic control input 1 LOW current	ICTL1L	CNTL1= Low	-200	-165	-130	uA

Electrical Characteristics (Continued)

(Ta=25°C, unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Units
RUNNING MODE CHECK						
Back-EMF threshold voltage ⁽²⁾	VBTH	–	65	80	95	mV
FG output high voltage	VFGH	–	4.5	–	–	V
FG output low voltage	VFGL	–	–	–	0.5	V
Running mode check	RM1	U=V=W=5V, N=100Hz	–	100	–	Hz
SPINDLE FG GENERATION						
FG frequency	FG	U,V,W=120° shift pulse(100Hz)	–	300	–	Hz
FG duty	DTFG	U,V,W=120° shift pulse(1KHz)	45	50	55	%
SPINDLE PWM CONTROL						
PWM high level input voltage ⁽²⁾	VSPMH	–	3.0	–	–	V
PWM low level input voltage ⁽²⁾	VSPML	–	–	–	2.0	V
High input current at PWMSP	IPSP1	PWMSP=100%	100	150	200	uA
CFSP voltage2(100% duty of PWMSP)	VSP2	PWMSP=100%	1.5	1.7	1.9	V
Low input current at PWMSP	IPSP2	PWMSP=0%	-200	-150	-100	uA
CFSP voltage1(0% duty of PWMSP)	VSP1	PWMSP=0%	3.1	3.3	3.5	V
CFSP voltage amplitude	VSPD	–	1.2	1.6	2.0	V
CFSP voltage3 (50% of PWMSP)	VSP3	PWMSP=50%	2.35	2.5	2.65	V
CFSP charging current	ICFSP1	PWMSP=0%, CFSP=2.5V	-200	-150	-100	uA
CFSP discharge current	ICFSP2	SPMSP=100%, CFSP=2.5V	100	150	200	uA
BRAKE						
CBrake output voltage	VBC	–	11.0	–	–	V
Brake output high voltage	VBH	(Test only)	–	VDD	–	V
Brake output low voltage	VBL	–	–	–	0.5	V

Electrical Characteristics (Continued)

(Ta=25°C, unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Units
SPINDLE PWM SOFT COMMUTATION						
PWM high level input voltage ⁽²⁾	V _{SFMH}	–	3.0	–	–	V
PWM low level input voltage ⁽²⁾	V _{SFML}	–	–	–	2.0	V
High input current at PWMSF	I _{FPF1}	PWMSF=100%	100	150	200	uA
CFSF voltage2(100% duty of PWMSF)	V _{SF2}	PWMSF=100%	2.60	2.75	2.90	V
Low input current at PWMSF	I _{PSF2}	PWMSF=0%	-200	-150	-100	uA
CFSF voltage1(0% duty of PWMSF)	V _{SF1}	PWMSF=0%	2.10	2.25	2.40	V
CFSF voltage amplitude	V _{SFD}	–	425	475	525	mV
CFSF voltage3 (50% of PWMSF)	V _{SF3}	PWMSF=50%	2.35	2.50	2.65	V
CFSF charging current	I _{CFSF1}	PWMSF=0%, CFSP=2.5V	-150	-100	-50	uA
CFSF discharge current	I _{CFSF2}	SPMSF=100%, CFSP=2.5V	50	100	150	uA
SPINDLE OUTPUT						
U saturation voltage_upper	V _{SU5U}	R _U ,R _V ,R _W =5Ω	–	–	0.9	V
V saturation voltage_upper	V _{SU5V}	R _U ,R _V ,R _W =5Ω	–	–	0.9	V
W saturation voltage_upper	V _{SU5W}	R _U ,R _V ,R _W =5Ω	–	–	0.9	V
U saturation voltage_lower	V _{SV5L}	R _U ,R _V ,R _W =5Ω	–	–	0.8	V
V saturation voltage_lower	V _{SU5L}	R _U ,R _V ,R _W =5Ω	–	–	0.8	V
W saturation voltage_lower	V _{SU5L}	R _U ,R _V ,R _W =5Ω	–	–	0.8	V
U output frequency	F _U	CNTL2=12KHz	–	1	–	KHz
V output frequency	F _V	CNTL2=12KHz	–	1	–	KHz
W output frequency	F _W	CNTL2=12KHz	–	1	–	KHz
Leakage current U upper	I _{ULQU}	–	-10	0	10	uA
Leakage current V upper	I _{VLQU}	–	-10	0	10	uA
Leakage current W upper	I _{WLQU}	–	-10	0	10	uA
Leakage current U lower	I _{ULQL}	–	-20	0	20	uA
Leakage current V lower	I _{VLQL}	–	-20	0	20	uA
Leakage current W lower	I _{WLQL}	–	-20	0	20	uA
Transconductance gain SPM	G _{MSP}	R _U ,R _V ,R _W =5Ω	–	0.85	–	A/V
CCOMP charging current1	I _{COMP1}	PWMSP=0%	-10	0	10	uA
CCOMP charging current2	I _{COMP2}	PWMSP=50%	-400	-300	-200	uA
CCOMP charging current3	I _{COMP3}	PWMSP=100%	-750	-630	-500	uA

Electrical Characteristics (Continued)

(Ta=25°C, unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Units
REGULATOR						
Adjustable PIN voltage	VADJ	–	1.29	1.31	1.33	V
Regulator output voltage	VREG	–	3.1	3.3	3.5	V
Regulator line regulation ⁽²⁾	RLINE	–	–	–	2.0	%
Regulator load regulation ⁽²⁾	RLOAD	I _O = 500mA	–	–	2.0	%
VCM PWM CONTROL						
High PWMH input current	IPWMH1	PWMH = 100%	36	48	60	uA
Low PWMH input current	IPWMH2	PWMH = 0%	-200	-150	-100	uA
High PWML input current	IPWML1	PWML = 100%	36	48	60	uA
Low PWML input current	IPWM2	PWML = 0%	-200	-150	-100	uA
PWMH high level input voltage ⁽²⁾	VPWMH1	–	3.0	–	–	V
PWMH low level input voltage ⁽²⁾	VPWMH2	–	–	–	2.0	V
PWML high level input voltage ⁽²⁾	VPWML1	–	3.0	–	–	V
PWML low level input voltage ⁽²⁾	VPWM2	–	–	–	2.0	V
CFVCM voltage1	VCFVC1	PWMH=100%,PWML=100%	5.56	5.95	6.34	V
CFVCM voltage5	VCFVC5	PWMH=50%,PWML=50%	3.80	4.00	4.20	V
CFVCM voltage9	VCFVC9	PWMH=0%,PWML=0%	1.66	2.05	2.44	V
PWM current ratio (VCM)	RPWM	–	–	64	–	–
PWMH current variation	IPPWM	–	1.2	1.3	1.4	mA
PWML current variation	IPPWM	–	17.7	20.3	22.3	uA
VCM PWM FILTER						
Maximum phase shift ⁽²⁾	DF	Measure at 500HZ, CFVCM=10nF	–	–	2	deg
Filter cut-off frequency ⁽²⁾	FCO	–	–	100	–	kHz
Filter attenuation at 1MHz ⁽²⁾	aFILTER	–	–	70	–	dB

Electrical Characteristics (Continued)

(Ta=25°C, unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Units
VCM REFERENCE VOLTAGE						
VCM reference voltage	VREF	CNTL3= High	3.8	4.0	4.2	V
VCM ERROR AMPLIFIER						
Amplifier output high	VEOH	–	10.8	–	–	V
Amplifier output low	VEOL	–	–	–	1.2	V
Short circuit current ⁽²⁾	IESC	–	8	–	–	mA
Input offset voltage ⁽²⁾	VOSE	–	-15	0	15	mV
Error amplifier open loop gain ⁽²⁾	AVE	–	–	80	–	dB
Unit gain bandwidth ⁽²⁾	BGE	–	–	2	–	MHz
VCM SENSE AMPLIFIER						
Amplifier output high	VSOH	–	10.8	–	–	V
Amplifier output low	VSOL	–	–	–	1.2	V
Short circuit current ⁽²⁾	ISSC	–	10	–	–	mA
Input offset voltage ⁽²⁾	VOSE	–	-15	0	15	mV
Unit gain bandwidth ⁽²⁾	BGS	–	–	2	–	MHz
Sense amplifier voltage gain1 ⁽²⁾	AVS1	GainSel=High	–	18	–	dB
Sense amplifier voltage gain2 ⁽²⁾	AVS2	GainSel=Low	–	6	–	dB
VCM POWER AMPLIFIER						
Power Amplifier gain	APO	–	–	22.9	–	dB
Power Amplifier output high voltage	VPOH	–	11.0	–	–	V
Power Amplifier output low voltage	VPOL	–	–	–	1.0	V
Input offset voltage ⁽²⁾	VOSE	–	-15	0	15	mV
Unit gain bandwidth ⁽²⁾	BGP	–	–	2	–	MHz

Electrical Characteristics (Continued)

(Ta=25°C, unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Units
VCM AMPLIFIER TOTAL						
VCM offset current	IOSVCM	PWMH=PWML=50% duty	-20	0	20	mA
VCM transconductance gain high	GM _{VH}	Gain _{sel} =Low	–	0.45	–	A/V
VCM transconductance gain low	GM _{VL}	Gain _{sel} =High	–	0.11	–	A/V
VCM+ saturation voltage lower	V _{VMS1}	R _{vcm} =15Ω	–	–	0.7	V
VCM- saturation voltage upper	V _{VMS2}	R _{vcm} =15Ω	–	–	0.7	V
VCM+ saturation voltage upper	V _{VMS3}	R _{vcm} =15Ω	–	–	0.7	V
VCM- saturation voltage lower	V _{VMS4}	R _{vcm} =15Ω	–	–	0.7	V
Leakage current power Amplifier1	IVCML1	–	-20	0	20	uA
RETRACT						
Min. operating voltage of CRET2	VCRET2	CRET2=Sweep	–	–	3.6	V
Source voltage	V _{SRC}	CRET2=5V	–	–	1.2	V
Sinking saturation voltage	V _{RTSAT}	CRET2=5V	–	–	0.7	V
Retract sinking current1	I _{RCT1}	R _{ret} =8.0KΩ	40	58	76	mA
Retract sinking current2	I _{RCT2}	R _{ret} =4.2KΩ	80	100	130	mA
Upper power transistor leakage	I _{LRET1}	–	-10	0	10	uA
Lower power transistor leakage	I _{LRET1}	–	-10	0	10	uA
THERMAL SHUT DOWN						
Operating temperature	T _{SD}	–	–	150	–	°C
Thermal hysteresis	T _{HYS}	–	–	30	–	°C

Notes:

1. No Spindle or VCM Load.
2. Guaranteed by Design.
3. Logic control input2 & 3 spec's are equal to logic control input1.

Application Information

Spindle Motor Drive Circuit

The FAN8620B is a combination chip consisting of spindle motor and voice coil motor designed for HDD system. According to the spindle conditions, the digital ASIC provides optimum control signals (Start-up, commutation, speed control, and commutation mode) to the FAN8620B.

Back-EMF (BEMF) signal of the spindle motor is fed back to ASIC via FG line. The MCLK and PWM signals are used to determine the commutation timing and to control the spindle speed, respectively.

Spindle Driver

The spindle includes both low and high side drivers (H-bridge) for a three-phase sensorless brushless DC motor. To reduce the saturation voltage, the vertical PNP transistor is used as the high side driver.

Frequency Generation (FG)

FG stands for Frequency Generation. It is the output signal to the ASIC.

It contains important information about the motor speed.

According to the FG frequency, the digital ASIC provides different motor clock signals to the motor drive IC via MCLK.

It checks the motor speed to send the VCM enable signal via CNTL3.

FG frequency (Hz), motor speed (rpm) and pole number are directly related as shown below in the three phase motor.

$$\text{FG frequency(Hz)} = \text{motor speed(rpm)} \times \text{pole number} / 2 \times 3 / 60$$

In a typical application,(8 pole motor)

$$\text{FG frequency} = 5400 \times 8 / 2 \times 3 / 60 = 1080 \text{ [Hz]}$$

MCLK & Mask

The MCLK is a motor clock used as the standard clock signal for the proper commutation timing of the spindle motor. It is supplied by the ASIC.

As shown in table 1, it has different delay times depending on the mode of the spindle.

	MCLK (Td)	MASK	Commutation
Start-up mode	2ms (External ASIC)	1ms	Hard
Acceleration mode	FG(n-1) / 2	FG(n-1) / 4	Hard
Running mode	FG(n-1) / 32	344.45ms	Soft

Table 1.

After the FG_Edge signal detection, the MCLK occurs after a half FG_Edge delay time in the acceleration mode and 1/ 32 FG_Edge delay time in the soft commutation mode.

Mask

When the coil current is abruptly changed in a short time interval, a spark voltage occurs. This spark voltage mixes with the FG output to give the wrong spindle information to the ASIC. To eliminate the spark voltage from the FG output, the masking circuit is needed.

$$V_{coil} = -L \frac{di}{dt}$$

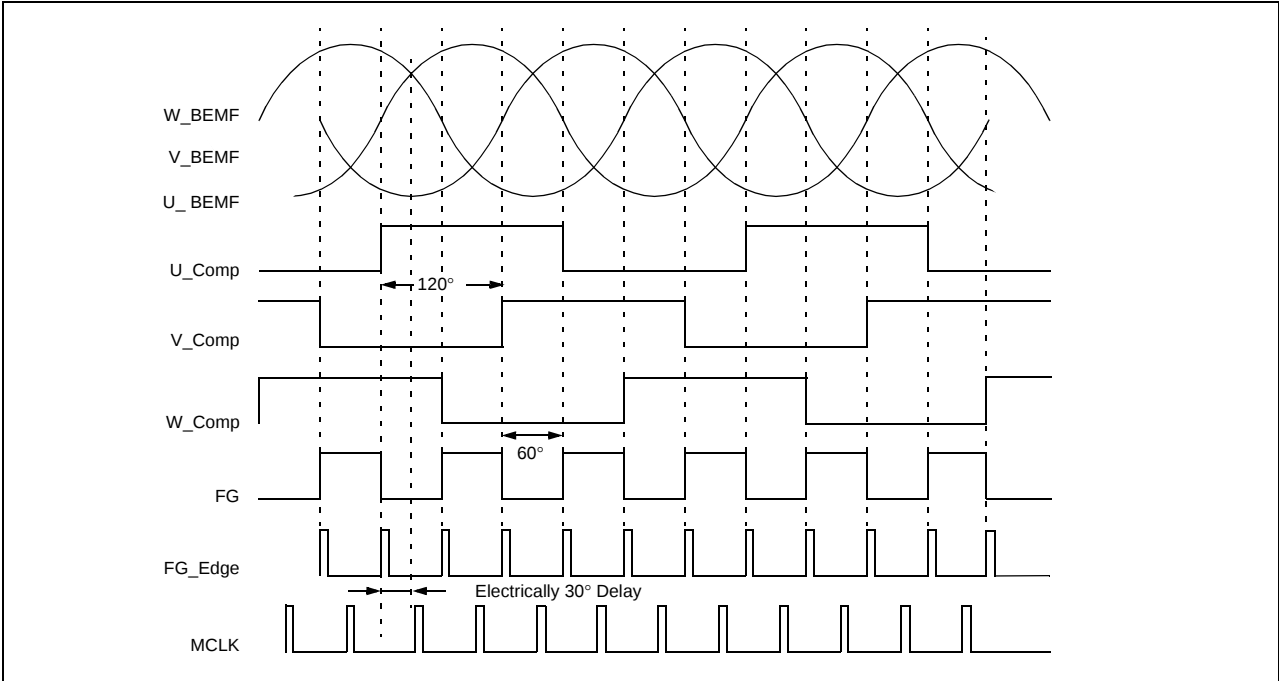


Figure 1. BEMF, FG, and MCLK in the acceleration mode

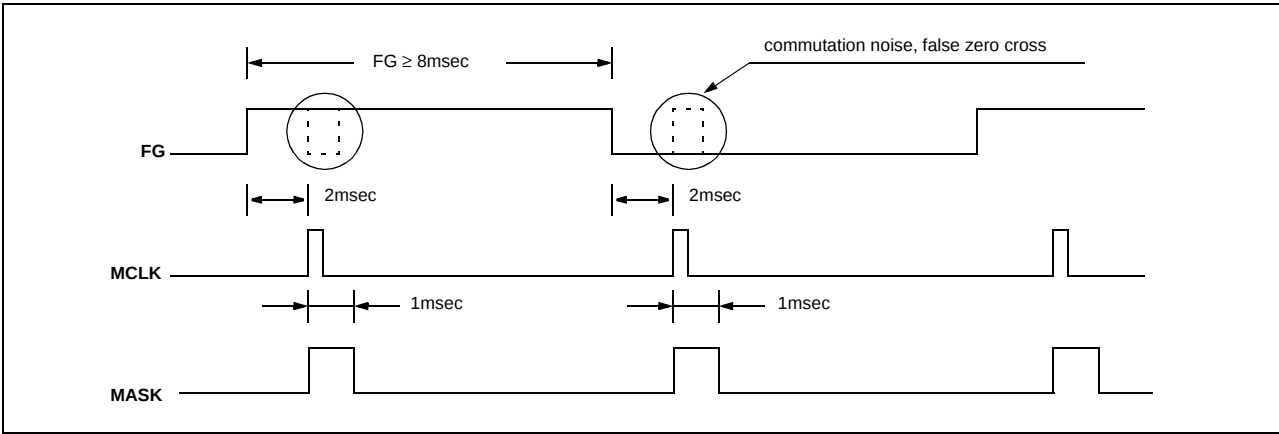


Figure 2. MCLK vs MASK in the start-up mode

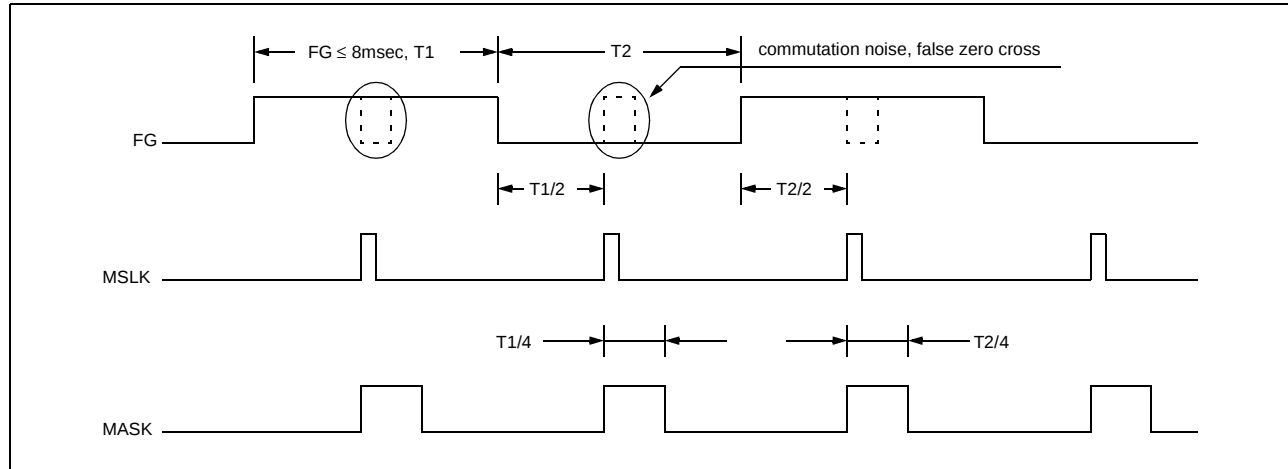
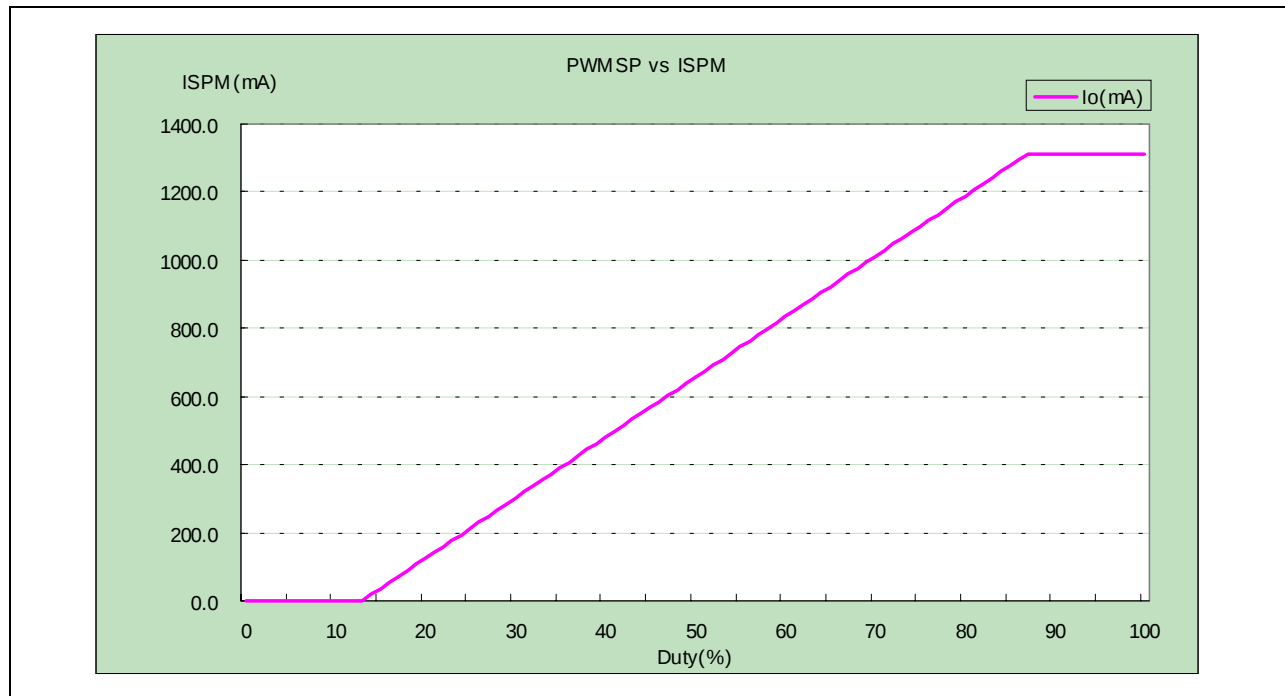


Figure 3. MCLK vs MASK in the acceleration mode

PWMDEC and Speed Control

Motor speed is measured by the ASIC via the FG output. The digital ASIC compares FG frequency with the target motor speed and sends the speed compensation signal to the PWMSP input of the FAN8620B. This PWM signal is internally filtered and is converted into DC voltage through the built-in PWM Decoder Filter. The analog output of the filter depends on the duty of the PWM signal. The filter is a 3rd order, low-pass filter. The first pole location of the filter is determined by the external capacitor connected to pin(48) CFSP.

$$I_{\text{spindle}} = (D - D_{\text{MIN}}) \cdot \frac{1}{R_{33} + R_{\text{METAL}}} \cdot \frac{0.5}{D_{\text{MAX}}} = (D - 0.13) \cdot \frac{1}{R_{33} + 0.074} \cdot \frac{0.5}{0.87}$$

Figure 4. Spindle current vs PWMSP duty variation ($R_{33} = 0.25\Omega$)

Start-up Mode

In the sensorless BLDC motor the Back-EMF is used to determine the rotor position.

At standstill condition, there is no Back-EMF voltage and no FG output. There is no information about the motor position.

To drive the spindle in the start-up mode, the digital ASIC sends the spindle enable signal via CNTL1 and supplies the HIGH or OPEN signal via CNTL2 to be used as commutation signal of the spindle motor.

The digital ASIC continuously provides HIGH or OPEN signal until the Back-EMF generated is large enough to produce the FG signal for the self commutation. During a fixed time, if the Back-EMF generated is too small and the spindle motor is not driven by the self commutation, the ASIC resets all signals and retries the spindle.

	CNTL1 ⁽¹⁾		CNTL2 ⁽²⁾	CNTL3 ⁽³⁾		GAINSEL	
	SPM driver	Brake	Commutation	VCM driver	Retract	SPM driver	VCM gain
High	1	0	Hard	1	0	Normal	0.11
Open (Floating)	0	0	Hard	0	0	x	x
Low	0	1	Soft	0	1	Start up ⁽⁵⁾ Hold	0.45

Notes:

1. CNTL1: Spindle motor control
2. CNTL2: commutation mode control
3. CNTL3: VCM control
4. "1": Enable; "0": disable;

Test only

Acceleration Mode

When the Back-EMF detected is large enough to determine motor position, the mode is changed from start-up to acceleration. The ASIC sends the optimum commutation timing signal via MCLK according to the FG input.

By using the Back-EMF, the spindle is self-commuted at acceleration and running modes. During the motor drive, the spindle motor is commuted at a point which is electrically 30° delayed after the FG_Edge.

Running Mode

The running mode is when the spindle motor speed arrives within $\pm 1\%$ of the target speed. The commutation mode, commutation delay time, MCLK delay time (Td) and masking time are changed at the running mode.

The spindle motor speed is controlled by PWM signal within $\pm 0.01\%$.

The soft commutation using the current slope of the motor may reduce audible noise, EMI (Electromagnetic Interference) and spark voltage which is generated on the motor coil commutation.

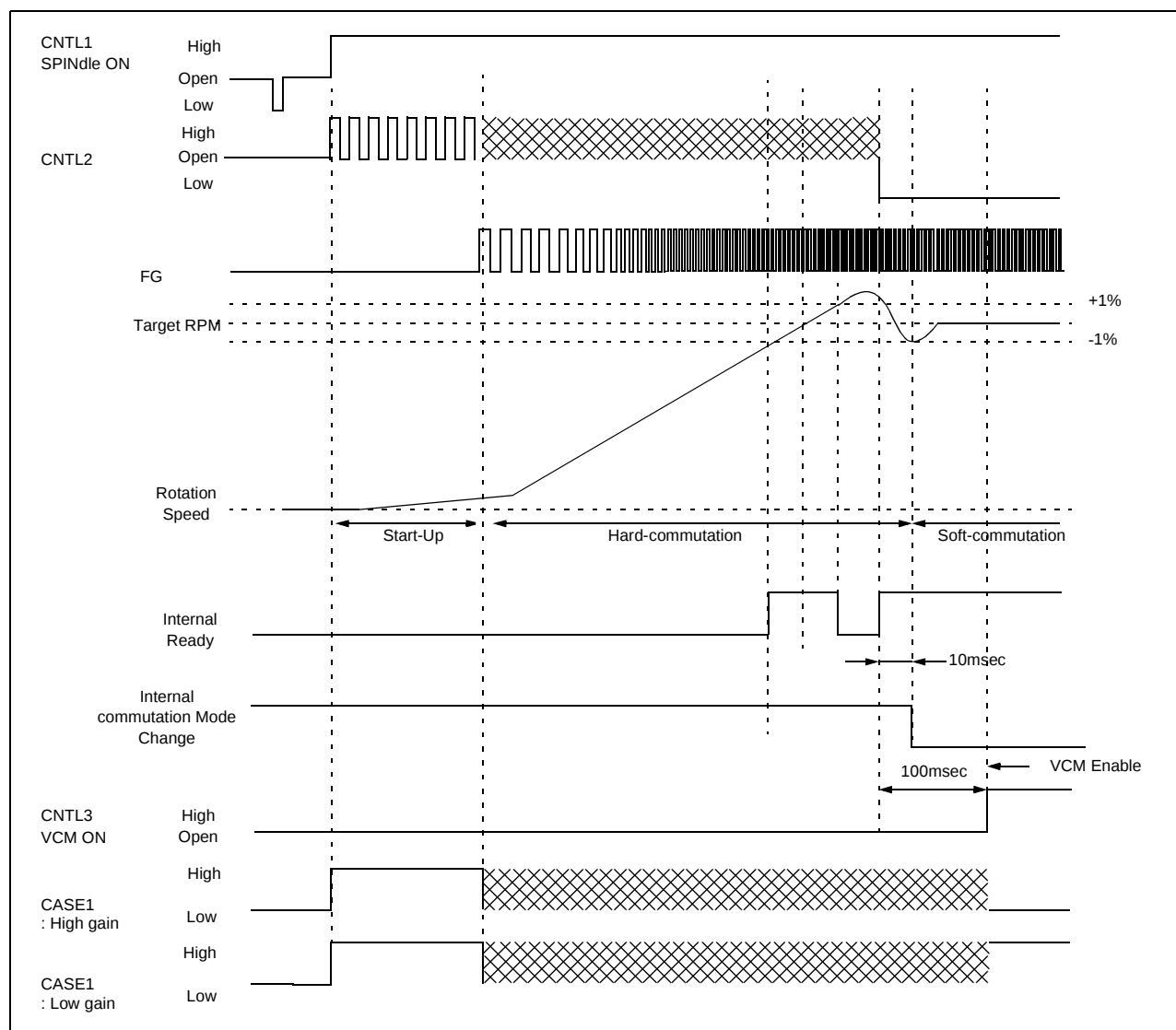


Figure 5. Motor start-up sequence

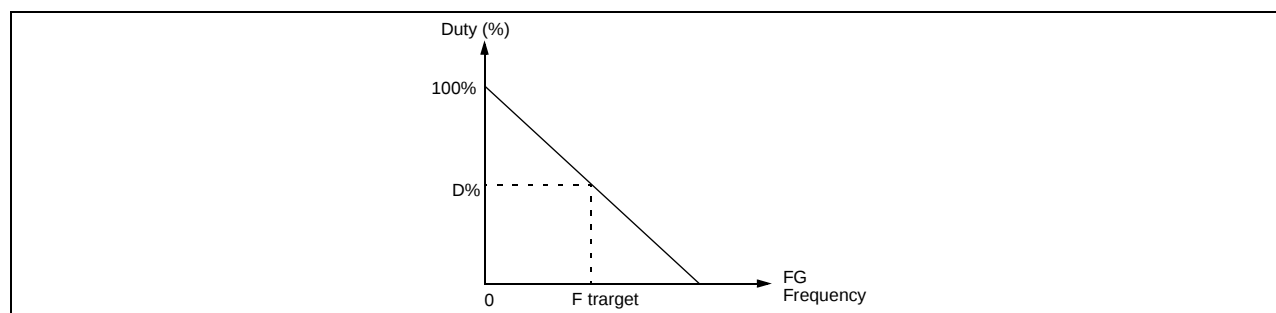


Figure 6. FG vs PWMSP duty variation

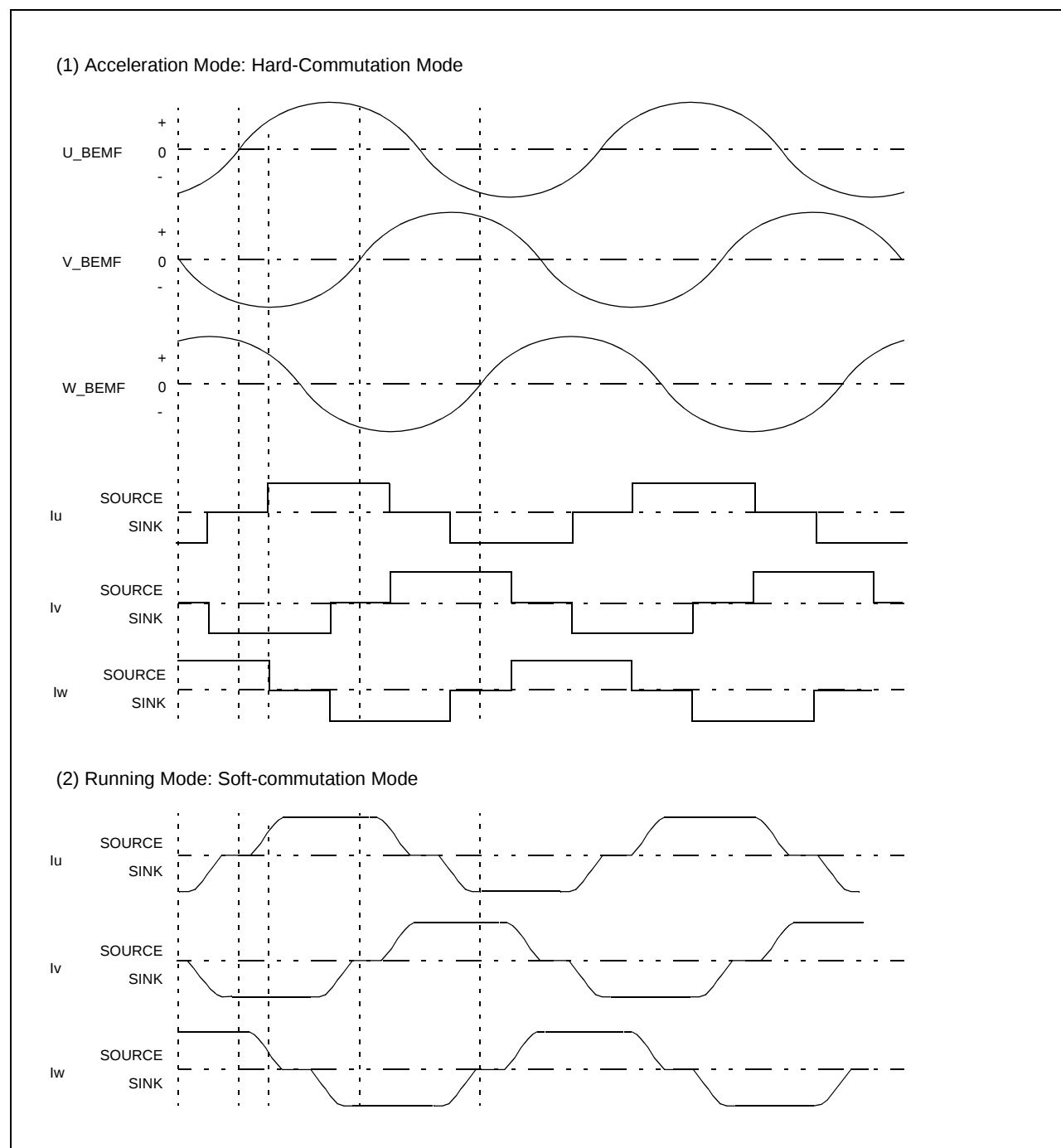


Figure 7. Acceleration and running the spindle motor

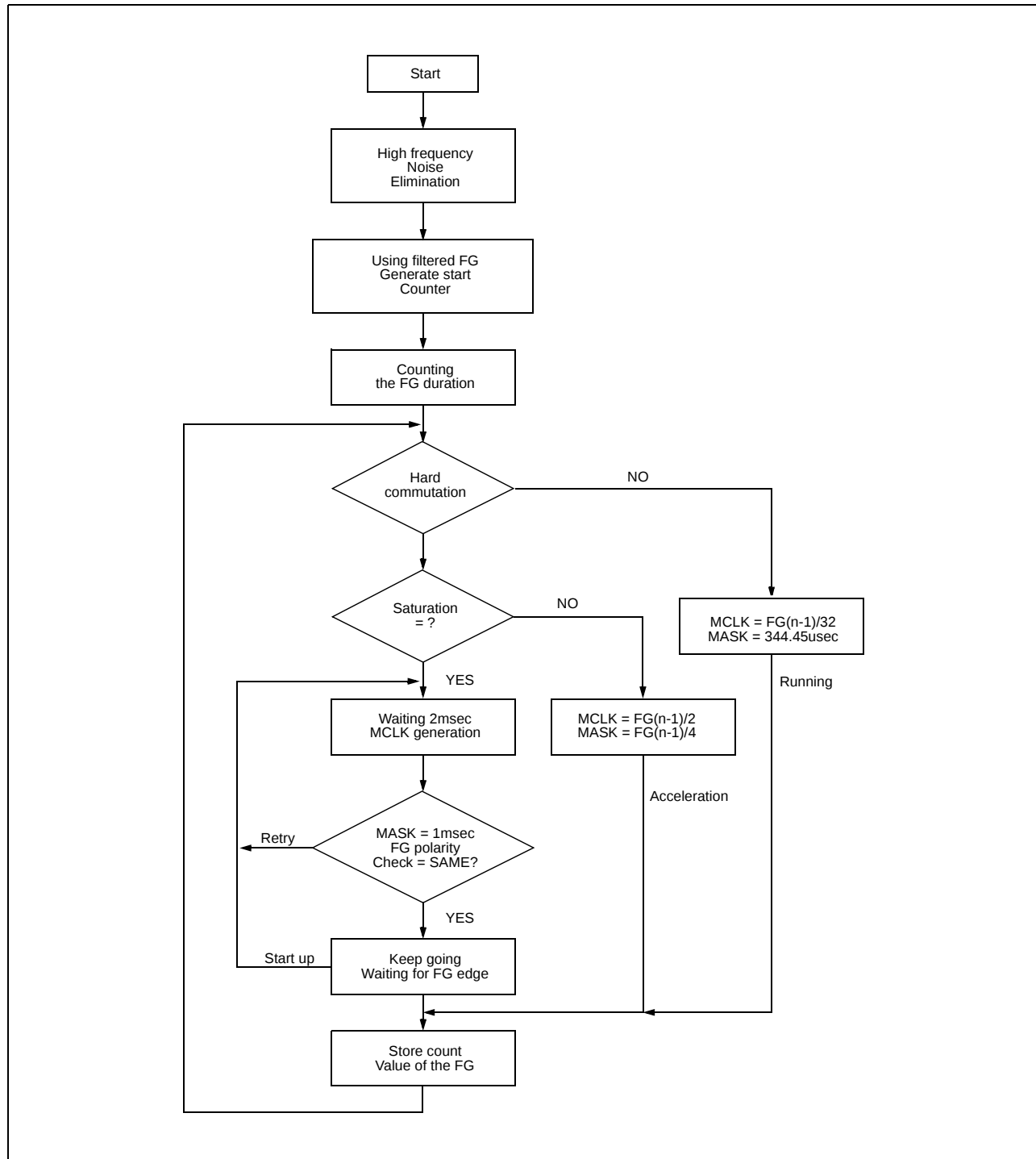


Figure 8. MCLK generation flow chart

The transconductance of VCM amplifier gain, G_m , is:

$$G_m = \frac{I_{VCM}}{V_{in}} = \frac{2 \cdot A_{error} \cdot A_{power} \cdot R_{25}}{2 \cdot R_{18} \cdot R_{sense} \cdot A_s \cdot A_{error} \cdot A_{power} + (R_{18} + R_{25})(Z_{VCM} + R_{sense})}$$

$$G_m = \frac{A_{loop}}{1 + A_{loop}} \left(\frac{R_{25}}{R_{18} R_{sense} A_s} \right)$$

$$A_{loop} = \frac{2 \cdot R_{18} \cdot A_s \cdot A_{error} \cdot A_{power}}{(R_{18} + R_{25})(Z_{VCM} + R_{sense})}$$

Therefore $A_{loop} \gg 1$,

$$G_m \cong \frac{R_{25}}{R_{18}} \cdot \frac{1}{R_{sense}} \cdot \frac{1}{A_s} \cdot 2$$

The transconductance (G_m) can be adjusted by selecting the external components R_{18} , R_{25} and sense resistor R_{sense} .

if $R_{18} = R_{25}$, $R_{sense} = 1\Omega$

GAINSEL = Low, $1 / A_s = 0.45$

$G_m = 0.45$

GAINSEL = High, $1 / A_s = 0.11$

$G_m = 0.11$

VCM current (I_{VCM}) is:

$$I_{motor} = 4 \times \left[(PWMH - 0.5) + \frac{1}{32}(PWML - 0.5) \right] \times \frac{R_{25}}{R_{18}} \times \frac{1}{R_{sense}} \times \frac{1}{A_s}$$

NOTES:

PWMH = 1 when 100% duty

PWMH = 0.5 when 50% duty

PWMH = 0 when 0% duty

The schematic diagram illustrates a retractor control system. Key components and connections include:

- Inputs:** Three inputs labeled U, V, and W are connected to a logic block.
- Reference and Control:** A Bandgap Reference and a Retractor Enable input are connected to the control logic.
- Amplification:** A 300x gain amplifier is used to amplify the control signal.
- Feedback Loop:** A feedback loop is formed by a 2K resistor and a 2V reference voltage.
- Current Source:** A current source I_{ref} is connected to the feedback loop.
- Output Stage:** The output of the amplifier is connected to a transistor (Q19) and a motor (VCM).
- Timing/Reset:** A 27 pin component is connected to the output stage and a capacitor (Cret2).

Figure 11. Retract block schematic

$$V_{ret} = \left[\left(\frac{2 \times R_{ret}}{R_{ret} + 2k} \right) - V_{BE, Q19} \right] [V]$$

Power Management Features

Low Power Interrupt:

The low power interrupt operation occurs when the power supply voltage (5V,12V) level drops below each threshold voltage. The threshold voltage (V_{th}) and time delay (T_{dly}) may be adjustable by the external component value.

$$T_{dly} = CDLY \frac{V_{th}}{I}, (V_{th} = 2.5V, I = 14\mu A)$$

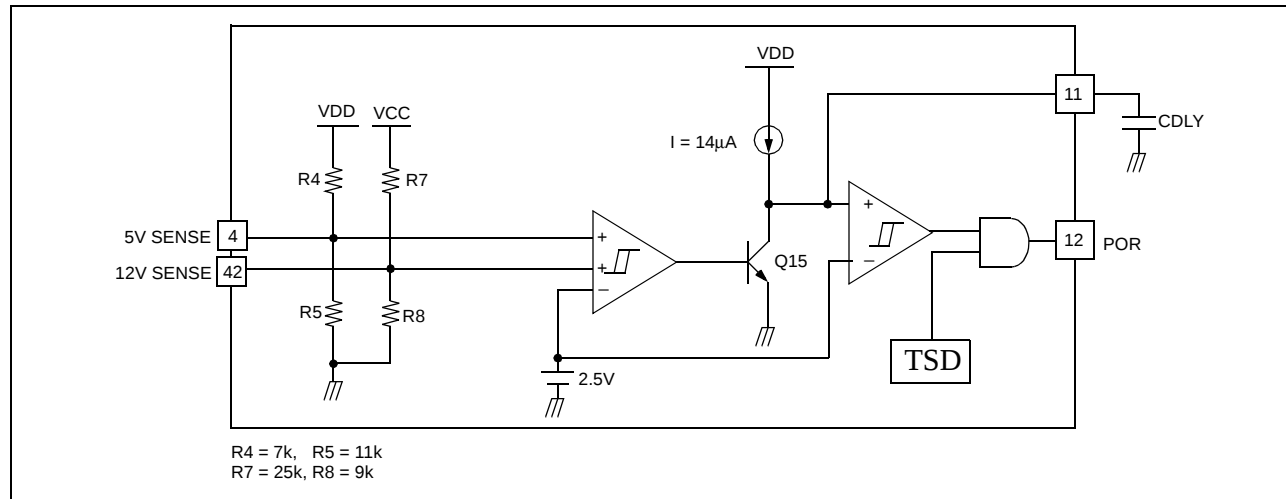


Figure 12. Power on reset block schematic

Power on Reset

The power-on reset circuit monitors the voltage level of both +5V or +12V power supplies and chip temperature (thermal shut down). The power-on reset circuit disables the spindle and VCM circuit when the power supply voltage level drops below the reference voltage.

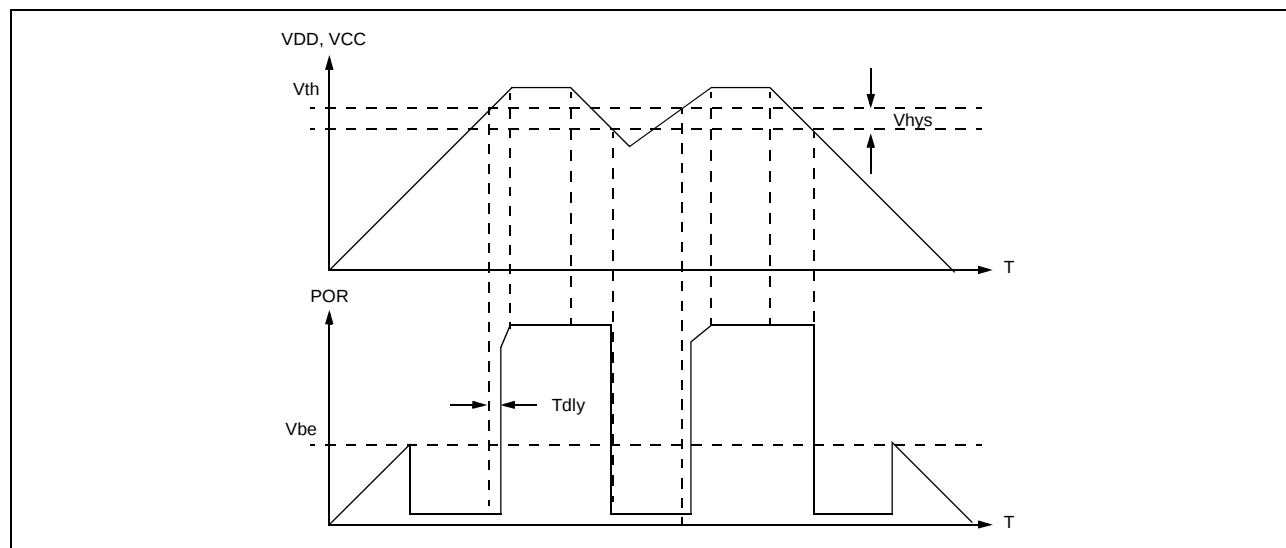


Figure 13. Power on reset function

$$V_{\text{hys}} = 53\text{mV}$$

$$V_{\text{DD}}; V_{\text{hys}}(5\text{V}) = \frac{R4 + R5}{R5} \times V_{\text{hys}}$$

$$V_{\text{DD}}; V_{\text{hys}}(12\text{V}) = \frac{R7 + R8}{R8} \times V_{\text{hys}}$$

Default (pin4, pin42 : not connected)

$$V_{\text{DD}}, t_{\text{h}} \cong 4.1\text{V}$$

$$V_{\text{CC}}, t_{\text{h}} \cong 9.4\text{V}$$

$$V_{\text{DD}}; V_{\text{hys}}(5\text{V}) = \frac{7\text{k} + 11\text{k}}{11\text{k}} \times 53\text{mV} \cong 90\text{mV}$$

$$V_{\text{DD}}; V_{\text{hys}}(12\text{V}) = \frac{25\text{k} + 9\text{k}}{9\text{k}} \times 53\text{mV} \cong 200\text{mV}$$

Regulator

The FAN8620B includes the voltage regulator for ASIC and other circuits. It consists bias circuit, the band gap reference and the external NPN power transistor. The regulator voltage can be adjusted by the external resistor, R3a, R3b.

$$V_{\text{REG}} = V_{\text{REF}} \left(1 + \frac{R3a}{R3b} \right), V_{\text{REF}} = 1.3\text{V}$$

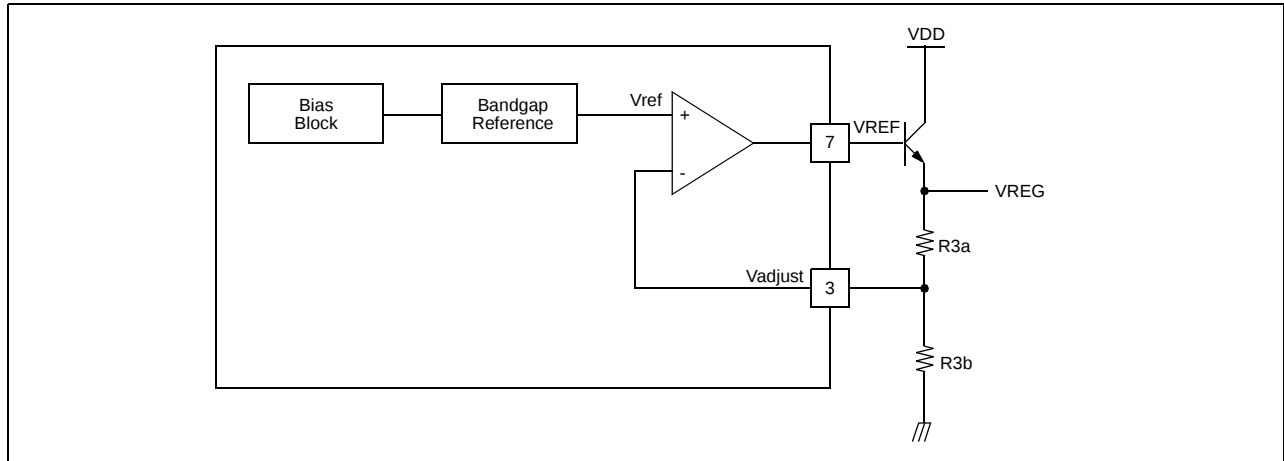


Figure 14. low drop regulator schematic

if R3a = 20k, R3b = 13k

$$V_{\text{REG}} = V_{\text{REF}} \left(1 + \frac{R3a}{R3b} \right) = 1.3 \times \left(1 + \frac{20\text{k}}{13\text{k}} \right) = 3.3\text{V}$$

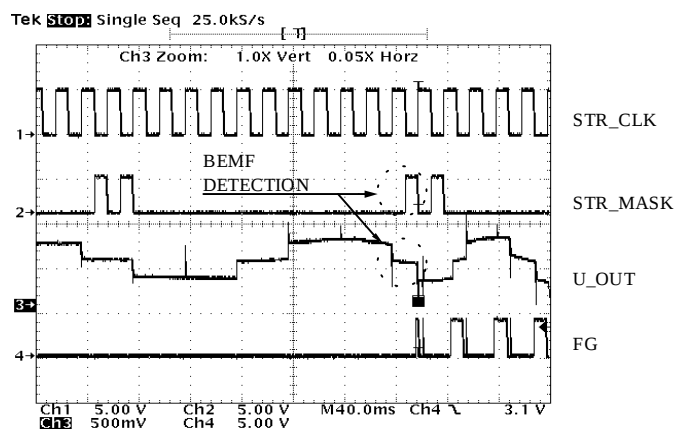


Figure 15. Start-up mode

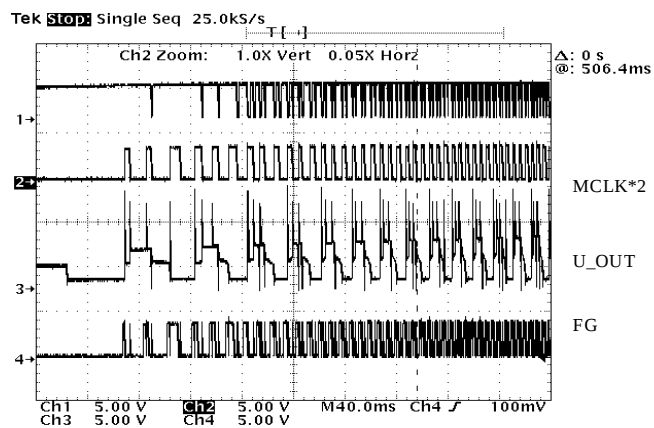


Figure 16. Acceleration mode 1

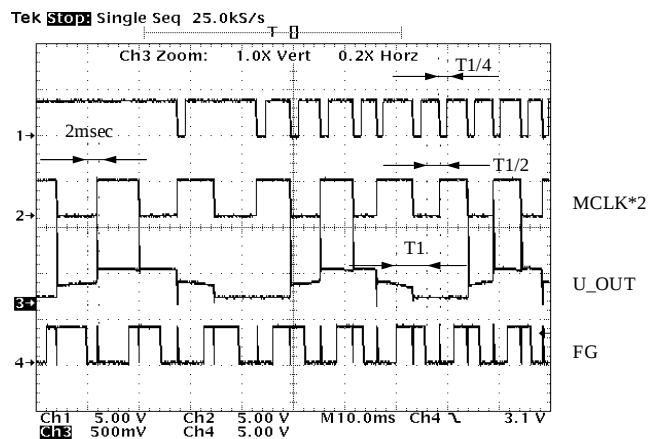


Figure 17. Acceleration mode 2

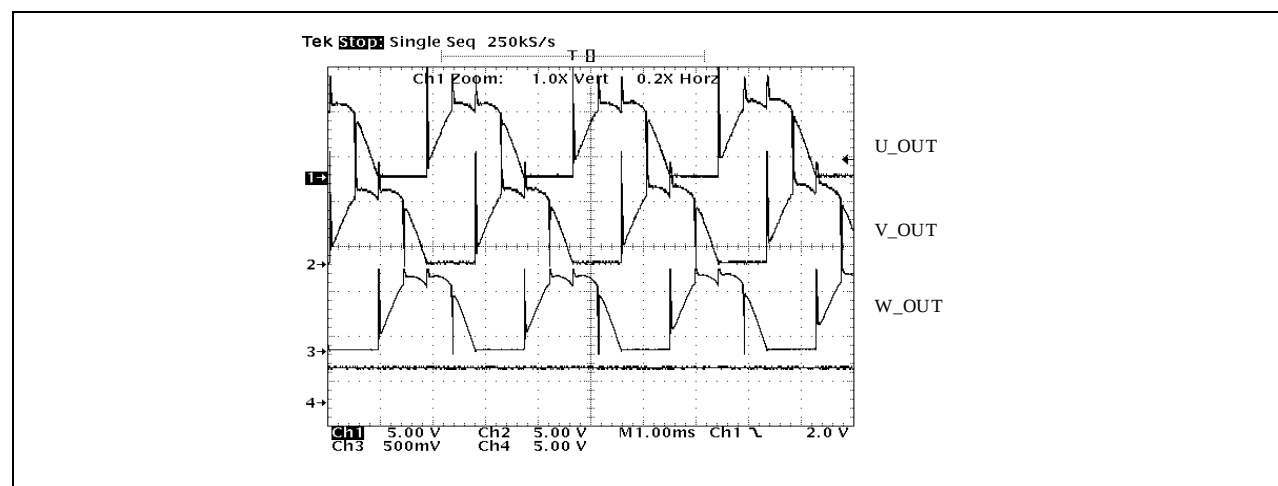


Figure 18. Output in hard-commutation mode

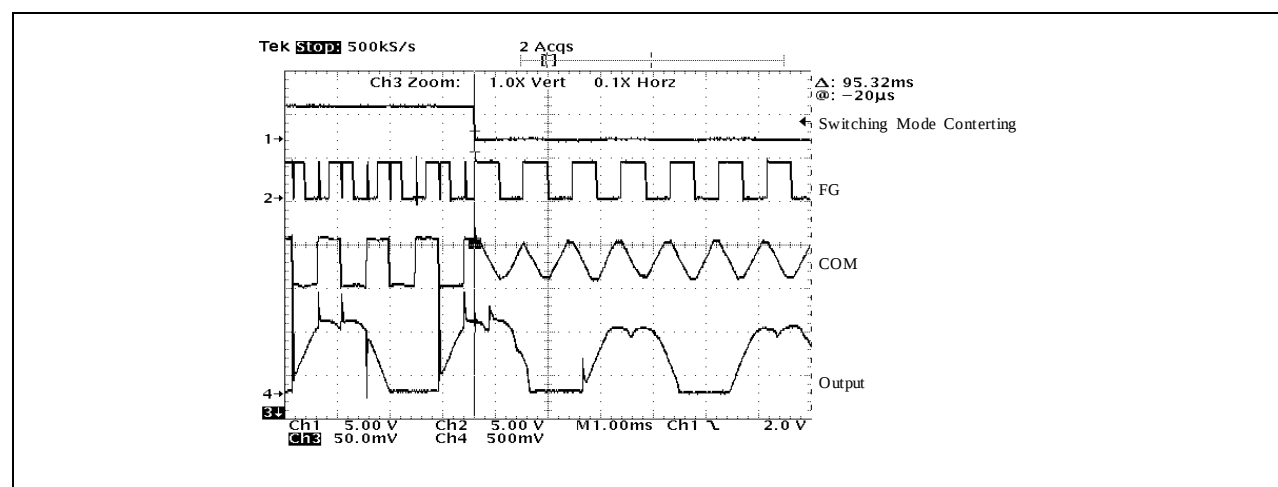


Figure 19. commutation mode converting

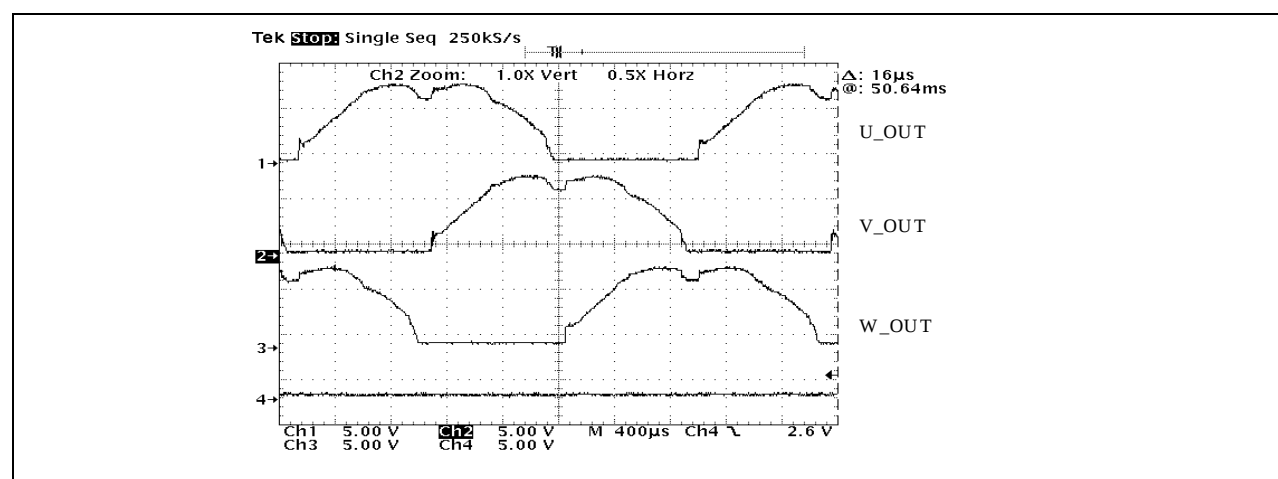


Figure 20. Soft-commutation mode

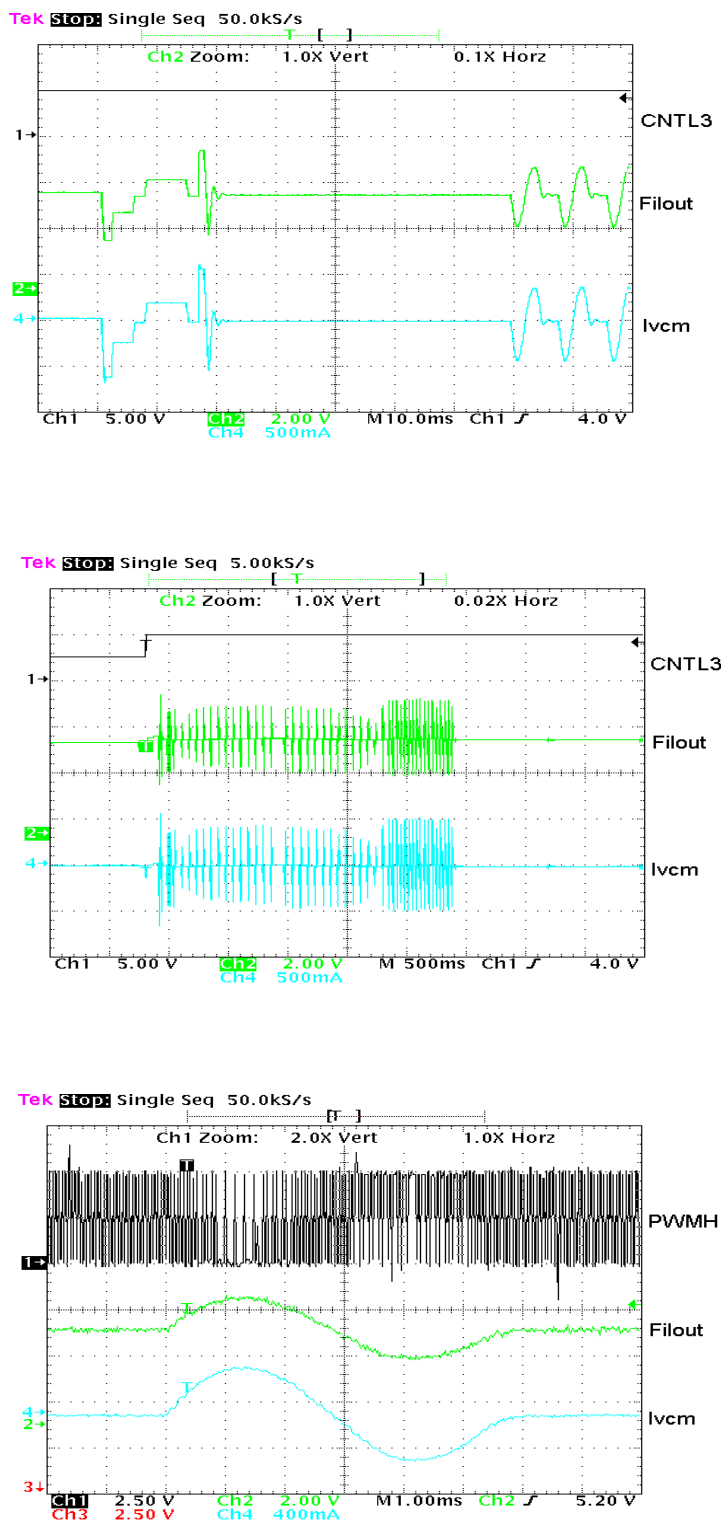


Figure 21. VCM recalibration flow

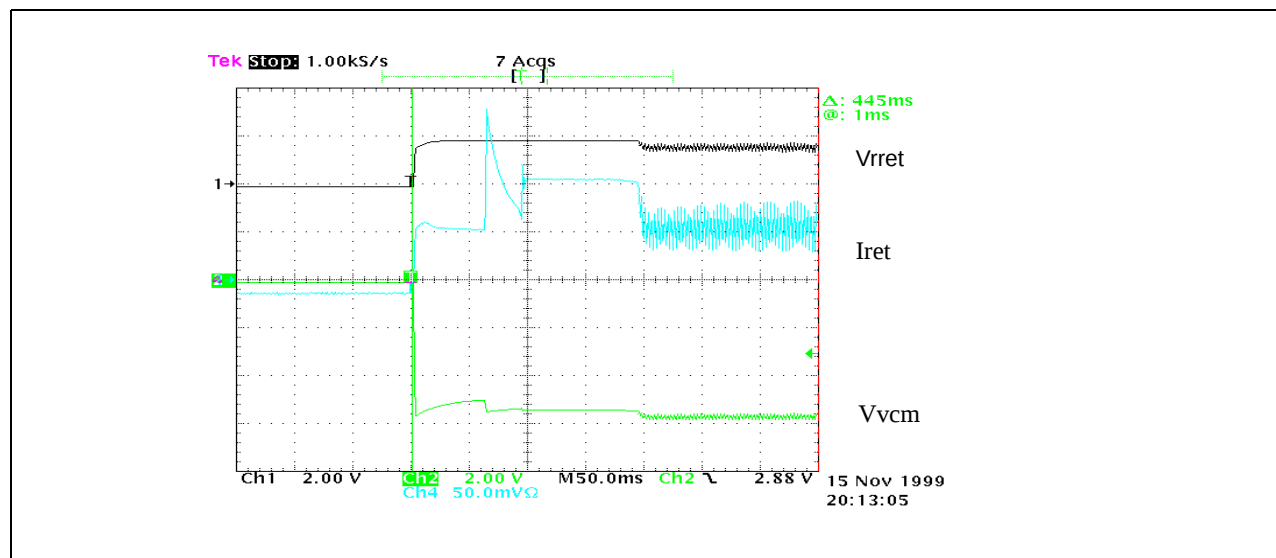
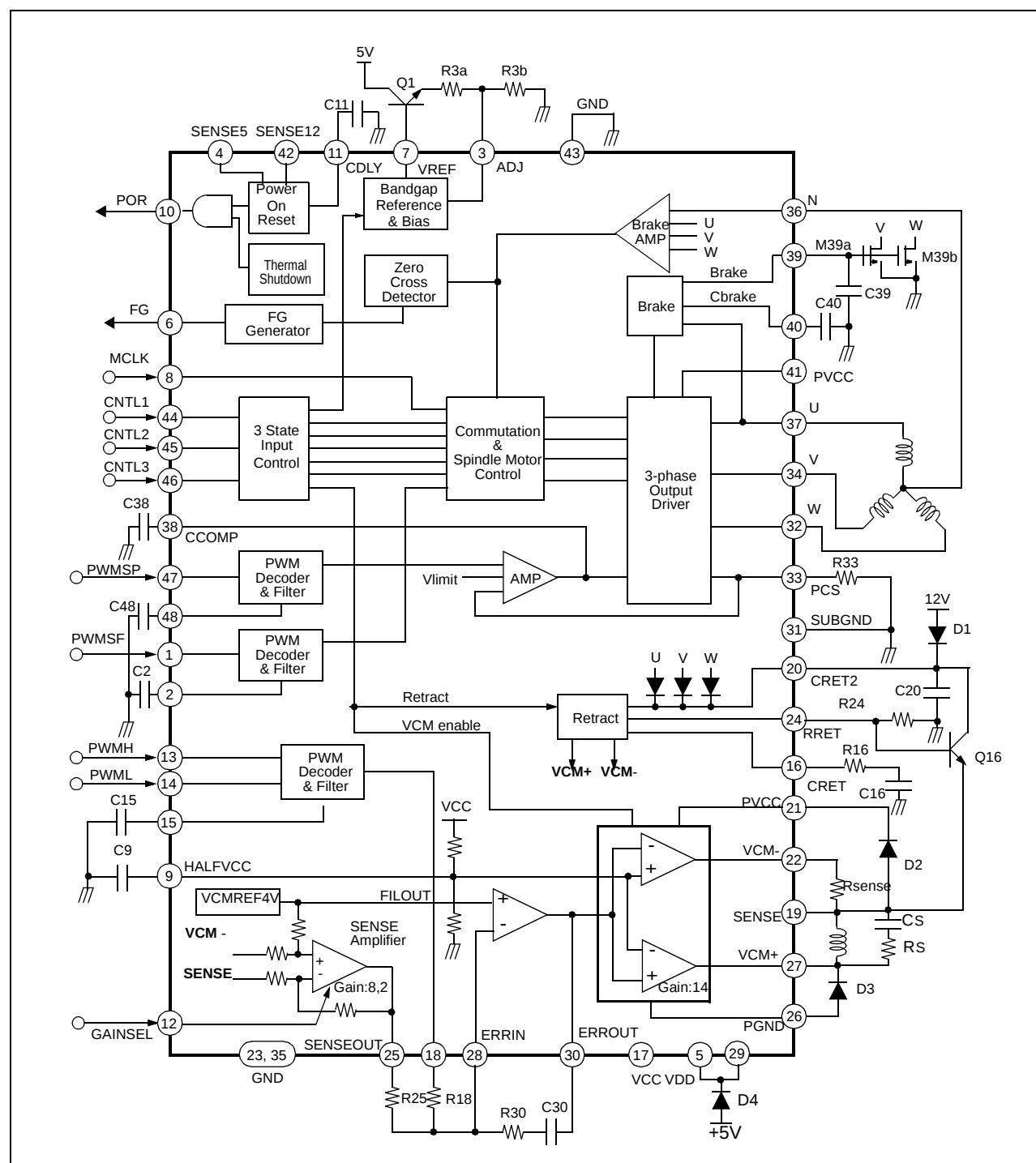
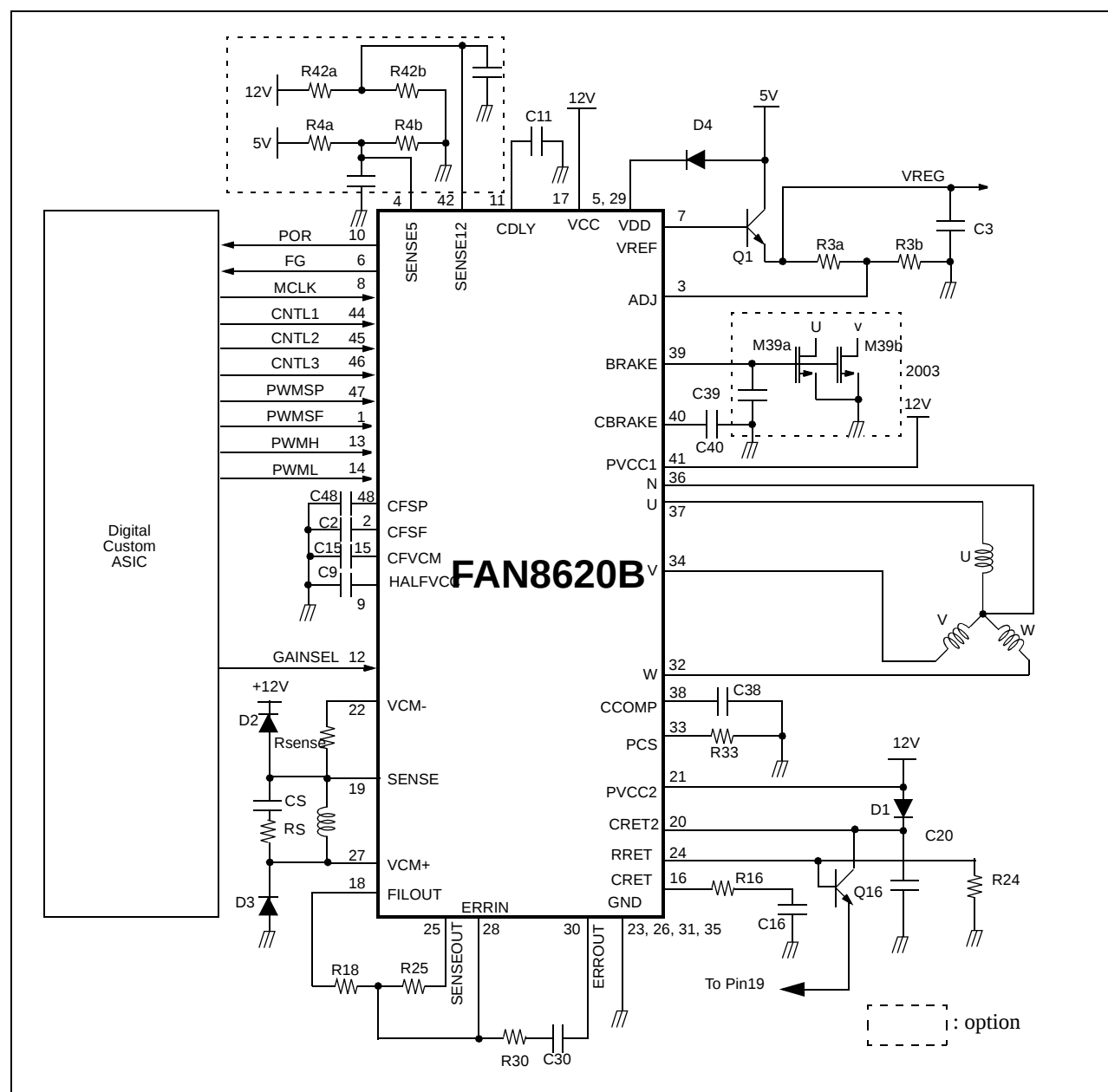


Figure 22. Retract & break at power off



Application Circuits



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