NB2308A

3.3 V Zero Delay Clock Buffer

The NB2308A is a versatile, 3.3 V zero delay buffer designed to distribute high−speed clocks. It is available in a 16 pin package. The part has an on−chip PLL which locks to an input clock presented on the REF pin. The PLL feedback is required to be driven to FBK pin, and can be obtained from one of the outputs. The input−to−output propagation delay is guaranteed to be less than 250 ps, and the output−to−output skew is guaranteed to be less than 200 ps.

The NB2308A has two banks of four outputs each, which can be controlled by the select inputs as shown in the Select Input Decoding Table. If all the output clocks are not required, Bank B can be three−stated. The select input also allows the input clock to be directly applied to the outputs for chip and system testing purposes.

Multiple NB2308A devices can accept the same input clock and distribute it. In this case the skew between the outputs of the two devices is guaranteed to be less than 700 ps.

The NB2308A is available in five different configurations (Refer to NB2308A Configurations Table). The NB2308AI1 is the base part, where the output frequencies equal the reference if there is no counter in the feedback path. The NB2308AI1H is the high−drive version of the −1 and the rise and fall times on this device are much faster.

The NB2308AI2 allows the user to obtain 2X and 1X frequencies on each output bank. The exact configuration and output frequencies depends on which output drives the feedback pin. The NB2308AI3 allows the user to obtain 4X and 2X frequencies on the outputs.

The NB2308AI4 enables the user to obtain 2X clocks on all outputs. Thus, the part is extremely versatile, and can be used in a variety of applications.

The NB2308AI5H is a high−drive version with REF/2 on both banks.

Features

- Zero Input − Output Propagation Delay, Adjustable by Capacitive Load on FBK Input
- Multiple Configurations − Refer to NB2308A Configurations Table
- Input Frequency Range: 15 MHz to 133 MHz
- Multiple Low−Skew Outputs
- Output−Output Skew Less than 200 ps
- Device−Device Skew Less than 700 ps
- Two banks of four outputs, three−stateable by two select inputs
- Less than 200 ps Cycle−to−Cycle Jitter
- Available in 16−pin SOIC and TSSOP Packages
- 3.3 V Operation
- Guaranteed Across Commercial and Industrial Temperature Ranges
- Advanced 0.35 μ CMOS Technology
- These are Pb−Free Devices

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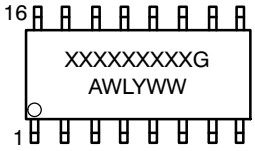
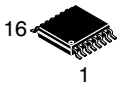
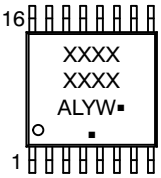
MARKING DIAGRAMS*

SOIC−16
D SUFFIX
CASE 751B





TSSOP−16
DT SUFFIX
CASE 948F



XXXX = Device Code
A = Assembly Location
WL, L = Wafer Lot
Y = Year
WW, W = Work Week
G or ▪ = Pb−Free Package
(Note: Microdot may be in either location)

*For additional marking information, refer to Application Note AND8002/D.

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 9 of this data sheet.

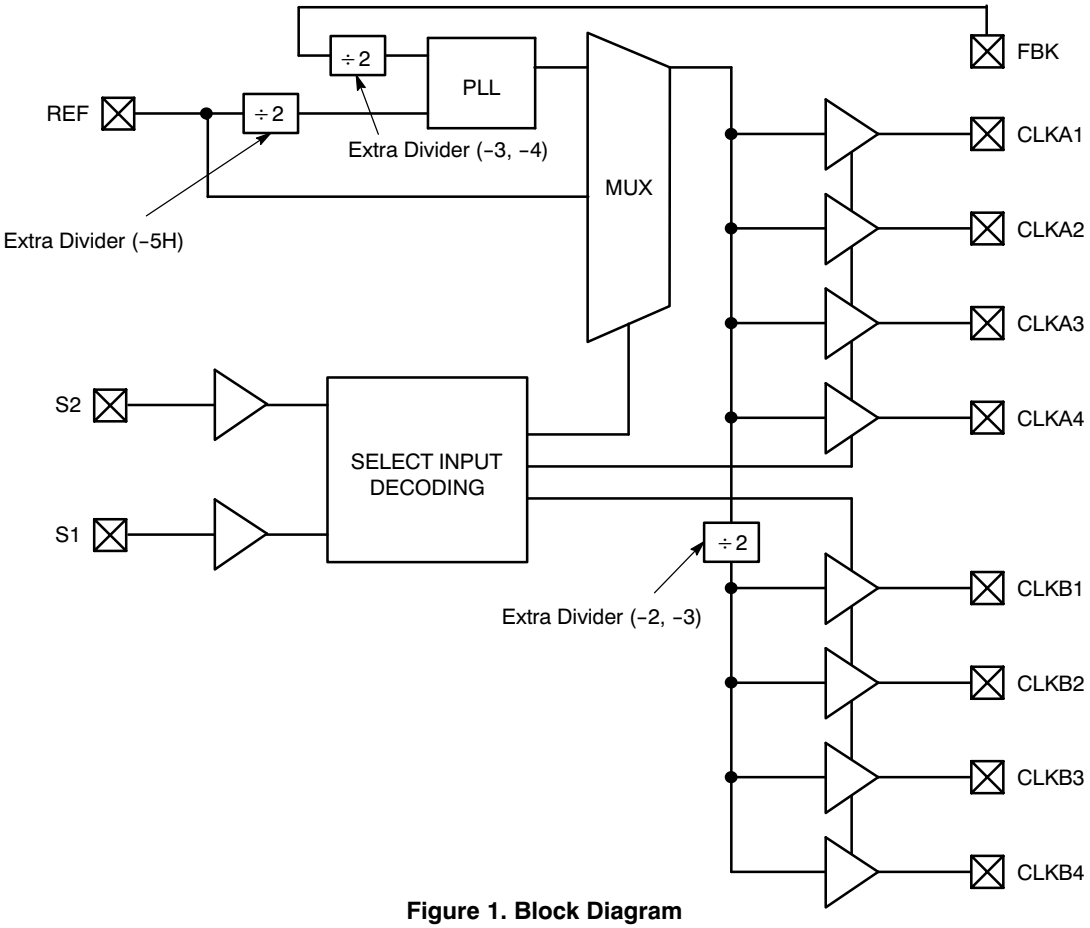


Figure 1. Block Diagram
(see Figures 11, 12, 13, 14 and 15 for device specific Block Diagrams)

Table 1. CONFIGURATIONS

Device	Feedback From	Bank A Frequency	Bank B Frequency
NB2308AI1	Bank A or Bank B	Reference	Reference
NB2308AI1H	Bank A or Bank B	Reference	Reference
NB2308AI2	Bank A	Reference	Reference ÷2
NB2308AI2	Bank B	2 X Reference	Reference
NB2308AI3	Bank A	2 X Reference	Reference or $\overline{\text{Reference}}$ (Note 1)
NB2308AI3	Bank B	4 X Reference	2 X Reference
NB2308AI4	Bank A or Bank B	2 X Reference	2 X Reference
NB2308AI5H	Bank A or Bank B	Reference ÷2	Reference ÷2

1. Output phase is indeterminant (0° or 180° from input clock). If phase integrity is required, use the NB2308AI2.

Table 2. SELECT INPUT DECODING

S2	S1	Clock A1 − A4	Clock B1 − B4	Output Source	PLL ShutDown
0	0	Three−state	Three−state	PLL	Y
0	1	Driven	Three−state	PLL	N
1	0	Driven (Note 2)	Driven	Reference	Y
1	1	Driven	Driven	PLL	N

2. Outputs inverted on 2308−2 and 2308−3 in bypass mode, S2 = 1 and S1 = 0.

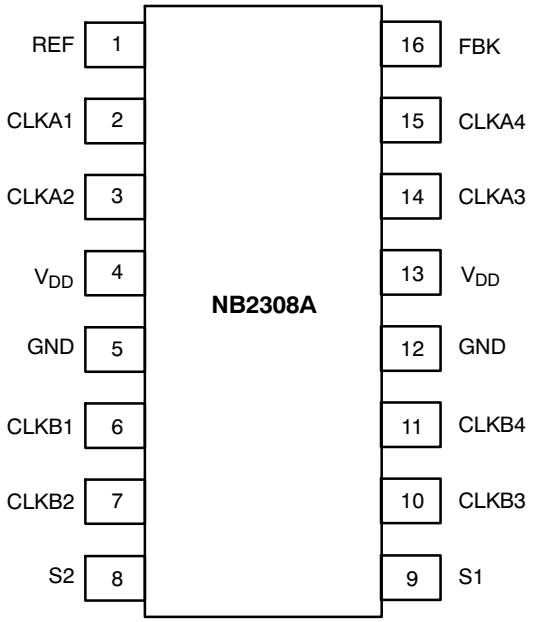


Figure 2. Pin Configuration

Table 3. PIN DESCRIPTION

Pin #	Pin Name	Description
1	REF (Note 3)	Input reference frequency, 5 V tolerant input.
2	CLKA1 (Note 4)	Buffered clock output, Bank A.
3	CLKA2 (Note 4)	Buffered clock output, Bank A.
4	V_{DD}	3.3 V supply.
5	GND	Ground.
6	CLKB1 (Note 4)	Buffered clock output, Bank B.
7	CLKB2 (Note 4)	Buffered clock output, Bank B.
8	S2 (Note 5)	Select input, bit 2.
9	S1 (Note 5)	Select input, bit 1.
10	CLKB3 (Note 4)	Buffered clock output, Bank B.
11	CLKB4 (Note 4)	Buffered clock output, Bank B.
12	GND	Ground.
13	V_{DD}	3.3 V supply.
14	CLKA3 (Note 4)	Buffered clock output, Bank A.
15	CLKA4 (Note 4)	Buffered clock output, Bank A.
16	FBK	PLL feedback input.

3. Weak pulldown.
4. Weak pulldown on all outputs.
5. Weak pullup on these inputs.

Table 4. MAXIMUM RATINGS

Parameter	Min	Max	Unit
Supply Voltage to Ground Potential	−0.5	+7.0	V
DC Input Voltage (Except REF)	−0.5	V_{DD} + 0.5	V
DC Input Voltage (REF)	−0.5	7	V
Storage Temperature	−65	+150	°C
Maximum Soldering Temperature (10 sec)		260	°C
Junction Temperature		150	°C
Static Discharge Voltage (per MIL−STD−883, Method 3015)		>2000	V

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

Table 5. OPERATING CONDITIONS

Parameter	Description		Min	Max	Unit
V_{DD}	Supply Voltage		3.0	3.6	V
T_A	Operating Temperature (Ambient Temperature)	Industrial Commercial	−40 0	85 70	°C
C_L	Load Capacitance, below 100 MHz			30	pF
C_L	Load Capacitance, from 100 MHz to 133 MHz			15	pF
C_{IN}	Input Capacitance (Note 6)			7	pF

6. Applies to both REF Clock and FBK.

Table 6. ELECTRICAL CHARACTERISTICS

Parameter	Description	Test Conditions		Min	Max	Unit
V_{IL}	Input LOW Voltage				0.8	V
V_{IH}	Input HIGH Voltage			2.0		V
I_{IL}	Input LOW Current	V_{IN} = 0 V			50.0	μA
I_{IH}	Input HIGH Current	V_{IN} = V_{DD}			100.0	μA
V_{OL}	Output LOW Voltage	I_{OL} = 8 mA (−1, −2, −3, −4) I_{OL} = 12 mA (−1H, −5H)			0.4	V
V_{OH}	Output HIGH Voltage	I_{OH} = −8 mA (−1, −2, −3, −4) I_{OH} = −12 mA (−1H, −5H)		2.4		V
I_{DD}	Supply Current (Note 7)	Unloaded outputs 100 MHz REF	−2, −3, −4		49	mA
		Select inputs at V_{DD} or GND	−1H, −5H		60	mA
		Unloaded outputs, 66 MHz REF (−1, −2, −3, −4)			34	mA
		Unloaded outputs, 33 MHz REF (−1, −2, −3, −4)			18	mA

7. Supply currents are measured for PLL−Bypass Mode (S2 = 1, S1 = 0).

Table 7. SWITCHING CHARACTERISTICS

Parameter	Description	Test Conditions	Min	Typ	Max	Unit
t_1	Output Frequency	30 pF load (all devices) 15 pF load (−1H, −5H) 15 pF load (−1, −2, −3, −4)	15 15 15		100 133.3 133.3	MHz
t_1	Duty Cycle = (t_2 / t_1) * 100 (all devices)	Measured at 1.4 V, F_{OUT} = < 66.66 MHz 30 pF load	40.0	50.0	60.0	%
		Measured at 1.4 V, F_{OUT} = < 50 MHz 15 pF load	45.0	50.0	55.0	
t_3	Output Rise Time (−1, −2, −3, −4)	Measured between 0.8 V and 2.0 V 30 pF load			2.20	ns
		Measured between 0.8 V and 2.0 V 15 pF load			1.50	
	Output Rise Time (−1H, −5H)	Measured between 0.8 V and 2.0 V 30 pF load			1.50	
t_4	Output Fall Time (−1, −2, −3, −4)	Measured between 2.0 V and 0.8 V 30 pF load			2.20	ns
		Measured between 0.8 V and 2.0 V 15 pF load			1.50	
	Output Fall Time (−1H, −5H)	Measured between 2.0 V and 0.8 V 30 pF load			1.25	
t_5	Output−to−Output Skew on same Bank (−1, −2, −3, −4)	All outputs equally loaded			200	ps
	Output−to−Output Skew (−1H, −5H)	All outputs equally loaded			200	
	Output Bank A−to−Output Bank B Skew (−1, −4, −5H)	All outputs equally loaded			200	
	Output Bank A−to−Output Bank B Skew (−2, −3)	All outputs equally loaded			400	
t_6	Delay, REF Rising Edge to FBK Rising Edge	Measured at V_{DD}/2		0	±250	ps
t_7	Device−to−Device Skew	Measured at V_{DD}/2 on the FBK pins of the device		0	700	ps
t_J	Cycle−to−Cycle Jitter (−1, −1H, −4, −5H)	Measured at 66.67 MHz, loaded outputs, 15 pF load			200	ps
		Measured at 66.67 MHz, loaded outputs, 30 pF load			200	
		Measured at 133.3 MHz, loaded outputs 15 pF load			100	
	Cycle−to−Cycle Jitter (−2, −3)	Measured at 66.67 MHz, loaded outputs, 30 pF load			400	
		Measured at 66.67 MHz, loaded outputs, 15 pF load			400	
t_{LOCK}	PLL Lock Time	Stable power supply, valid clock presented on REF and FBK pins			1.0	ms

Zero Delay and Skew Control

All outputs should be uniformly loaded to achieve Zero Delay between input and output.

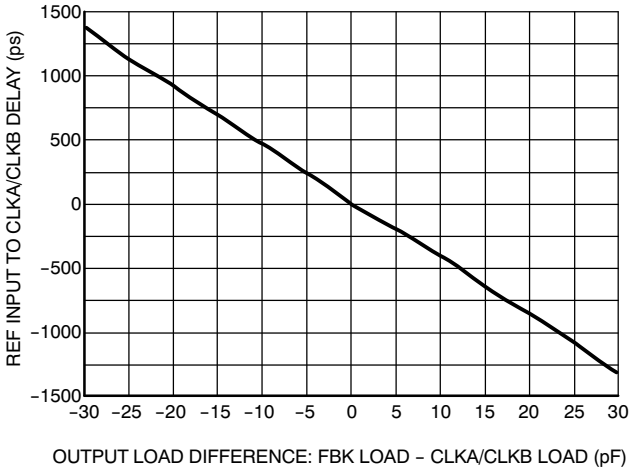


Figure 3. REF Input to CLKA/CLKB Delay vs. Difference in Loading between FBK Pin and CLKA/CLKB Pins

To close the feedback loop of the NB2308A, the FBK pin can be driven from any of the eight available output pins. The output driving the FBK pin will be driving a total load of 7 pF plus any additional load that it drives. The relative loading of this output (with respect to the remaining outputs) can adjust the input−output delay. This is shown in Figure 3.

For applications requiring zero input−output delay, all outputs including the one providing feedback should be equally loaded. If input−output delay adjustments are required, use the above graph to calculate loading differences between the feedback output and remaining outputs. For zero output−output skew, be sure to load outputs equally.

SWITCHING WAVEFORMS

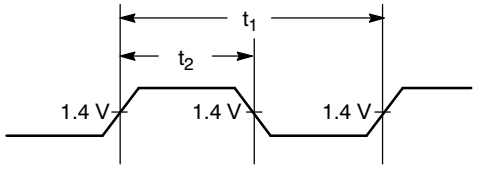


Figure 4. Duty Cycle Timing

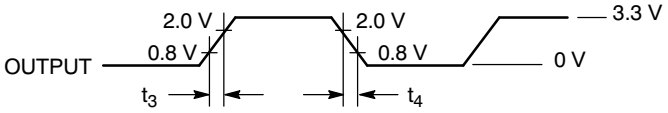


Figure 5. All Outputs Rise/Fall Time

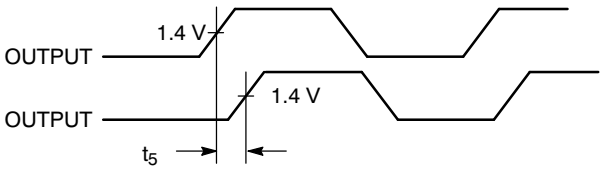


Figure 6. Output − Output Skew

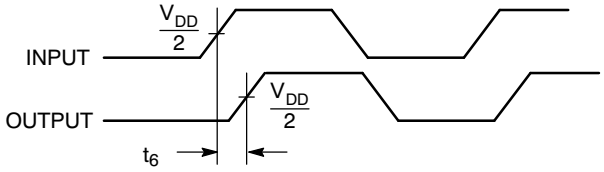


Figure 7. Input − Output Propagation Delay

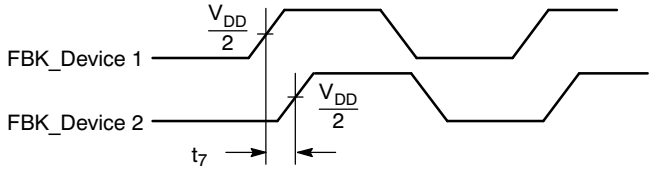


Figure 8. Device − Device Skew

TEST CIRCUITS

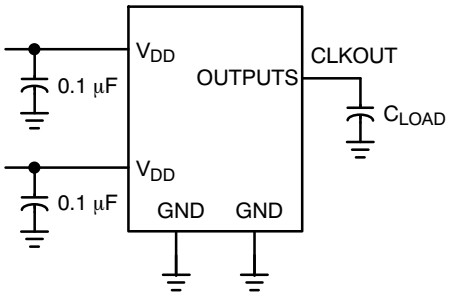


Figure 9. Test Circuit #1

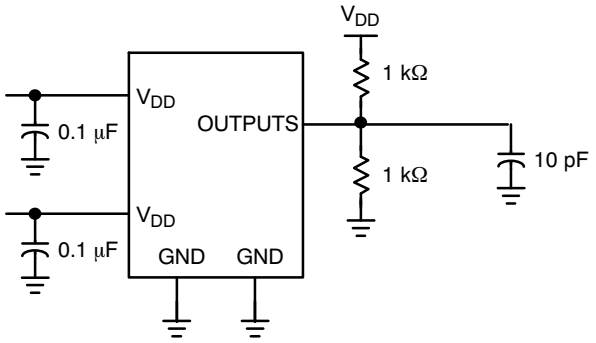


Figure 10. Test Circuit #2
For parameter t_8 (output slew rate) on –1H devices

BLOCK DIAGRAMS

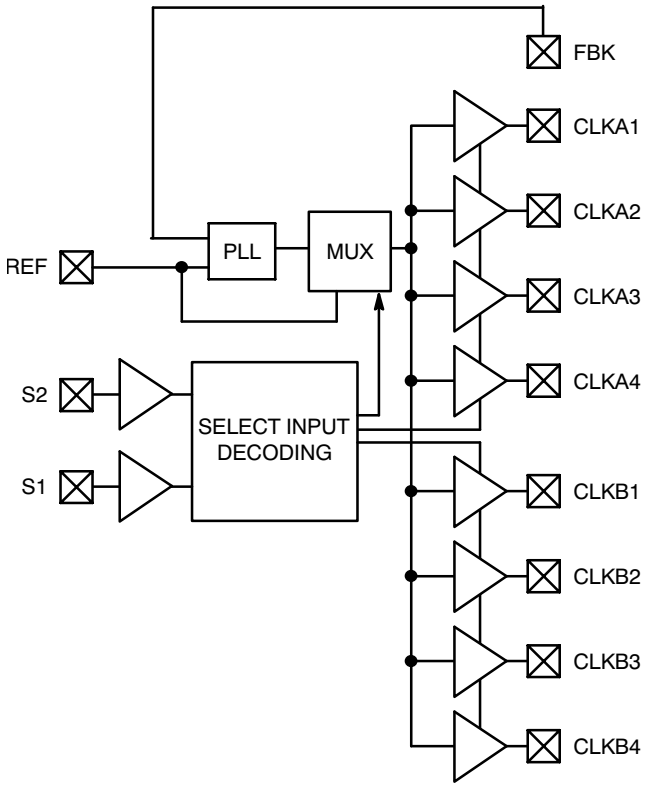


Figure 11. NB2308AI1 and NB2308AI1H

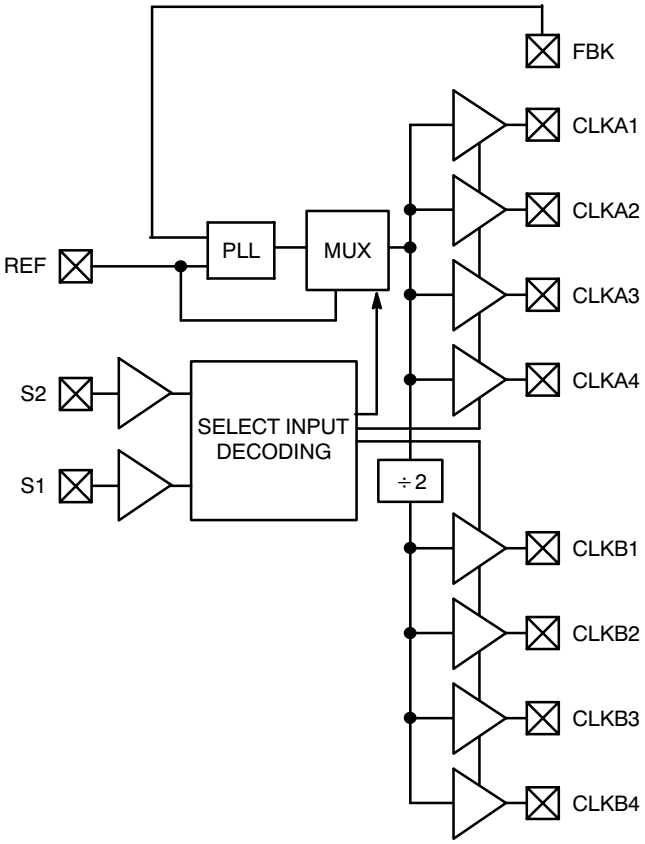


Figure 12. NB2308AI2

BLOCK DIAGRAMS

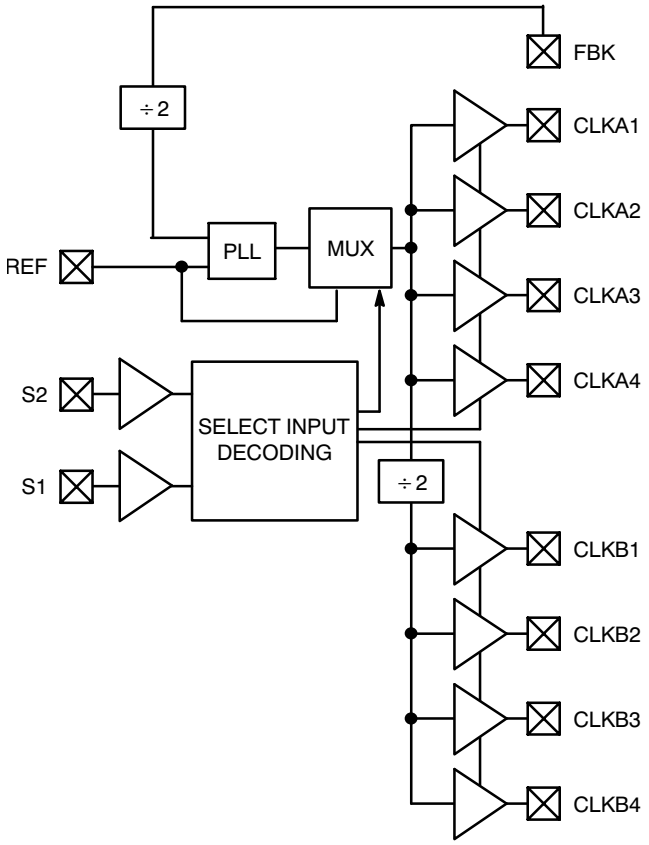


Figure 13. NB2308AI3

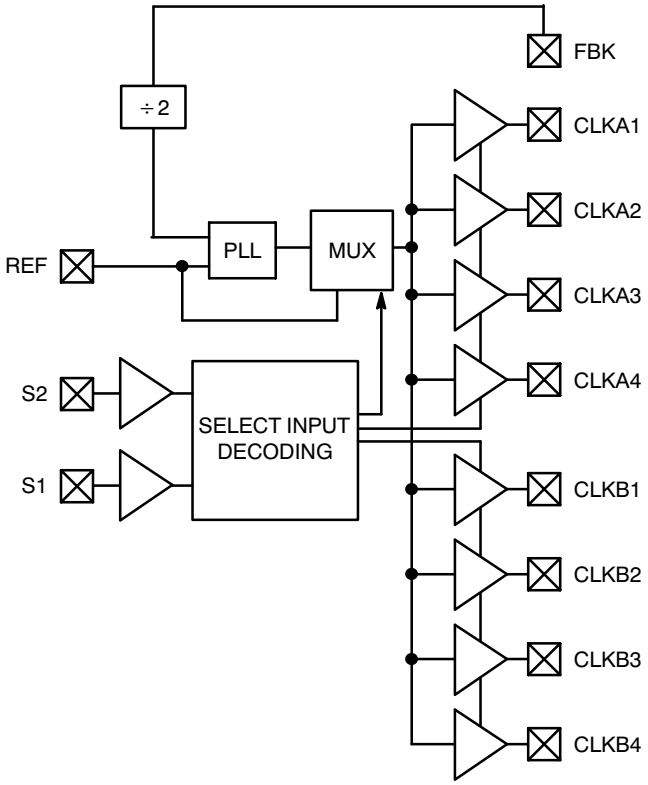


Figure 14. NB2308AI4

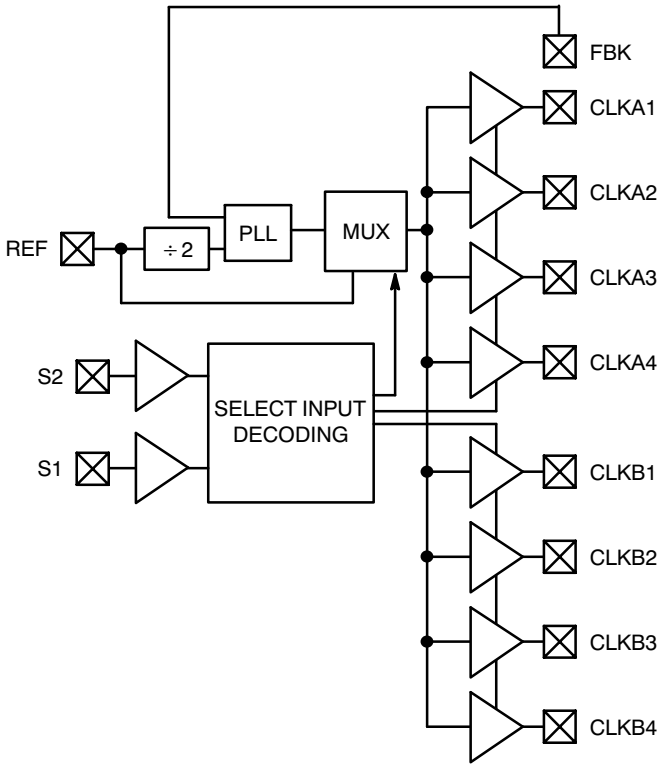


Figure 15. NB2308AI5H

ORDERING INFORMATION

Device	Marking	Operating Range	Package	Shipping†	Availability
NB2308AI1DG	2308AI1G	Industrial & Commercial	SOIC−16 (Pb−Free)	48 Units / Rail	*Now*
NB2308AI1DR2G	2308AI1G	Industrial & Commercial	SOIC−16 (Pb−Free)	2500 Tape & Reel	*Now*
NB2308AI1HDG	2308AI1HG	Industrial & Commercial	SOIC−16 (Pb−Free)	48 Units / Rail	*Now*
NB2308AI1HDR2G	2308AI1HG	Industrial & Commercial	SOIC−16 (Pb−Free)	2500 Tape & Reel	*Now*
NB2308AI1DTG	2308 AI1	Industrial & Commercial	TSSOP−16 (Pb−Free)	96 Units / Rail	*Now*
NB2308AI1DTR2G	2308 AI1	Industrial & Commercial	TSSOP−16 (Pb−Free)	2500 Tape & Reel	*Now*
NB2308AI1HDTG	2308 AI1H	Industrial & Commercial	TSSOP−16 (Pb−Free)	96 Units / Rail	*Now*
NB2308AI1HDTR2G	2308 AI1H	Industrial & Commercial	TSSOP−16 (Pb−Free)	2500 Tape & Reel	*Now*
NB2308AI2DG	2308AI2G	Industrial & Commercial	SOIC−16 (Pb−Free)	48 Units / Rail	*Now*
NB2308AI2DR2G	2308AI2G	Industrial & Commercial	SOIC−16 (Pb−Free)	2500 Tape & Reel	*Now*
NB2308AI2DTG	2308 AI2	Industrial & Commercial	TSSOP−16 (Pb−Free)	96 Units / Rail	*Now*
NB2308AI2DTR2G	2308 AI2	Industrial & Commercial	TSSOP−16 (Pb−Free)	2500 Tape & Reel	*Now*
NB2308AI2HDG	2308AI2HG	Industrial & Commercial	SOIC−16 (Pb−Free)	48 Units / Rail	*Now*
NB2308AI2HDR2G	2308AI2HG	Industrial & Commercial	SOIC−16 (Pb−Free)	2500 Tape & Reel	*Now*
NB2308AI2HDTG	2308 AI2H	Industrial & Commercial	TSSOP−16 (Pb−Free)	96 Units / Rail	*Now*
NB2308AI2HDTR2G	2308 AI2H	Industrial & Commercial	TSSOP−16 (Pb−Free)	2500 Tape & Reel	*Now*
NB2308AI3DG	2308AI3G	Industrial & Commercial	SOIC−16 (Pb−Free)	48 Units / Rail	*Now*
NB2308AI3DR2G	2308AI3G	Industrial & Commercial	SOIC−16 (Pb−Free)	2500 Tape & Reel	*Now*
NB2308AI3DTG	2308 AI3	Industrial & Commercial	TSSOP−16 (Pb−Free)	96 Units / Rail	*Now*
NB2308AI3DTR2G	2308 AI3	Industrial & Commercial	TSSOP−16 (Pb−Free)	2500 Tape & Reel	*Now*
NB2308AI4DG	2308AI4G	Industrial & Commercial	SOIC−16 (Pb−Free)	48 Units / Rail	*Now*
NB2308AI4DR2G	2308AI4G	Industrial & Commercial	SOIC−16 (Pb−Free)	2500 Tape & Reel	*Now*
NB2308AI4DTG	2308 AI4	Industrial & Commercial	TSSOP−16 (Pb−Free)	96 Units / Rail	*Now*
NB2308AI4DTR2G	2308 AI4	Industrial & Commercial	TSSOP−16 (Pb−Free)	2500 Tape & Reel	*Now*

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

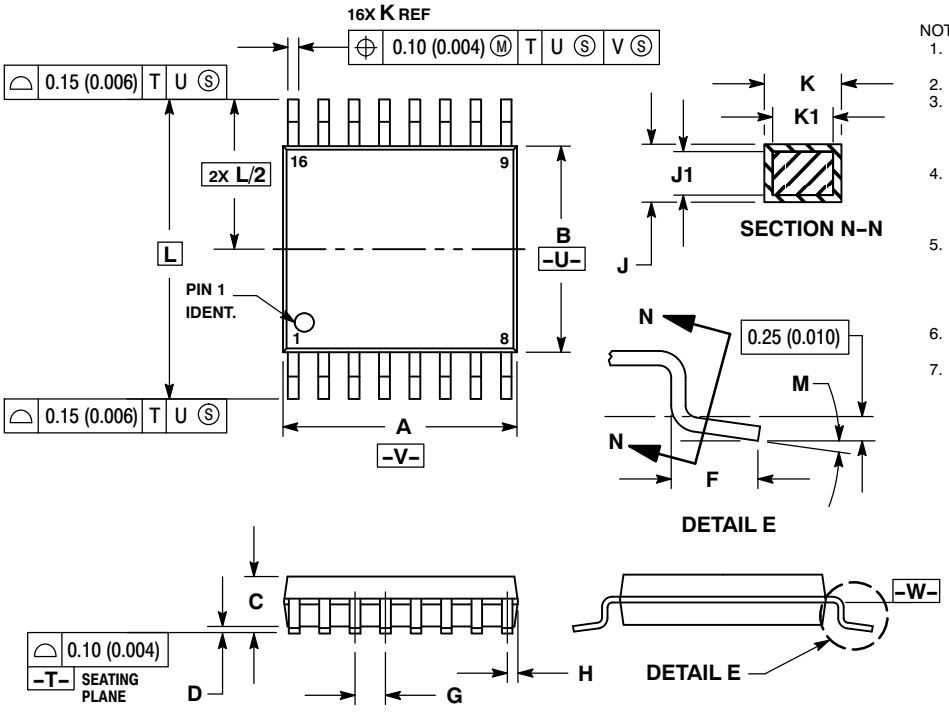
ORDERING INFORMATION

Device	Marking	Operating Range	Package	Shipping†	Availability
NB2308AI5HDG	2308AI5HG	Industrial & Commercial	SOIC−16 (Pb−Free)	48 Units / Rail	*Now*
NB2308AI5HDR2G	2308AI5HG	Industrial & Commercial	SOIC−16 (Pb−Free)	2500 Tape & Reel	*Now*
NB2308AI5HDTG	2308 AI5H	Industrial & Commercial	TSSOP−16 (Pb−Free)	96 Units / Rail	*Now*
NB2308AI5HDTR2G	2308 AI5H	Industrial & Commercial	TSSOP−16 (Pb−Free)	2500 Tape & Reel	*Now*

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

PACKAGE DIMENSIONS

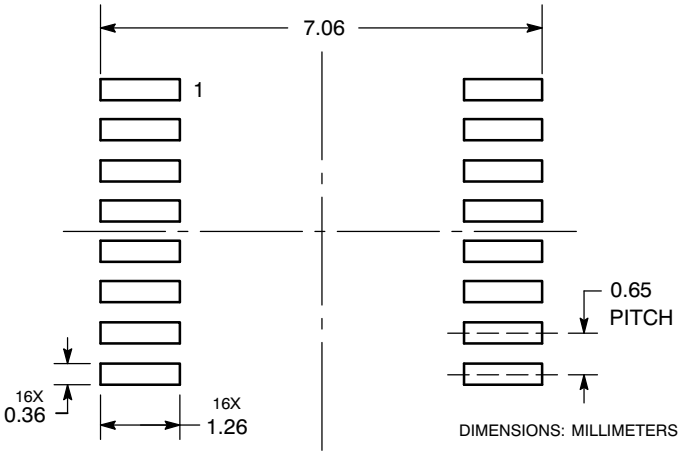
TSSOP−16
CASE 948F−01
ISSUE B



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE −W−.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.18	0.28	0.007	0.011
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0 °	8 °	0 °	8 °

SOLDERING FOOTPRINT

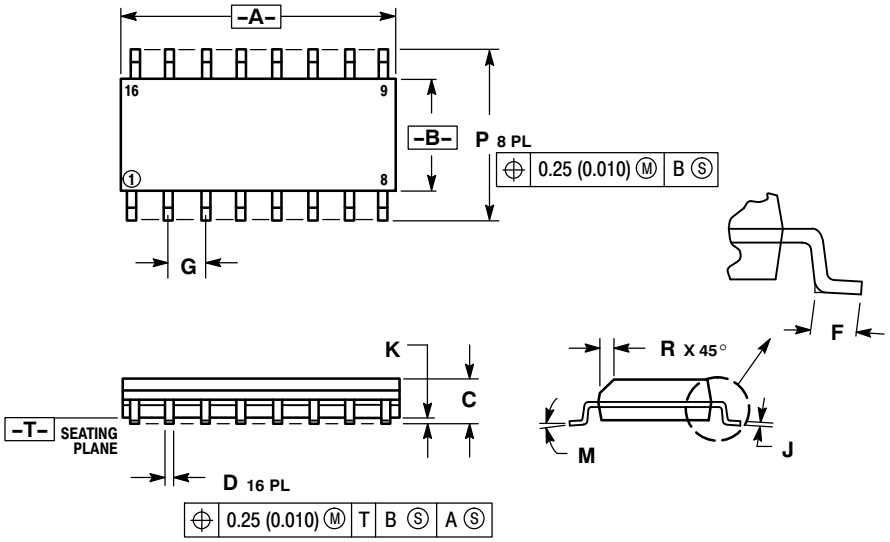


*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PACKAGE DIMENSIONS

SOIC−16
CASE 751B−05
ISSUE K

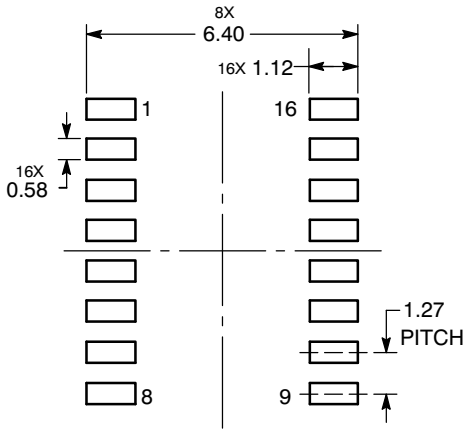
DATE 29 DEC 2006



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

SOLDERING FOOTPRINT



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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