NB4N507A

3.3V/5V, 50 MHz to 200 MHz PECL Clock Synthesizer

Description

The NB4N507A is a precision clock synthesizer which generates a very low jitter differential PECL output clock. It produces a clock output based on an integer multiple of an input reference frequency.

The NB4N507A accepts a standard fundamental mode crystal, using Phase−Locked−Loop (PLL) techniques, will produce output clocks up to 200 MHz. In addition, the PLL circuitry will produce a 50% duty cycle square−wave clock output.

The NB4N507A can be programmed to generate a selection of input reference frequency multiples. An exact 155.52 MHz output clock can be generated from a 19.44 MHz crystal and the x8 multiplier selection. The NB4N507A is intended for low output jitter clock generation.

Features

- Input Crystal Frequency of 10 − 27 MHz
- Enable Usage of Common Low−Cost Crystal
- Differential PECL Output Clock Frequencies up to 200 MHz
- Duty Cycle of 48%/52%
- Operating Range: V_{CC} = 3.0 V to 5.5 V
- Ideal for SONET Applications and Oscillator Manufacturers
- Available in Die Form
- Packaged in 16−Pin Narrow SOIC
- Pb−Free Packages are Available*

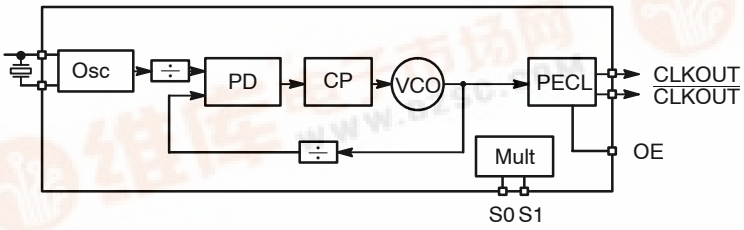

Figure 1. Simplified Logic Block

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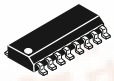
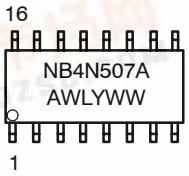
MARKING DIAGRAM



SOIC−16
D SUFFIX
CASE 751B



A = Assembly Location
WL, L = Wafer Lot
Y = Year
WW, W = Work Week

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 5 of this data sheet.

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

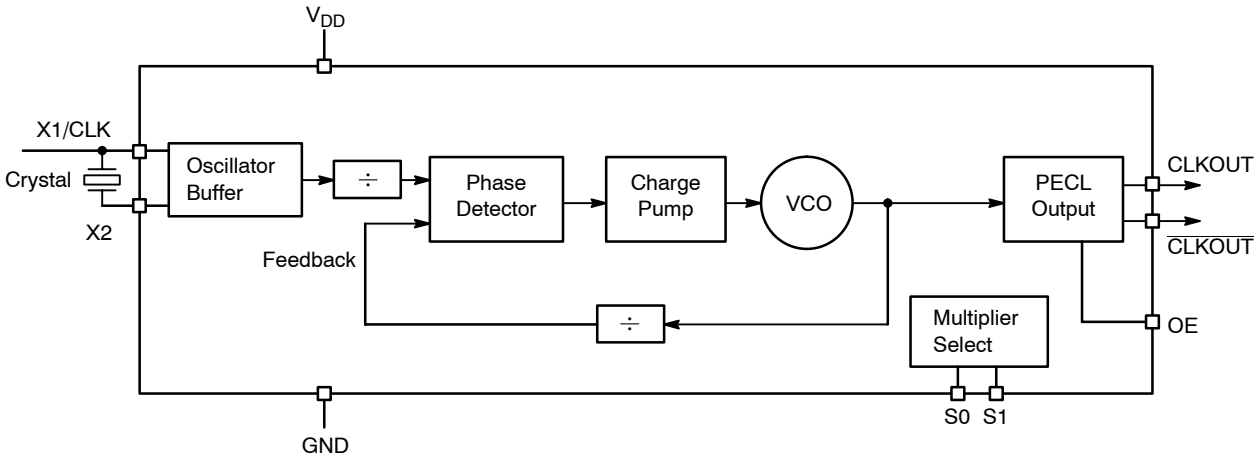


Figure 2. NB4N507A Logic Diagram

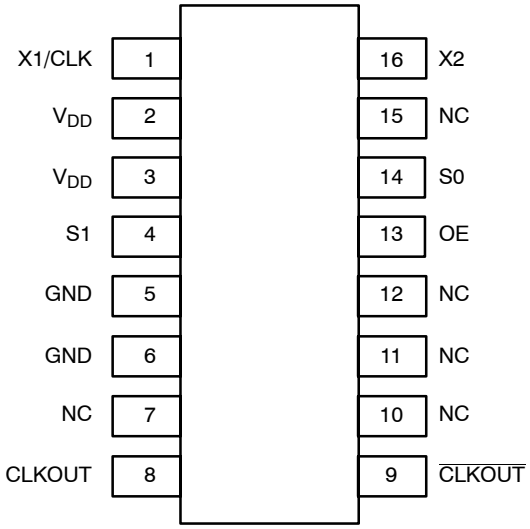


Figure 3. 16−Pin SOIC (Top View)

Table 1. CLOCK MULTIPLIER SELECT TABLE

S1	S0	Multiplier
L	L	9.72X*
L	M	10X
L	H	12X
M	L	6.25X
M	M	8X
M	H	5X
H	L	NA
H	M	3X
H	H	4X

Table 2. OE, OUTPUT ENABLE FUNCTION

OE	Function
0	Disable
1	Enable

*Crystal = 16 MHz, f_{CLKOUT} = 155.52 MHz
L = GND
H = V_{DD}
M = OPEN

Table 3. PIN DESCRIPTION

Pin # SOIC−16	Name	I/O	Description
1	X1/CLK	Crystal Input	Crystal or Clock Input
2,3	V_{DD}	Power Supply	Positive Supply Voltage (3.0 V to 5.5 V)
4	S1	Tri−Level Input	Multiplier Select Pin; When Left Open, Defaults to $V_{DD} \div 2$
5,6	GND	Power Supply	Negative Supply Voltage
7,10,11,12, 15	NC	No Connect	
8	CLKOUT	PECL Output	Non−inverted differential PECL clock output.
9	$\overline{\text{CLKOUT}}$	PECL Output	Inverted differential PECL clock output.
13	OE	(LV)CMOS/(LV)TTL Input	Output Enable for the CLKOUT/$\overline{\text{CLKOUT}}$ Outputs. Outputs are enabled when HIGH or when left open; OE pin has internal pullup resistor. Disables both outputs when LOW. CLKOUT goes LOW, $\overline{\text{CLKOUT}}$ goes HIGH.
14	S0	Tri−Level Input	Multiplier Select Pin; When Left Open, Defaults to $V_{DD} \div 2$
16	X2	Crystal Input	Crystal Input

Table 4. ATTRIBUTES

Characteristics		Value
ESD Protection	Human Body Model Machine Model Charged Device Model	> 1 kV > 150 V > 1 kV
Moisture Sensitivity, Indefinite Time Out of Drypack (Note 1)		Level 1
Flammability Rating	Oxygen Index: 28 to 34	UL 94 V−0 @ 0.125 in
Transistor Count		1145 Devices
Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test		

1. For additional information, see Application Note AND8003/D.

Table 5. MAXIMUM RATINGS

Symbol	Parameter	Condition 1	Condition 2	Rating	Unit
V_{CC}	Positive Power Supply	GND = 0 V		6	V
V_I	Input Voltage			$GND - 0.5 \le V_I \le V_{DD} + 0.5$	V
T_A	Operating Temperature Range			−40 to +85	°C
T_{stg}	Storage Temperature Range			−65 to +150	°C
θ_{JA}	Thermal Resistance (Junction−to−Ambient)	0 lfpm 500 lfpm	SOIC−16	100 60	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction−to−Case)	(Note 2)	SOIC−16	33 to 36	°C/W
T_{sol}	Wave Solder Pb Pb−Free	< 3 sec @ 248°C < 3 sec @ 260°C		265 265	°C

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

2. JEDEC standard multilayer board − 2S2P (2 signal, 2 power).

Table 6. DC CHARACTERISTICS (V_{DD} = 3.0 V to 5.5 V, GND = 0 V, T_A = −40°C to +85°C (Note 3))

Symbol	Characteristic		Min	Typ	Max	Unit
I_{DD}	Power Supply Current (does not include output load resistor current)	V_{DD} = 5 V V_{DD} = 3.3 V	15 10	27 23	35 30	mA mA
V_{OH}	Output HIGH Voltage (Notes 5 & 6)	V_{DD} = 5 V V_{DD} = 3.3 V	3.95 2.57	4.05 2.67	4.15 2.77	V
V_{OL}	Output LOW Voltage (Notes 5 & 6)	V_{DD} = 5 V V_{DD} = 3.3 V	3.12 1.90	3.20 2.00	3.30 2.10	V
V_{IH}	Input HIGH Voltage, S0, S1, OE, X1	(Note 4)	V_{DD} − 0.5		V_{DD}	V
V_{IL}	Input LOW Voltage, S0, S1, OE, X1	(Note 4)	0		0.5	V
C_x	Internal Crystal Capacitance, X1 & X2			0		pF
C_{in}	Input Capacitance, S0, S1, OE			5.0		pF

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

3. PECL output parameters vary 1:1 with V_{DD}.
4. S0 and S1 default to V_{DD} ÷ 2 when left open.

Table 7. AC CHARACTERISTICS (V_{DD} = 3.0 V to 5.5 V, GND = 0 V, T_A = −40°C to +85°C (Note 5))

Symbol	Characteristic	Min	Typ	Max	Unit
f_{Xtal}	Crystal Input Frequency	10		27	MHz
f_{CLK}	Input Clock Frequency (Note 8)	5		52	MHz
f_{OUT}	Output Frequency Range	50		200	MHz
$V_{out\ pk-pk}$	Output Amplitude	550	680		mV
DC	Clock Output Duty Cycle (Note 8)	48		52	%
PLL_{BW}	PLL Bandwidth (Note 8)	10			kHz
$t_{jitter\ (pd)}$	Period Jitter (RMS, 1σ)			10	ps
$t_{jitter\ (cyc-cyc)}$	Cycle−to−cycle Jitter			40	ps
tr/tf	Output Rise and Fall Times (Note 8)	50	270	500	ps

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

5. PECL outputs loaded with external resistors for proper operation (see Figure 4).
6. V_{OH} and V_{OL} can be set by the external resistors, which can be modified.
7. The crystal should be fundamental mode, parallel resonant. Do not use third overtone. For exact tuning when using a crystal, capacitors should be connected from pins X1 to ground and X2 to ground. The value of these capacitors is given by the following equation, where CL is the specified crystal load capacitance: Crystal caps (pF) = (CL−5) x 2. So, for a crystal with 16 pF load capacitance, use two 22 pF caps.
8. Guaranteed by design and characterization.

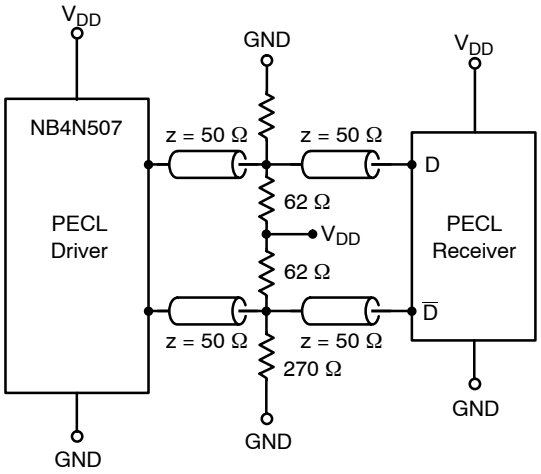


Figure 4. Recommended PECL Output Loading for the NB4N507A

APPLICATIONS INFORMATION

High Frequency Differential PECL Oscillators: The NB4N507A, along with a low frequency fundamental mode crystal, can build a high frequency differential PECL output oscillator. For example, a 10 MHz crystal connected to the NB4N507A with the 12X output selected (S1 = 0, S0 = 1) produces a 120 MHz PECL output clock.

High Frequency VCXO: The bandwidth of the PLL is guaranteed to be greater than 10 kHz. This means that the PLL will track any modulation on the input with a frequency of less than 10 kHz. By using this property, a low frequency VCXO can be built. The output can then be multiplied by the NB4N507A, thereby producing a high frequency VCXO.

High Frequency TCXO: Extending the previous application, an inexpensive, low frequency TCXO can be built and the output frequency can be multiplied using the NB4N507A. Since the output of the chip is phase−locked to the input, the NB4N507A has no temperature dependence, and the temperature coefficient of the combined system is the same as that of the low frequency TCXO.

Decoupling and External Components

The NB4N507A requires a 0.01 μF decoupling capacitor to be connected between V_{DD} and GND on pins 2 and 5. It must be connected close to the NB4N507A. Other V_{DD} and GND connections should be connected to those pins, or to the V_{DD} and GND planes on the board. Another four resistors are needed for the PECL outputs as shown on the block diagram in Figure 1. Suggested values of these resistors are shown in the Block Diagram, but they can be varied to change the differential pair output swing, and the DC level.

ORDERING INFORMATION

Device	Package	Shipping†
NB4N507AD	SOIC−16	48 Units / Rail
NB4N507ADG	SOIC−16 (Pb−Free)	48 Units / Rail
NB4N507ADR2	SOIC−16	2500 / Tape & Reel
NB4N507ADR2G	SOIC−16 (Pb−Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

Resource Reference of Application Notes

AN1405/D – ECL Clock Distribution Techniques

AN1406/D – Designing with PECL (ECL at +5.0 V)

AN1503/D – ECLinPS™ I/O SPiCE Modeling Kit

AN1504/D – Metastability and the ECLinPS Family

AN1568/D – Interfacing Between LVDS and ECL

AN1642/D – The ECL Translator Guide

AND8001/D – Odd Number Counters Design

AND8002/D – Marking and Date Codes

AND8020/D – Termination of ECL Logic Devices

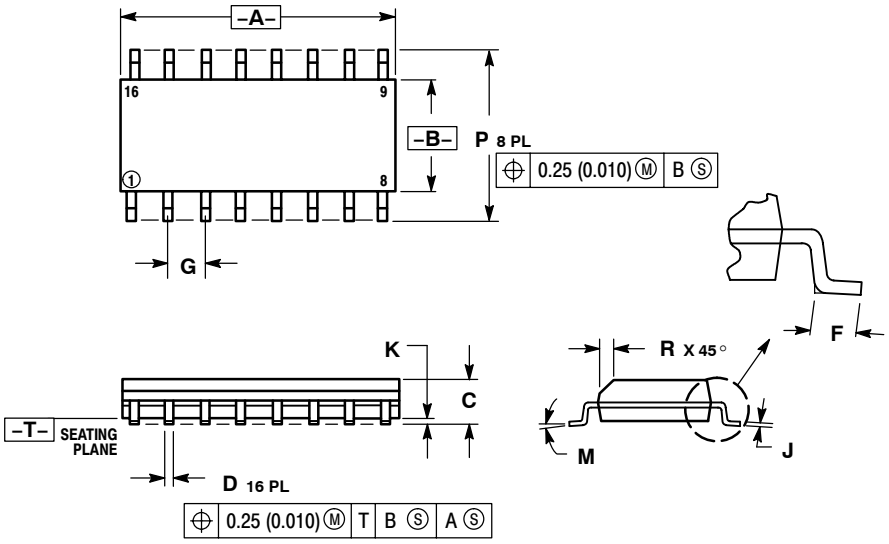
AND8066/D – Interfacing with ECLinPS

AND8090/D – AC Characteristics of ECL Devices

NB4N507A

PACKAGE DIMENSIONS

SOIC−16
D SUFFIX
CASE 751B−05
ISSUE J



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
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