

NC7WZ07 TinyLogic® UHS Dual Buffer (Open Drain Outputs)

General Description

The NC7WZ07 is a dual buffer with open drain outputs from Fairchild's Ultra High Speed Series of TinyLogic® in the space saving SC70 6-lead package. The device is fabricated with advanced CMOS technology to achieve ultra high speed with high output drive while maintaining low static power dissipation over a very broad V_{CC} operating range. The device is specified to operate over the 1.65V to 5.5V V_{CC} range. The inputs and outputs are high impedance when V_{CC} is 0V. Inputs tolerate voltages up to 7V independent of V_{CC} operating voltage.

Features

- Space saving SC70 6-lead package
- Ultra small MicroPak™ Pb-Free leadless package
- Ultra High Speed: t_{PZL} 2.3 ns Typ into 50 pF at 5V V_{CC}
- High I_{OL} Output Drive: +24 mA at 3V V_{CC}
- Broad V_{CC} Operating Range: 1.65V to 5.5V
- Matches the performance of LCX when operated at 3.3V V_{CC}
- Power down high impedance inputs/outputs
- Overvoltage tolerant inputs facilitate 5V to 3V translation
- Patented noise/EMI reduction circuitry implemented

Ordering Code:

Order Number	Package Number	Product Code Top Mark	Package Description	Supplied As
NC7WZ07P6X	MAA06A	Z07	6-Lead SC70, EIAJ SC88, 1.25mm Wide	3k Units on Tape and Reel
NC7WZ07P6X_NL (Note 1)	MAA06A	Z07	Pb-Free 6-Lead SC70, EIAJ SC88, 1.25mm Wide	3k Units on Tape and Reel
NC7WZ07L6X	MAC06A	D3	Pb-Free 6-Lead MicroPak, 1.0mm Wide	5k Units on Tape and Reel

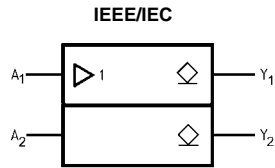
Pb-Free package per JEDEC J-STD-020B.

Note 1: "_NL" indicates Pb-Free product (per JEDEC J-STD-020B). Device is available in Tape and Reel only.

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NC7WZ07 TinyLogic® UHS Dual Buffer (Open Drain Outputs)

Logic Symbol



Pin Descriptions

Pin Names	Description
A ₁ , A ₂	Data Inputs
Y ₁ , Y ₂	Output

Function Table

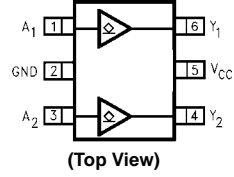
$Y = A$

Input	Output
A	Y
L	L
H	Z

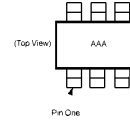
H = HIGH Logic Level
L = LOW Logic Level

Connection Diagrams

Pin Assignments for SC70

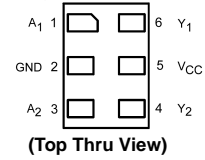


Pin One Orientation Diagram



AAA represents Product Code Top Mark - see ordering code
Note: Orientation of Top Mark determines Pin One location. Read the top product code mark left to right, Pin One is the lower left pin (see diagram).

Pad Assignments for MicroPak



Absolute Maximum Ratings (Note 2)

Supply Voltage (V_{CC})	-0.5V to +7V
DC Input Voltage (V_{IN})	-0.5V to +7V
DC Output Voltage (V_{OUT})	-0.5V to +7V
DC Input Diode Current (I_{IK}) @ $V_{IN} < -0.5V$	-50 mA
DC Output Diode Current (I_{OK}) @ $V_{OUT} < -0.5V$	-50 mA
DC Output Current (I_{OUT})	+50 mA
DC V_{CC}/GND Current (I_{CC}/I_{GND})	± 100 mA
Storage Temperature (T_{STG})	-65°C to +150°C
Junction Temperature under Bias (T_J)	150°C
Junction Lead Temperature (T_L) (Soldering, 10 seconds)	260°C
Power Dissipation (P_D) @ +85°C	180 mW

Recommended Operating Conditions (Note 3)

Supply Voltage Operating (V_{CC})	1.65V to 5.5V
Supply Voltage Data Retention (V_{CC})	1.5V to 5.5V
Input Voltage (V_{IN})	0V to 5.5V
Output Voltage (V_{OUT})	0V to 5.5V
Operating Temperature (T_A)	-40°C to +85°C
Input Rise and Fall Time (t_r, t_f) $V_{CC} = 1.8V, 2.5V \pm 0.2V$	0 ns/V to 20 ns/V
$V_{CC} = 3.3V \pm 0.3V$	0 ns/V to 10 ns/V
$V_{CC} = 5.0V \pm 0.5V$	0 ns/V to 5 ns/V
Thermal Resistance (θ_{JA})	350° C/W

Note 2: Absolute maximum ratings are DC values beyond which the device may be damaged or have its useful life impaired. The datasheet specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. Fairchild does not recommend operation outside datasheet specifications.

Note 3: Unused inputs must be held HIGH or LOW. They may not float.

DC Electrical Characteristics

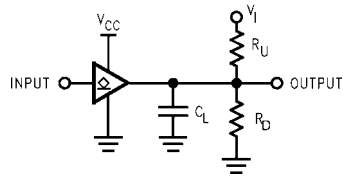
Symbol	Parameter	V_{CC} (V)	$T_A = +25^\circ C$			$T_A = -40^\circ C$ to $+85^\circ C$		Units	Conditions
			Min	Typ	Max	Min	Max		
V_{IH}	HIGH Level Input Voltage	1.65 to 1.95 2.3 to 5.5	0.75 V_{CC} 0.7 V_{CC}			0.75 V_{CC} 0.7 V_{CC}		V	
V_{IL}	LOW Level Input Voltage	1.65 to 1.95 2.3 to 5.5	0.25 V_{CC} 0.3 V_{CC}			0.25 V_{CC} 0.3 V_{CC}		V	
I_{LKG}	HIGH Level Output Leakage Current	1.65 to 5.5	± 5			± 10		μA	$V_{IN} = V_{IH}$ $V_{OUT} = V_{CC}$ or GND
V_{OL}	LOW Level Output Voltage	1.65	0.0	0.1	0.0		V	$V_{IN} = V_{IL}$ $I_{OL} = 100 \mu A$	
		1.8	0.0	0.1	0.1				
		2.3	0.0	0.1	0.1				
		3.0	0.0	0.1	0.1				
		4.5	0.0	0.1	0.1				
		1.65	0.08	0.24	0.24		V	$I_{OL} = 4 \text{ mA}$ $I_{OL} = 8 \text{ mA}$ $I_{OL} = 16 \text{ mA}$ $I_{OL} = 24 \text{ mA}$ $I_{OL} = 32 \text{ mA}$	
		2.3	0.10	0.3	0.3				
		3.0	0.16	0.4	0.4				
		3.0	0.24	0.55	0.55				
		4.5	0.25	0.55	0.55				
I_{IN}	Input Leakage Current	0 to 5.5	± 0.1			± 1.0		μA	$0 \leq V_{IN} \leq 5.5V$
I_{OFF}	Power Off Leakage Current	0.0	1			10		μA	V_{IN} or $V_{OUT} = 5.5V$
I_{CC}	Quiescent Supply Current	1.65 to 5.5	1.0			10		μA	$V_{IN} = 5.5V, GND$

AC Electrical Characteristics

Symbol	Parameter	V _{CC} (V)	T _A = +25°C			T _A = -40°C to +85°C		Units	Conditions	Figure Number
			Min	Typ	Max	Min	Max			
t _{PZL}	Propagation Delay	1.65	1.8	6.6	11.5	1.8	12.6	ns	C _L = 50 pF R _U = 500Ω R _D = 500Ω V _I = 2 x V _{CC}	Figures 1, 3
		1.8	1.8	5.5	9.5	1.8	10.5			
		2.5 ± 0.2	1.2	3.7	5.8	1.2	6.4			
		3.3 ± 0.3	0.8	2.9	4.4	0.8	4.8			
		5.0 ± 0.5	0.5	2.3	3.5	0.5	3.9			
t _{PLZ}	Propagation Delay	1.65	1.8	5.5	11.5	1.8	12.6	ns	C _L = 50 pF R _U = 500Ω R _D = 500Ω V _I = 2 x V _{CC}	Figures 1, 3
		1.8	1.8	4.3	9.5	1.8	10.5			
		2.5 ± 0.2	1.2	2.8	5.8	1.2	6.4			
		3.3 ± 0.3	0.8	2.1	4.4	0.8	4.8			
		5.0 ± 0.5	0.5	1.4	3.5	0.5	3.9			
C _{IN}	Input Capacitance	0	2.5					pF		
C _{OUT}	Output Capacitance	0	4.0					pF		
C _{PD}	Power Dissipation	3.3	3					pF	(Note 4)	Figure 2
	Capacitance	5.0	4							

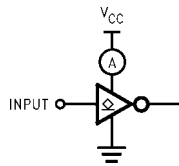
Note 4: C_{PD} is defined as the value of the internal equivalent capacitance which is derived from dynamic operating current consumption (I_{CCD}) at no output loading and operating at 50% duty cycle. (See Figure 2.) C_{PD} is related to I_{CCD} dynamic operating current by the expression:
 $I_{CCD} = (C_{PD})(V_{CC})(f_{IN}) + (I_{CCstatic})$.

AC Loading and Waveforms



C_L includes load and stray capacitance
 Input PRR = 1.0 MHz; t_w = 500 ns

FIGURE 1. AC Test Circuit



Input = AC Waveform; t_r = t_f = 1.8 ns;
 PRR = 10 MHz; Duty Cycle = 50%

FIGURE 2. I_{CCD} Test Circuit

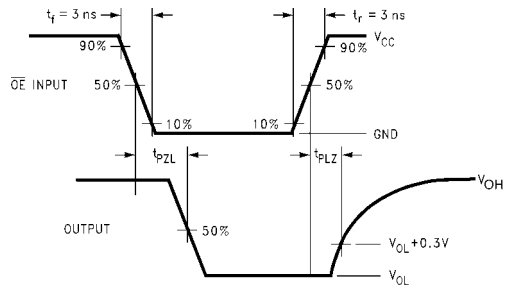


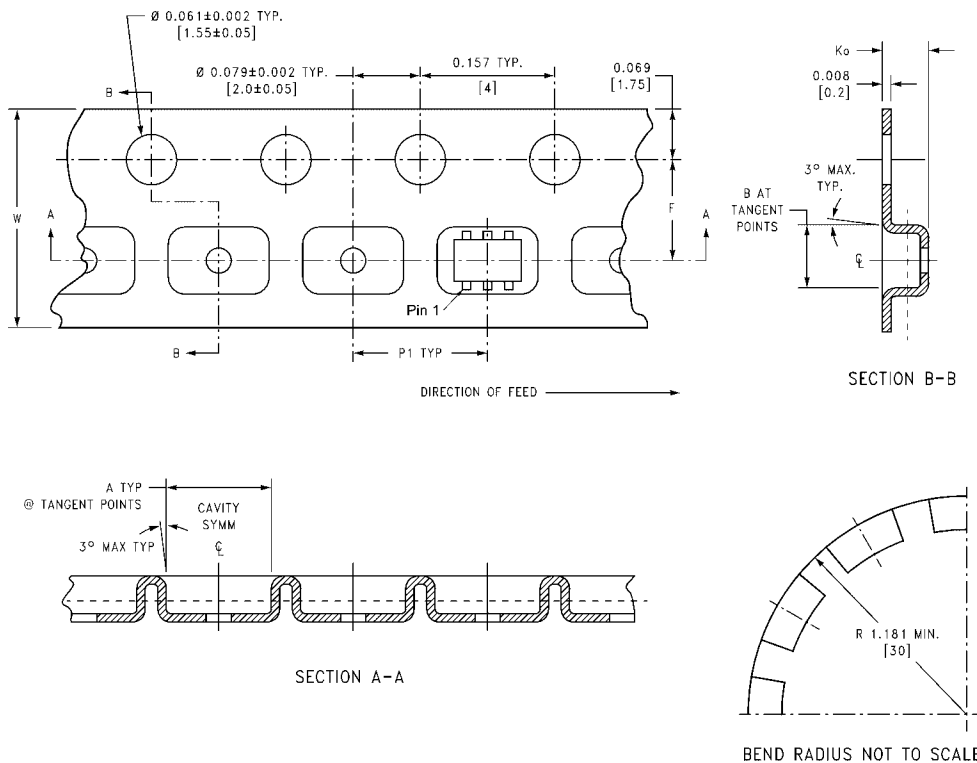
FIGURE 3. AC Waveforms

Tape and Reel Specification

TAPE FORMAT for SC70

Package Designator	Tape Section	Number Cavities	Cavity Status	Cover Tape Status
P6X	Leader (Start End)	125 (typ)	Empty	Sealed
	Carrier	3000	Filled	Sealed
	Trailer (Hub End)	75 (typ)	Empty	Sealed

TAPE DIMENSIONS inches (millimeters)



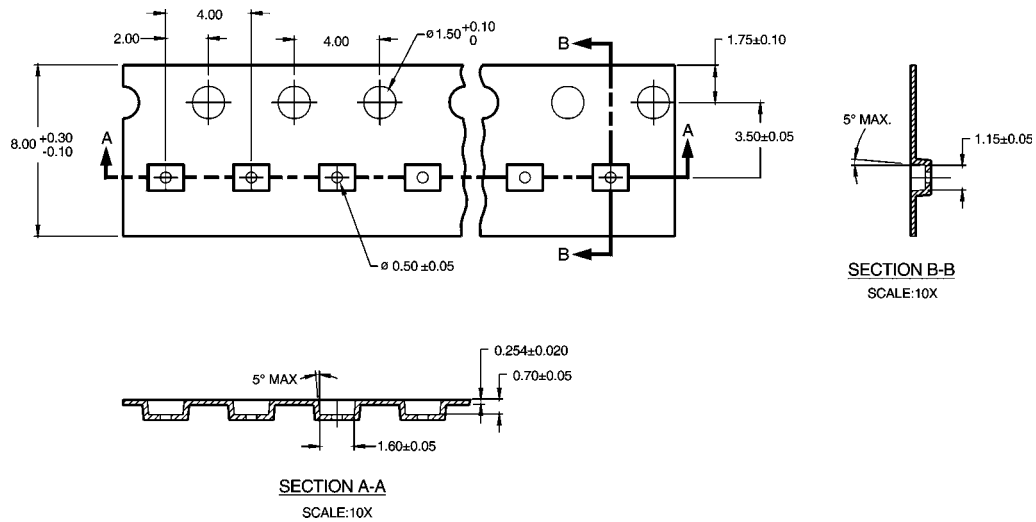
Package	Tape Size	DIM A	DIM B	DIM F	DIM K_0	DIM P1	DIM W
SC70-6	8 mm	0.093 (2.35)	0.096 (2.45)	0.138 ± 0.004 (3.5 ± 0.10)	0.053 ± 0.004 (1.35 ± 0.10)	0.157 (4)	0.315 ± 0.004 (8 ± 0.1)

NC7WZ07

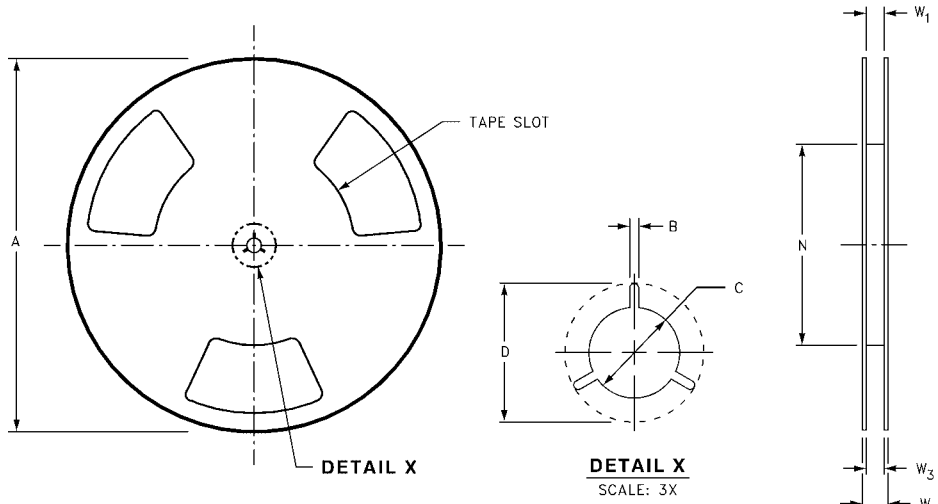
Tape and Reel Specification (Continued)

TAPE FORMAT for MicroPak

Package Designator	Tape Section	Number Cavities	Cavity Status	Cover Tape Status
L6X	Leader (Start End)	125 (typ)	Empty	Sealed
	Carrier	5000	Filled	Sealed
	Trailer (Hub End)	75 (typ)	Empty	Sealed

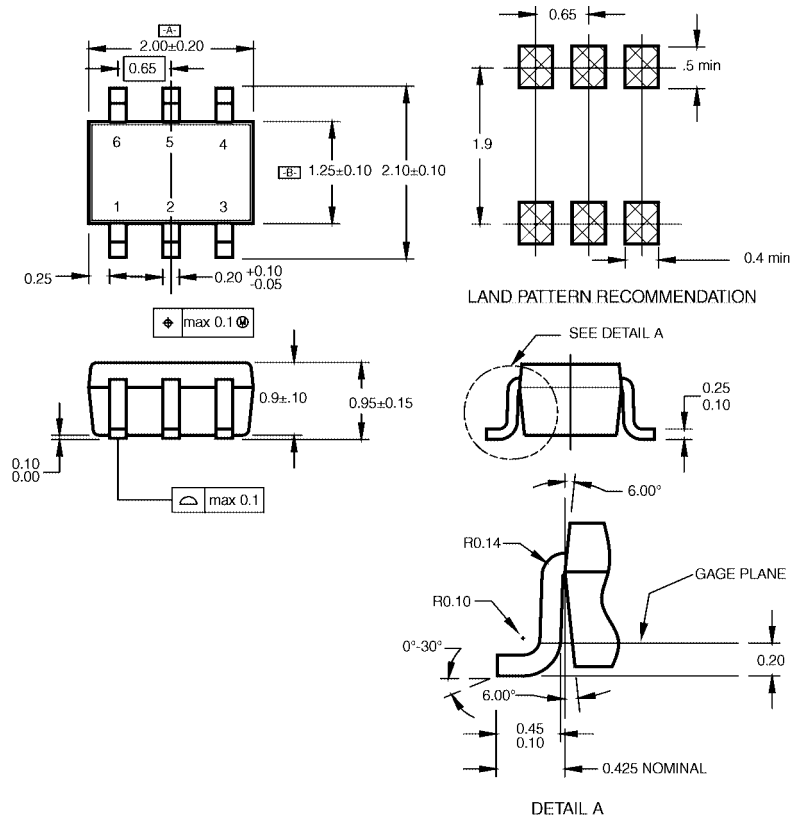


REEL DIMENSIONS inches (millimeters)



Tape Size	A	B	C	D	N	W1	W2	W3
8 mm	7.0 (177.8)	0.059 (1.50)	0.512 (13.00)	0.795 (20.20)	2.165 (55.00)	0.331 + 0.059/-0.000 (8.40 + 1.50/-0.00)	0.567 (14.40)	W1 + 0.078/-0.039 (W1 + 2.00/-1.00)

Physical Dimensions inches (millimeters) unless otherwise noted

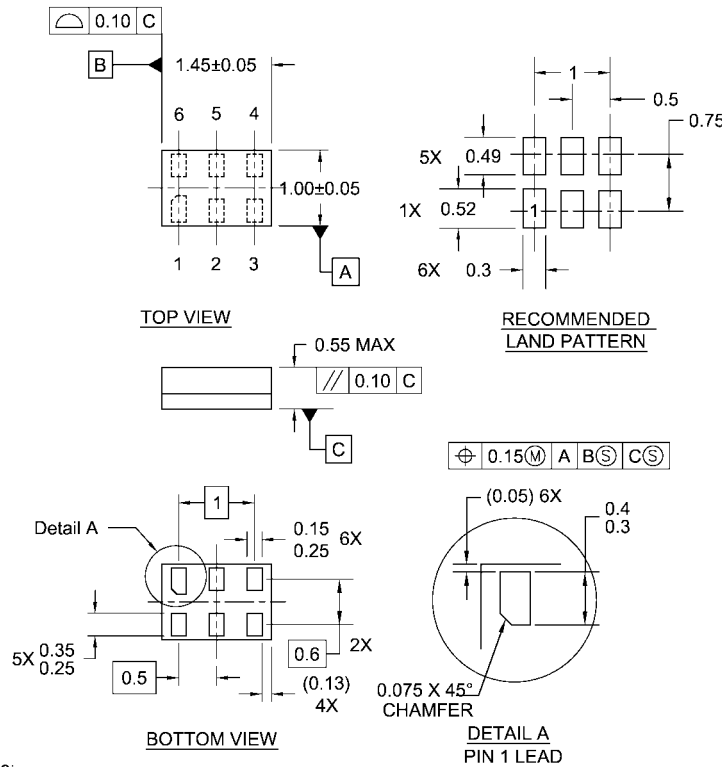


- NOTES:
- A. CONFORMS TO EIAJ REGISTERED OUTLINE DRAWING SC88.
 - B. DIMENSIONS DO NOT INCLUDE BURRS OR MOLD FLASH.
 - C. DIMENSIONS ARE IN MILLIMETERS.

MAA06ARevC

**6-Lead SC70, EIAJ SC88, 1.25mm Wide
Package Number MAA06A**

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



Notes:

1. JEDEC PACKAGE REGISTRATION IS ANTICIPATED
2. DIMENSIONS ARE IN MILLIMETERS
3. DRAWING CONFORMS TO ASME Y14.5M-1994

MAC06ARevB

**Pb-Free 6-Lead MicroPak, 1.0mm Wide
Package Number MAC06A**

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