

July 2001 Revised April 2003

NC7NZ34 TinyLogic® UHS Triple Buffer

General Description

The NC7NZ34 is a triple buffer from Fairchild's Ultra High Speed Series of TinyLogic® in the space saving US8 package. The device is fabricated with advanced CMOS technology to achieve ultra high speed with high output drive while maintaining low static power dissipation over a very broad $\rm V_{CC}$ operating range. The device is specified to operate over the 1.65V to 5.5V $\rm V_{CC}$ range. The inputs and outputs are high impedance when $\rm V_{CC}$ is 0V. Inputs tolerate voltages up to 7V independent of $\rm V_{CC}$ operating voltage.

Features

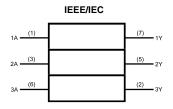
- Space saving US8 surface mount package
- MicroPak™ leadless package
- Ultra High Speed: t_{PD} 2.4 ns Typ into 50 pF at 5V V_{CC}
- High Output Drive: ±24 mA at 3V V_{CC}
- Broad V_{CC} Operating Range: 1.65V to 5.5V
- Power down high impedance inputs/outputs
- Overvoltage tolerant inputs facilitate 5V to 3V translation
- Patented noise/EMI reduction circuitry implemented

Ordering Code:

Order Number	Package Number	Product Code Top Mark	Package Description	Supplied As
NC7NZ34K8X	MAB08A	7NZ34	8-Lead US8, JEDEC MO-187, Variation CA 3.1mm Wide	3k Units on Tape and Reel
NC7NZ34L8X (Preliminary)	MAC08A	P9	8-Lead MicroPak, 1.6 mm Wide	5k Units on Tape and Reel

 $\label{eq:total_cond} \mbox{TinyLogio} \mbox{\mathbb{B} is a registered trademark of Fairchild Semiconductor Corporation.} \\ \mbox{MicroPak}^{\mbox{\mathbb{M}}} \mbox{\mathbb{M} is a trademark of Fairchild Semiconductor Corporation.} \\$

Logic Symbol



Pin Descriptions

Pin Names	Description
A ₁ , A ₂ , A ₃	Data Inputs
Y_1, Y_2, Y_3	Output

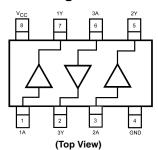
Function Table

$\boldsymbol{Y}=\boldsymbol{A}$

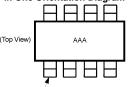
Input	Output
Α	Y
L	L
Н	Н

H = HIGH Logic Level L = LOW Logic Level

Connection Diagrams



Pin One Orientation Diagram

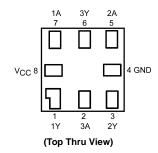


Pin One

AAA represents Product Code Top Mark - see ordering code

Note: Orientation of Top Mark determines Pin One location. Read the top product code mark left to right, Pin One is the lower left pin (see diagram).

Pad Assignments for MicroPak



Absolute Maximum Ratings(Note 1)

 $\begin{array}{lll} \text{Supply Voltage (V}_{\text{CC}}) & -0.5 \text{V to } +7.0 \text{V} \\ \text{DC Input Voltage (V}_{\text{IN}}) & -0.5 \text{V to } +7.0 \text{V} \\ \text{DC Output Voltage (V}_{\text{OUT}}) & -0.5 \text{V to } +7.0 \text{V} \\ \end{array}$

DC Input Diode Current (I_{IK})

 $V_{IN} < 0V$ –50 mA

DC Output Diode Current (I_{OK})

 $\begin{array}{ccc} V_{OUT} < 0V & -50 \text{ mA} \\ DC \text{ Output Source/Sink Current (I}_{OUT}) & \pm 50 \text{ mA} \\ DC \text{ V}_{CC} / \text{GND Current (I}_{CC} / \text{I}_{GND}) & \pm 100 \text{ mA} \\ Storage \text{ Temperature (T}_{STG}) & -65^{\circ}\text{C to +150}^{\circ}\text{C} \\ Junction \text{ Temperature under Bias (T,j)} & 150^{\circ}\text{C} \\ \end{array}$

Junction Lead Temperature (T_L)

(Soldering, 10 seconds) 260 $^{\circ}$ C Power Dissipation (P_D) @ +85 $^{\circ}$ C 250 mW

Recommended Operating Conditions (Note 2)

Supply Voltage

cations.

Operating (V_{CC}) 1.65V to 5.5V Data Retention 1.5V to 5.5V Input Voltage (V_{IN}) 0V to 5.5V Output Voltage (V_{OUT}) 0V to V_{CC} Input Rise and Fall Time $(t_r,\,t_f)$ $V_{CC} = 1.8V, \, 2.5V \pm 0.2V$ 0 to 20 ns/V $V_{CC}=3.3V\pm0.3V$ 0 to 10 ns/V $V_{CC} = 5.5V \pm 0.5V$ 0 to 5 ns/V Operating Temperature (T_A) -40°C to +85°C

Thermal Resistance (θ_{JA}) 250°C/W Note 1: Absolute maximum ratings are DC values beyond which the device may be damaged or have its useful life impaired. The datasheet specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. Fairchild does not recommend operation outside datasheet specifi-

Note 2: Unused inputs must be held HIGH or LOW. They may not float.

DC Electrical Characteristics

Symbol	Parameter	V_{CC} $T_A = +25^{\circ}C$		$T_A = -40^{\circ}C$ to $+85^{\circ}C$		Units	Conditions			
Зупівої	raiametei	(V)	Min	Тур	Max	Min	Max	Units	00	nations
V _{IH}	HIGH Level Control	1.8 ± 0.15	0.75 V _{CC}			0.75 V _{CC}		V		
	Input Voltage	2.3 to 5.5	0.7 V _{CC}			0.7 V _{CC}		V		
V _{IL}	LOW Level Control	1.8 ± 0.15			0.25 V _{CC}		0.25 V _{CC}	V		
	Input Voltage	2.3 to 5.5			$0.3\ V_{\rm CC}$		$0.3\mathrm{V}_{\mathrm{CC}}$	l v		
V _{OH}	HIGH Level Control	1.65	1.55	1.65		1.55				
	Output Voltage	2.3	2.2	2.3		2.2				$I_{OH} = -100 \mu A$
		3.0	2.9	3.0		2.9				10H = -100 μΑ
		4.5	4.4	4.5		4.4				
		1.65	1.29	1.52		1.29		V	$V_{IN} = V_{IH} \\$	$I_{OH} = -4 \text{ mA}$
		2.3	1.9	2.14		1.9				$I_{OH} = -8 \text{ mA}$
		3.0	2.4	2.75		2.4				$I_{OH} = -16 \text{ mA}$
		3.0	2.3	2.62		2.3				$I_{OH} = -24 \text{ mA}$
		4.5	3.8	4.13		3.8				$I_{OH} = -32 \text{ mA}$
V _{OL}	LOW Level Control	1.65		0.0	0.1		0.1			
	Output Voltage	2.3		0.0	0.1		0.1			I _{OL} = 100 μA
		3.0		0.0	0.1		0.1			100 μΑ
		4.5		0.0	0.1		0.1			
		1.65		0.08	0.24		0.24	V	$V_{\text{IN}} = V_{\text{IL}}$	$I_{OL} = 4 \text{ mA}$
		2.3		0.10	0.3		0.3			$I_{OL} = 8 \text{ mA}$
		3.0		0.16	0.4		0.4			$I_{OL} = 16 \text{ mA}$
		3.0		0.24	0.55		0.55			$I_{OL} = 24 \text{ mA}$
		4.5		0.25	0.55		0.55			$I_{OL} = 32 \text{ mA}$
I _{IN}	Input Leakage Current	0 to 5.5			±0.1		±1.0	μΑ	$0 \le V_{IN} \le 5$.5V
I _{OFF}	Power Off Leakage Current	0.0			1.0		10	μΑ	V _{IN} or V _{OU}	_T = 5.5V
I _{CC}	Quiescent Supply Current	1.65 to 5.5			1.0		10	μΑ	$V_{IN} = 5.5V$	GND

AC Electrical Characteristics

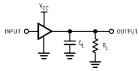
Symbol	Parameter	V _{CC}	V_{CC} $T_A = +25^{\circ}C$		$T_A = -40^{\circ}C$ to $+85^{\circ}C$		Units	Conditions	Figure	
		(V)	Min	Тур	Max	Min	Max	Oillio		Number
t _{PLH}	Propagation Delay	1.8 ± 0.15	1.8	4.6	8.0	1.8	8.8			
t _{PHL}		2.5 ± 0.2	1.0	3.0	5.2	1.0	5.8	ns	$C_L = 15 pF$,	Figures
		3.3 ± 0.3	0.8	2.3	3.6	0.8	4.0	115	$R_L = 1 \ M\Omega$	1, 3
		5.0 ± 0.5	0.5	1.8	2.9	0.5	3.2			
t _{PLH}	Propagation Delay	3.3 ± 0.3	1.2	3.0	4.6	1.2	5.1	ns	$C_L = 50 \text{ pF},$	Figures
t _{PHL}		5.0 ± 0.5	0.8	2.4	3.8	0.8	4.2	115	$R_L=500\Omega$	1, 3
C _{IN}	Input Capacitance	0		2.5				pF		
C _{PD}	Power Dissipation	3.3		9				pF	(Note 3)	Figure 2
	Capacitance	5.0		11				ρı	(NOTE 3)	rigule 2

Note 3: C_{PD} is defined as the value of the internal equivalent capacitance which is derived from dynamic operating current consumption (I_{CCD}) at no output loading and operating at 50% duty cycle. (See Figure 2.) C_{PD} is related to I_{CCD} dynamic operating current by the expression: $I_{CCD} = (C_{PD})(V_{CC})(f_{|N}) + (I_{CC} static)$.

Dynamic Switching Characteristics

Symbol	Parameter	Conditions	V _{CC}	T _A = 25°C	Unit
•,			(V) Typical		
V _{OLP}	Quiet Output Dynamic Peak V _{OL}	$C_L = 50pF, V_{IH} = 5.0V, V_{IL} = 0V$	5.0	0.8	V
V _{OLV}	Quiet Output Dynamic Valley V _{OL}	$C_L = 50pF, V_{IH} = 5.0V, V_{IL} = 0V$	5.0	-0.8	V

AC Loading and Waveforms



 C_L includes load and stray capacitance Input PRR = 1.0 MHz; t_W = 500 ns

FIGURE 1. AC Test Circuit



 $\begin{aligned} & \text{Input} = \text{AC Waveform; } t_{\text{f}} = t_{\text{f}} = 1.8 \text{ ns;} \\ & \text{PRR} = 10 \text{ MHz; Duty Cycle} = 50\% \end{aligned}$

FIGURE 2. I_{CCD} Test Circuit

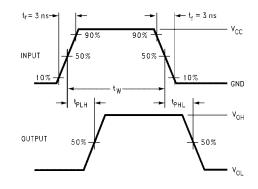


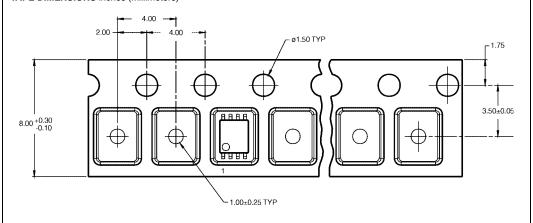
FIGURE 3. AC Waveforms

Tape and Reel Specification

TAPE FORMAT for US8

Package	Tape	Number	Cavity	Cover Tape	
Designator	Section	Cavities	Status	Status	
	Leader (Start End)	125 (typ)	Empty	Sealed	
K8X	Carrier	3000	Filled	Sealed	
	Trailer (Hub End)	75 (typ)	Empty	Sealed	

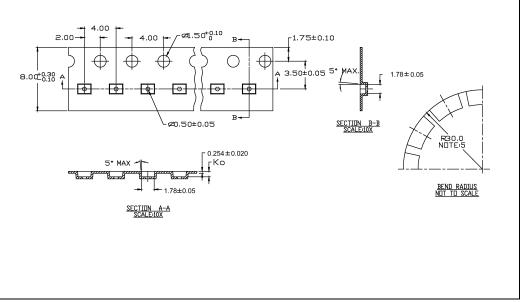
TAPE DIMENSIONS inches (millimeters)



TAPE FORMAT for MicroPak

Package	Tape	Number	Cavity	Cover Tape	
Designator	Section	Cavities	Status	Status	
	Leader (Start End)	125 (typ)	Empty	Sealed	
K8X	Carrier	3000	Filled	Sealed	
	Trailer (Hub End)	75 (typ)	Empty	Sealed	

TAPE DIMENSIONS inches (millimeters)



Tape and Reel Specification (Continued) REEL DIMENSIONS inches (millimeters) TAPE SLOT TAPE SLOT DETAIL X SCALE: 3X Tape A B C D N W1 W2 W3

0.567

(14.40)

W1 + 0.078/-0.039

(W1 + 2.00/-1.00)

7.0

(177.8)

8 mm

0.059

(1.50)

0.512

(13.00)

0.795

(20.20)

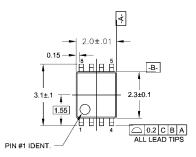
2.165

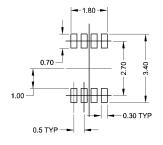
(55.00)

0.331 + 0.059/-0.000

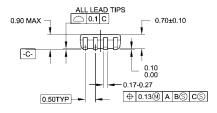
(8.40 + 1.50 / -0.00)

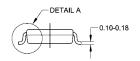
Physical Dimensions inches (millimeters) unless otherwise noted

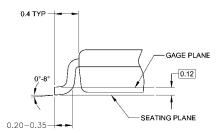




LAND PATTERN RECOMMENDATION







NOTES:

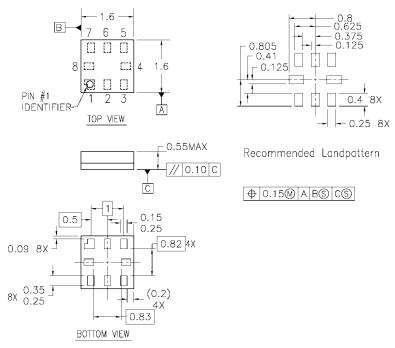
- A. CONFORMS TO JEDEC REGISTRATION MO-187
 B. DIMENSIONS ARE IN MILLIMETERS.
 C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.
- D. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1982.

DETAIL A

MAB08AREVC

8-Lead US8, JEDEC MO-187, Variation CA 3.1mm Wide Package Number MAB08A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



Notes:

- 1. PACKAGE REGISTRATION WITH JEDEC IS ANTICIPATED
- 2. DIMENSIONS ARE IN MILLIMETERS
- 3. DRAWING CONFORMS TO ASME Y.14M-1994

MAC08AREVB

8-Lead MicroPak, 1.6 mm Wide Package Number MAC08A (Preliminary)

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