NCS2510

Product Preview

1.0 GHz Current Feedback Op Amp with Enable Feature

NCS2510 is a 1.0 GHz current feedback monolithic operational amplifier featuring high slew rate and low differential gain and phase error. The current feedback architecture allows for a superior bandwidth and low power consumption. This device features an enable pin.

Features

- −3.0 dB Small Signal BW (A_V = +2.0, V_O = 0.5 V_{p-p}) 1.0 GHz Typ
- Slew Rate 1500 V/μs
- Supply Current 8.5 mA
- Input Referred Voltage Noise 6.0 nV/$\sqrt{Hz}$
- THD −60 dBc (f = 5.0 MHz, V_O = 2.0 V_{p-p})
- Output Current 150 mA
- Enable Pin Available
- Pin Compatible with AD8001
- Pb−Free Packages are Available

Applications

- High Resolution Video
- Line Driver
- High−Speed Instrumentation
- Wide Dynamic Range IF Amp
- Set Top Box
- NTSC/PAL/HDTV

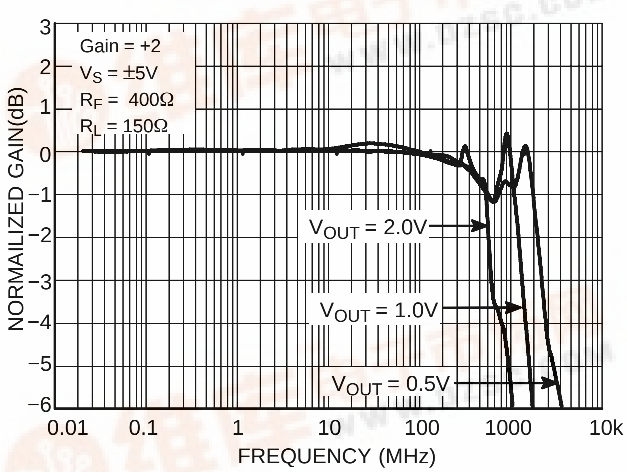

Figure 1. Frequency Response: Gain (dB) vs. Frequency Av = +2.0

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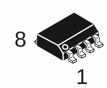
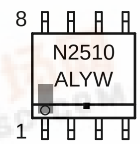
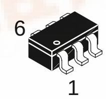
MARKING DIAGRAMS

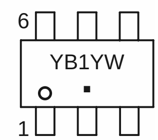


SO−8 D SUFFIX CASE 751



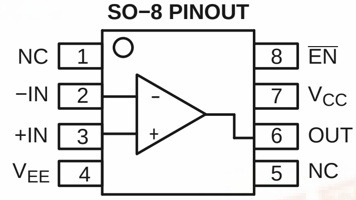


SOT23−6 (TSOP−6) SN SUFFIX CASE 318G



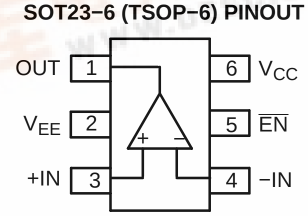
YB1, N2510	= NCS2510
A	= Assembly Location
L	= Wafer Lot
Y	= Year
W	= Work Week
▪	= Pb−Free Package

SO−8 PINOUT



(Top View)

SOT23−6 (TSOP−6) PINOUT

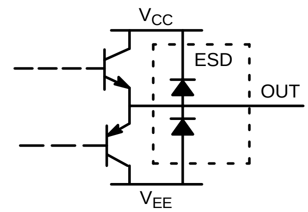
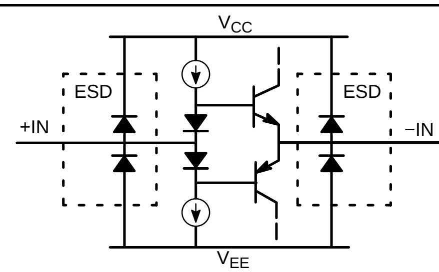
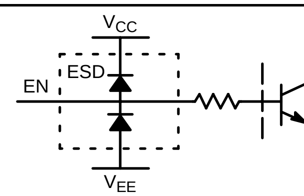


(Top View)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 12 of this data sheet.

PIN FUNCTION DESCRIPTION

Pin (SO−8)	Pin (SOT23/SC70)	Symbol	Function	Equivalent Circuit
6	1	OUT	Output	
4	2	V_{EE}	Negative Power Supply	
3	3	+IN	Non−inverted Input	
2	4	−IN	Inverted Input	See Above
7	6	V_{CC}	Positive Power Supply	
8	5	$\overline{EN}$	Enable	
1, 8	N/A	NC	No Connect	

ENABLE PIN TRUTH TABLE

	High	Low*
Enable	Disabled	Enabled

*Default open state

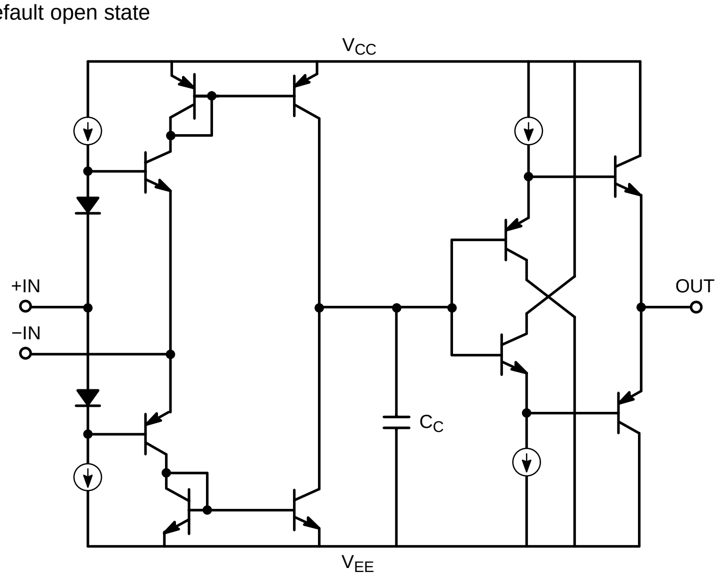


Figure 2. Simplified Device Schematic

ATTRIBUTES

Characteristics		Value
ESD Human Body Model Machine Model Charged Device Model		 2.0 kV (Note 1) 200 V 1.0 kV
Moisture Sensitivity (Note 2)		Level 1
Flammability Rating	Oxygen Index: 28 to 34	UL 94 V−0 @ 0.125 in

1. 0.8 kV between the input pairs +IN and −IN pins only. All other pins are 2.0 kV.
2. For additional information, see Application Note AND8003/D.

MAXIMUM RATINGS

Parameter	Symbol	Rating	Unit
Power Supply Voltage	V_S	11	Vdc
Input Voltage Range	V_I	$\leq V_S$	Vdc
Input Differential Voltage Range	V_{ID}	$\leq V_S$	Vdc
Output Current	I_O	100	mA
Maximum Junction Temperature (Note 3)	T_J	150	°C
Operating Ambient Temperature	T_A	−40 to +85	°C
Storage Temperature Range	T_{stg}	−60 to +150	°C
Power Dissipation	P_D	(See Graph)	mW
Thermal Resistance, Junction−to−Air SO−8 SOT23−6	$R_{\theta JA}$	 139 121	°C/W

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

3. Power dissipation must be considered to ensure maximum junction temperature (T_J) is not exceeded.

MAXIMUM POWER DISSIPATION

The maximum power that can be safely dissipated is limited by the associated rise in junction temperature. For the plastic packages, the maximum safe junction temperature is 150°C. If the maximum is exceeded momentarily, proper circuit operation will be restored as soon as the die temperature is reduced. Leaving the device in the "overheated" condition for an extended period can result in device damage. To ensure proper operation, it is important to observe the derating curves.

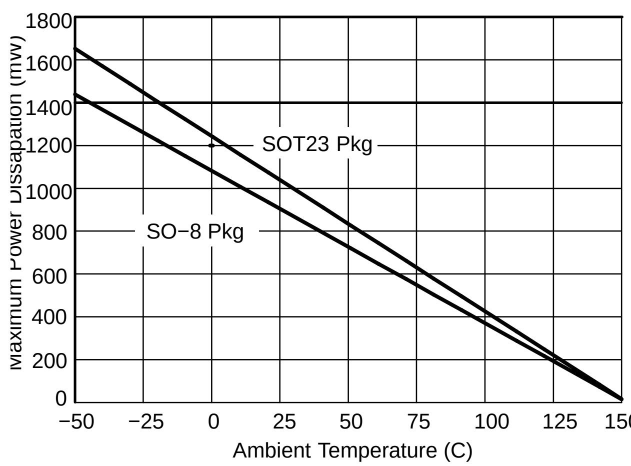


Figure 3. Power Dissipation vs. Temperature

AC ELECTRICAL CHARACTERISTICS (V_{CC} = +5.0 V, V_{EE} = −5.0 V, T_A = −40°C to +85°C, R_L = 150 Ω to GND, R_F = 400 Ω, A_V = +2.0, Enable is left open, unless otherwise specified).

Symbol	Characteristic	Conditions	Min	Typ	Max	Unit
FREQUENCY DOMAIN PERFORMANCE						
BW	Bandwidth 3.0 dB Small Signal 3.0 dB Large Signal	 A_V = +2.0, V_O = 0.5 V_{p-p} A_V = +2.0, V_O = 2.0 V_{p-p}		 1000 450		MHz
$GF_{0.1dB}$	0.1 dB Gain Flatness Bandwidth	A_V = +2.0		120		MHz
dG	Differential Gain	A_V = +2.0, R_L = 150 Ω, f = 3.58 MHz		0.01		%
dP	Differential Phase	A_V = +2.0, R_L = 150 Ω, f = 3.58 MHz		0.01		°
TIME DOMAIN RESPONSE						
SR	Slew Rate	A_V = +2.0, V_{step} = 2.0 V		1500		V/μs
t_s	Settling Time 0.01% 0.1%	 A_V = +2.0, V_{step} = 2.0 V A_V = +2.0, V_{step} = 2.0 V		 9.0 7.0		ns
t_r t_f	Rise and Fall Time	(10%−90%) A_V = +2.0, V_{step} = 2.0 V		1.5		ns
t_{ON}	Turn−on Time			55		ns
t_{OFF}	Turn−off Time			55		ns
HARMONIC/NOISE PERFORMANCE						
THD	Total Harmonic Distortion	f = 5.0 MHz, V_O = 2.0 V_{p-p}		−60		dBc
HD2	2nd Harmonic Distortion	f = 5.0 MHz, V_O = 2.0 V_{p-p}		−62		dBc
HD3	3rd Harmonic Distortion	f = 5.0 MHz, V_O = 2.0 V_{p-p}		−66		dBc
IP3	Third−Order Intercept	f = 10 MHz, V_O = 1.0 V_{p-p}		34		dBm
SFDR	Spurious−Free Dynamic Range	f = 5.0 MHz, V_O = 2.0 V_{p-p}		55		dBc
e_N	Input Referred Voltage Noise	f = 1.0 MHz		6.0		$nV/\sqrt{Hz}$
i_N	Input Referred Current Noise	f = 1.0 MHz, Inverting f = 1.0 MHz, Non−Inverting		10 3.0		$pA/\sqrt{Hz}$

DC ELECTRICAL CHARACTERISTICS (V_{CC} = +5.0 V, V_{EE} = −5.0 V, T_A = −40°C to +85°C, R_L = 150 Ω to GND, R_F = 400 Ω, A_V = +2.0, Enable is left open, unless otherwise specified).

Symbol	Characteristic	Conditions	Min	Typ	Max	Unit
DC PERFORMANCE						
V_{IO}	Input Offset Voltage		−5.0	0	+5.0	mV
$\Delta V_{IO}/\Delta T$	Input Offset Voltage Temperature Coefficient			6.0		μV/°C
I_{IB}	Input Bias Current	+Input (Non−Inverting), V_O = 0 V −Input (Inverting), V_O = 0 V (Note 4)		±3.0 ±6.0		μA
$\Delta I_{IB}/\Delta T$	Input Bias Current Temperature Coefficient	+Input (Non−Inverting), V_O = 0 V −Input (Inverting), V_O = 0 V		+40 −10		nA/°C
V_{IH}	Input High Voltage (Enable) (Note 4)		2.5			V
V_{IL}	Input Low Voltage (Enable) (Note 4)				−2.5	V
INPUT CHARACTERISTICS						
V_{CM}	Input Common Mode Voltage Range			±3.0		V
CMRR	Common Mode Rejection Ratio	(See Graph)		55		dB
R_{IN}	Input Resistance	+Input (Non−Inverting) −Input (Inverting)		100 50		kΩ Ω
C_{IN}	Differential Input Capacitance			1.0		pF
OUTPUT CHARACTERISTICS						
R_{OUT}	Output Resistance			0.1		Ω
V_O	Output Voltage Range			±3.0		V
I_O	Output Current		±90	±120		mA
POWER SUPPLY						
V_S	Operating Voltage Supply Range			10		V
$I_{S,ON}$	Power Supply Current − Enabled	V_O = 0 V		8.5		mA
$I_{S,OFF}$	Power Supply Current − Disabled	V_O = 0 V		0.11		mA
PSRR	Power Supply Rejection Ratio	(See Graph)		60		dB

4. Guaranteed by design and/or characterization.

AC ELECTRICAL CHARACTERISTICS (V_{CC} = +2.5 V, V_{EE} = −2.5 V, T_A = −40°C to +85°C, R_L = 150 Ω to GND, R_F = 400 Ω, A_V = +2.0, Enable is left open, unless otherwise specified).

Symbol	Characteristic	Conditions	Min	Typ	Max	Unit
FREQUENCY DOMAIN PERFORMANCE						
BW	Bandwidth 3.0 dB Small Signal 3.0 dB Large Signal	 A_V = +2.0, V_O = 0.5 V_{p-p} A_V = +2.0, V_O = 1.0 V_{p-p}		 600 300		MHz
$GF_{0.1dB}$	0.1 dB Gain Flatness Bandwidth	A_V = +2.0		100		MHz
dG	Differential Gain	A_V = +2.0, R_L = 150 Ω, f = 3.58 MHz		0.01		%
dP	Differential Phase	A_V = +2.0, R_L = 150 Ω, f = 3.58 MHz		0.01		°
TIME DOMAIN RESPONSE						
SR	Slew Rate	A_V = +2.0, V_{step} = 1.0 V		1000		V/μs
t_s	Settling Time 0.01% 0.1%	 A_V = +2.0, V_{step} = 1.0 V A_V = +2.0, V_{step} = 1.0 V		 12 9.0		ns
t_r t_f	Rise and Fall Time	(10%−90%) A_V = +2.0, V_{step} = 1.0 V		2.0		ns
t_{ON}	Turn−on Time			55		ns
t_{OFF}	Turn−off Time			55		ns
HARMONIC/NOISE PERFORMANCE						
THD	Total Harmonic Distortion	f = 5.0 MHz, V_O = 1.0 V_{p-p}		−60		dBc
HD2	2nd Harmonic Distortion	f = 5.0 MHz, V_O = 1.0 V_{p-p}		−62		dBc
HD3	3rd Harmonic Distortion	f = 5.0 MHz, V_O = 1.0 V_{p-p}		−66		dBc
IP3	Third−Order Intercept	f = 10 MHz, V_O = .5 V_{p-p}		28		dBm
SFDR	Spurious−Free Dynamic Range	f = 5.0 MHz, V_O = 1.0 V_{p-p}		55		dBc
e_N	Input Referred Voltage Noise	f = 1.0 MHz		6.0		$nV/\sqrt{Hz}$
i_N	Input Referred Current Noise	f = 1.0 MHz, Inverting f = 1.0 MHz, Non−Inverting		10 3.0		$pA/\sqrt{Hz}$

DC ELECTRICAL CHARACTERISTICS (V_{CC} = +2.5 V, V_{EE} = −2.5 V, T_A = −40°C to +85°C, R_L = 150 Ω to GND, R_F = 400 Ω, A_V = +2.0, Enable is left open, unless otherwise specified).

Symbol	Characteristic	Conditions	Min	Typ	Max	Unit
DC PERFORMANCE						
V_{IO}	Input Offset Voltage		−5.0	0	+5.0	mV
$\Delta V_{IO}/\Delta T$	Input Offset Voltage Temperature Coefficient			6.0		μV/°C
I_{IB}	Input Bias Current	+Input (Non−Inverting), V_O = 0 V −Input (Inverting), V_O = 0 V (Note 5)		±3.0 ±6.0		μA
$\Delta I_{IB}/\Delta T$	Input Bias Current Temperature Coefficient	+Input (Non−Inverting), V_O = 0 V −Input (Inverting), V_O = 0 V		+40 −10		nA/°C
V_{IH}	Input High Voltage (Enable) (Note 5)		1.875			V
V_{IL}	Input Low Voltage (Enable) (Note 5)				−1.875	V
INPUT CHARACTERISTICS						
V_{CM}	Input Common Mode Voltage Range			±1.0		V
CMRR	Common Mode Rejection Ratio	(See Graph)		55		dB
R_{IN}	Input Resistance	+Input (Non−Inverting) −Input (Inverting)		100 50		kΩ Ω
C_{IN}	Differential Input Capacitance			1.0		pF
OUTPUT CHARACTERISTICS						
R_{OUT}	Output Resistance			0.1		Ω
V_O	Output Voltage Range			±1.2		V
I_O	Output Current		±90	±120		mA
POWER SUPPLY						
V_S	Operating Voltage Supply Range			5.0		V
$I_{S,ON}$	Power Supply Current − Enabled	V_O = 0 V		8.0		mA
$I_{S,OFF}$	Power Supply Current − Disabled	V_O = 0 V		0.09		mA
PSRR	Power Supply Rejection Ratio	(See Graph)		60		dB

5. Guaranteed by design and/or characterization.

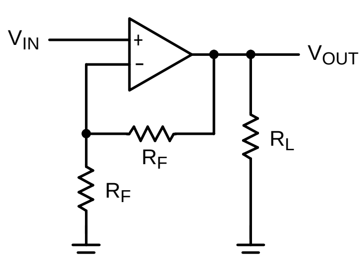


Figure 4. Typical Test Setup
(A_V = +2.0, R_F = 400 Ω, R_L = 150 Ω)

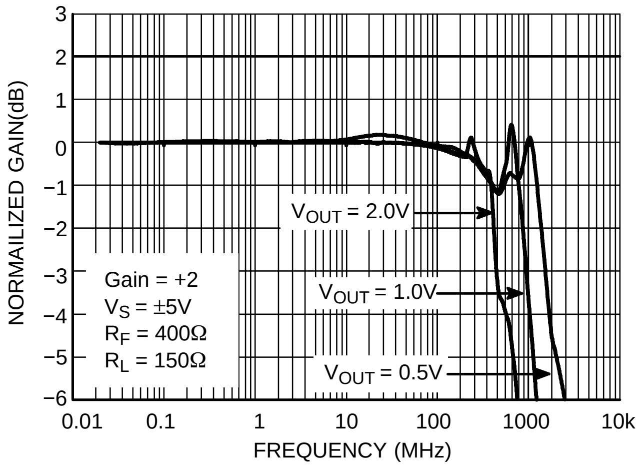


Figure 5. Frequency Response:
Gain (dB) vs. Frequency
Av = +2.0

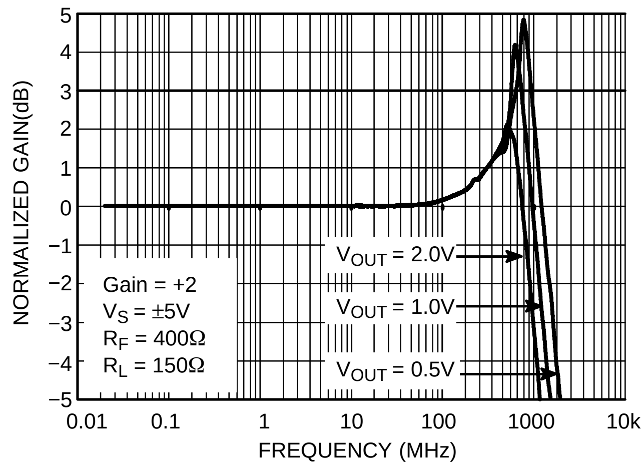


Figure 6. Frequency Response:
Gain (dB) vs. Frequency
Av = +1.0

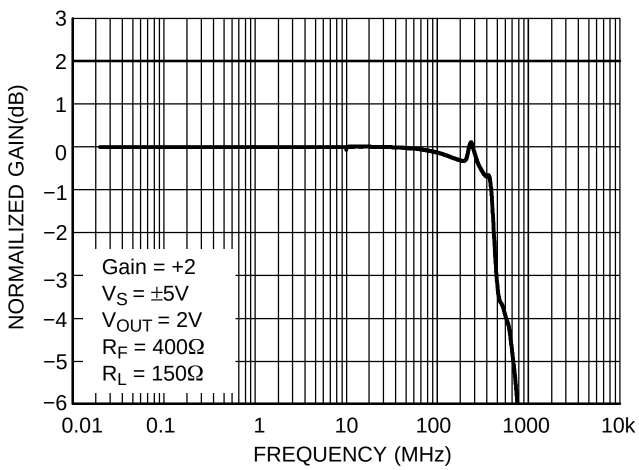


Figure 7. Large Signal Frequency Response
Gain (dB) vs. Frequency

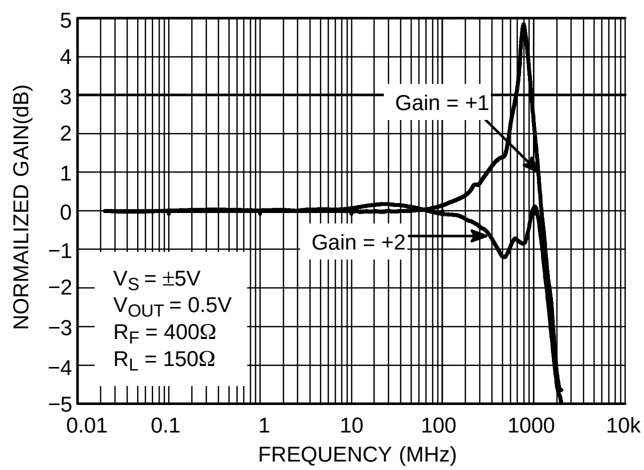


Figure 8. Small Signal Frequency Response
Gain (dB) vs. Frequency

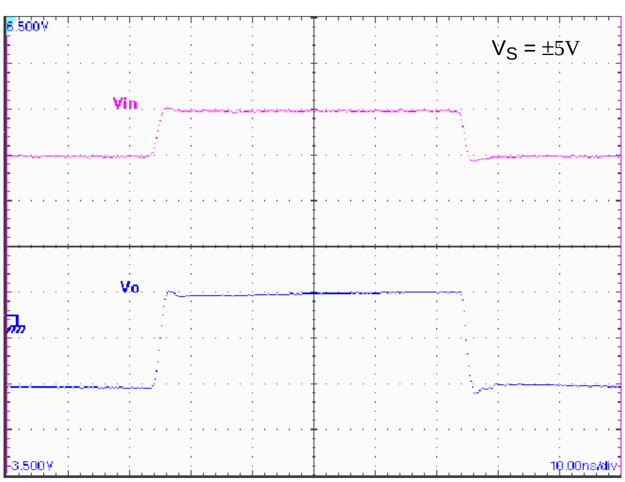


Figure 9. Small Signal Step Response
Vertical: 1V/div
Horizontal: 10ns/div

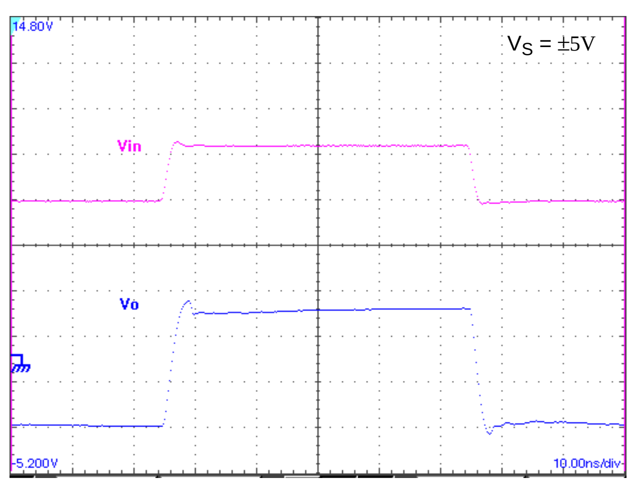


Figure 10. Large Signal Step Response
Vertical: 2V/div
Horizontal: 10ns/div

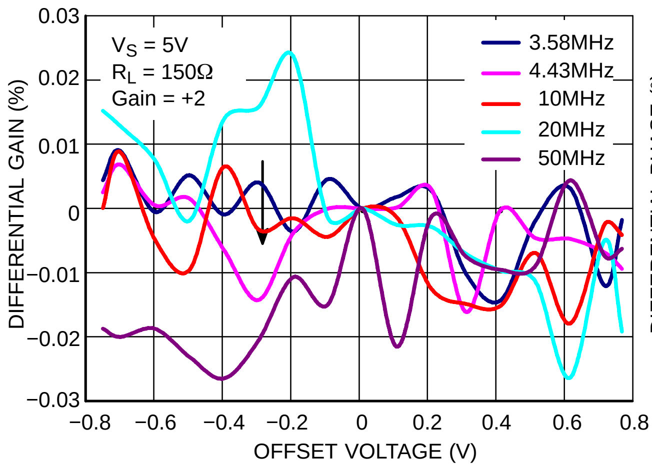


Figure 11. Differential Gain

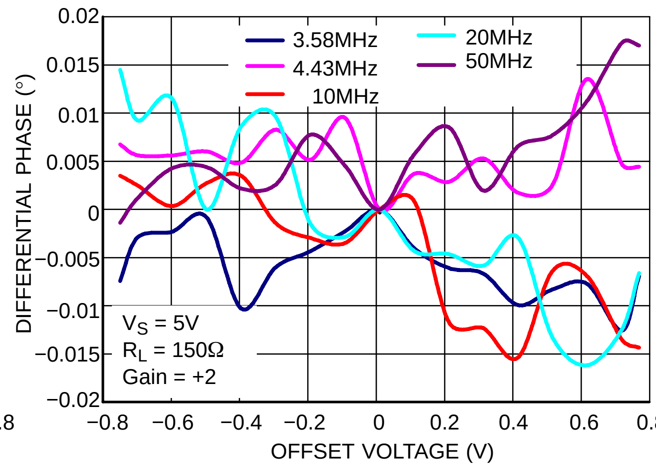


Figure 12. Differential Phase

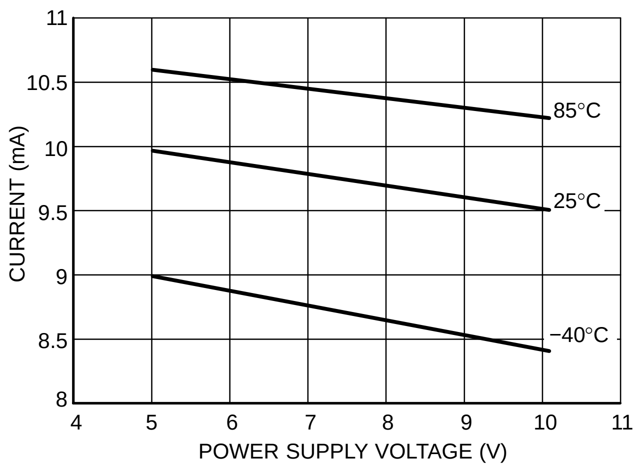


Figure 13. Supply Current vs. Power Supply (Enabled)

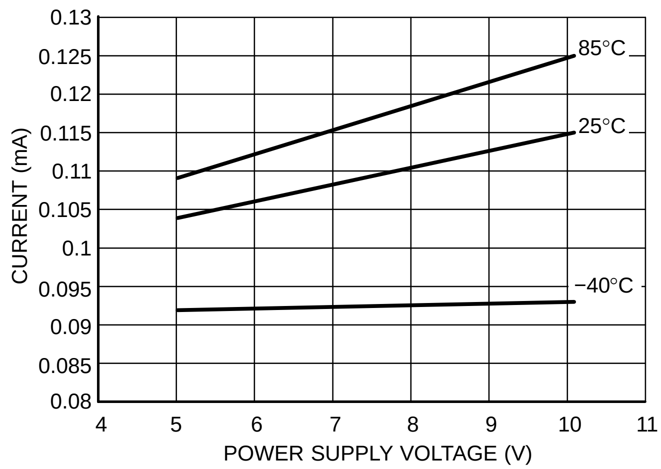


Figure 14. Supply Current vs. Temperature (Disabled)

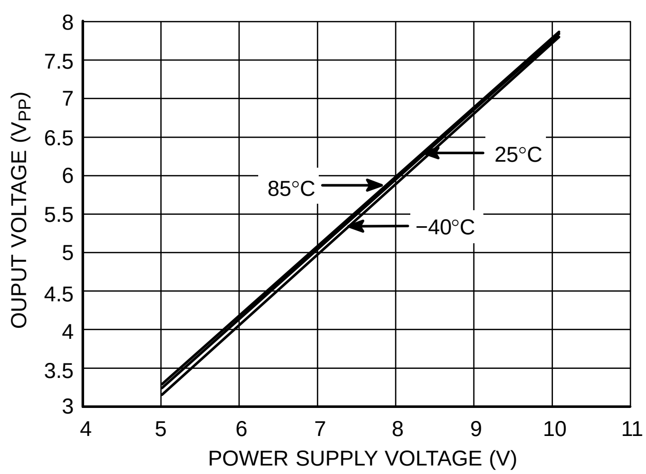


Figure 15. Output Voltage Swing vs. Supply Voltage

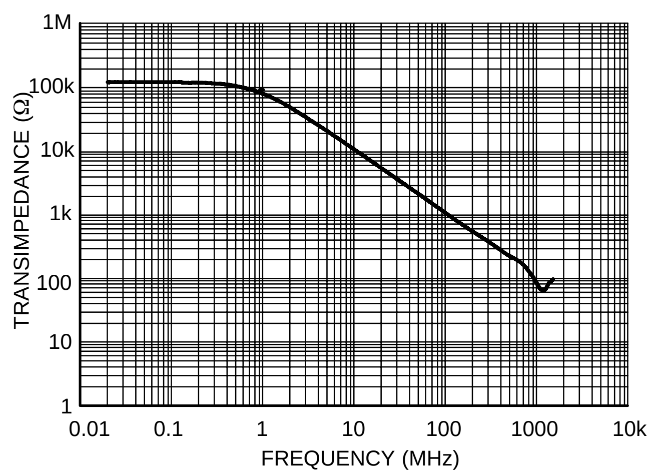


Figure 16. Transimpedance (ROL) vs. Frequency

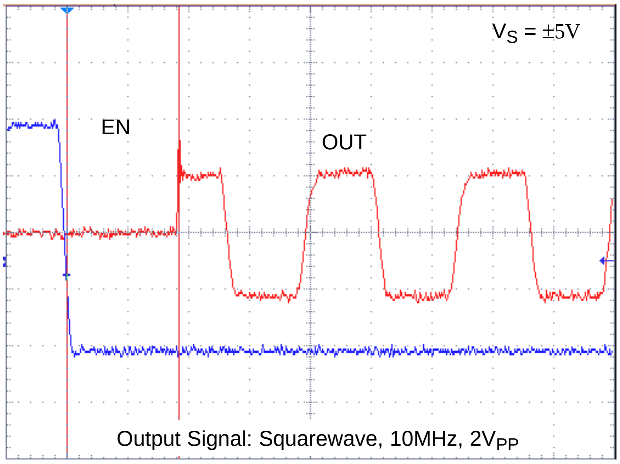


Figure 17. Turn ON Time Delay
Vertical: (EN) 500mV/div (OUT) 1V/div
Horizontal: 40ns/div

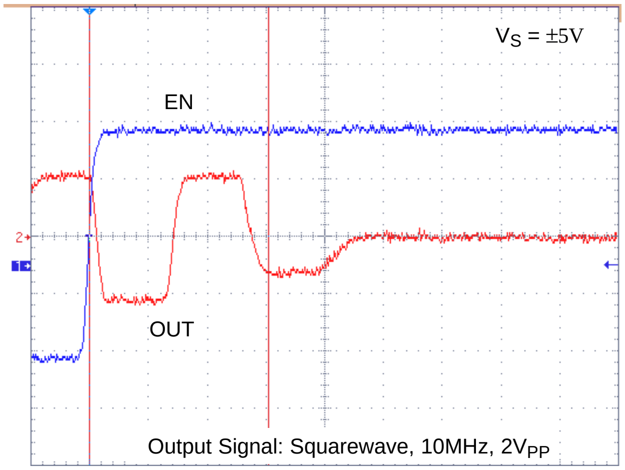


Figure 18. Turn OFF Time Delay
Vertical: (EN) 500mV/div (OUT) 1V/div
Horizontal: 40ns/div

General Design Considerations

The current feedback amplifier is optimized for use in high performance video and data acquisition systems. For current feedback architecture, its closed−loop bandwidth depends on the value of the feedback resistor. The closed−loop bandwidth is not a strong function of gain, as is for a voltage feedback amplifier, as shown in Figure 19.

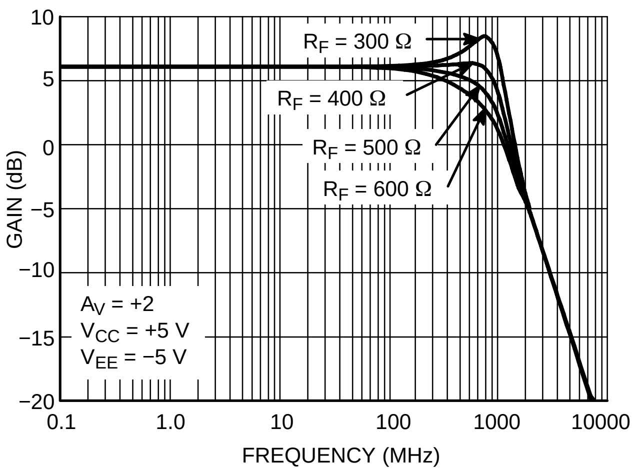


Figure 19. Frequency Response vs. R_F

The −3.0 dB bandwidth is, to some extent, dependent on the power supply voltages. By using lower power supplies, the bandwidth is reduced, because the internal capacitance increases. Smaller values of feedback resistor can be used at lower supply voltages, to compensate for this affect.

Feedback and Gain Resistor Selection for Optimum Frequency Response

A current feedback operational amplifier's key advantage is the ability to maintain optimum frequency response independent of gain by using appropriate values for the feedback resistor. To obtain a very flat gain response, the feedback resistor tolerance should be considered as well. Resistor tolerance of 1% should be used for optimum flatness. Normally, lowering RF resistor from its recommended value will peak the frequency response and extend the bandwidth while increasing the value of RF resistor will cause the frequency response to roll off faster. Reducing the value of RF resistor too far below its recommended value will cause overshoot, ringing, and eventually oscillation.

Since each application is slightly different, it is worth some experimentation to find the optimal RF for a given circuit. A value of the feedback resistor that produces ∼0.1 dB of peaking is the best compromise between stability and maximal bandwidth. It is not recommended to use a current feedback amplifier with the output shorted directly to the inverting input.

Printed Circuit Board Layout Techniques

Proper high speed PCB design rules should be used for all wideband amplifiers as the PCB parasitics can affect the overall performance. Most important are stray capacitances at the output and inverting input nodes as it can effect peaking and bandwidth. A space (3/16″ is plenty) should be left around the signal lines to minimize coupling. Also, signal lines connecting the feedback and gain resistors should be short enough so that their associated inductance does not cause high frequency gain errors. Line lengths less than 1/4″ are recommended.

Video Performance

This device designed to provide good performance with NTSC, PAL, and HDTV video signals. Best performance is obtained with back terminated loads as performance is degraded as the load is increased. The back termination reduces reflections from the transmission line and effectively masks transmission line and other parasitic capacitances from the amplifier output stage.

ESD Protection

All device pins have limited ESD protection using internal diodes to power supplies as specified in the attributes table (see Figure 20). These diodes provide moderate protection to input overdrive voltages above the supplies. The ESD diodes can support high input currents with current limiting series resistors. Keep these resistor values as low as possible since high values degrade both noise performance and frequency response. Under closed−loop operation, the ESD diodes have no effect on circuit performance. However, under certain conditions the ESD diodes will be evident. If the device is driven into a slewing condition, the ESD diodes will clamp large differential voltages until the feedback loop restores closed−loop operation. Also, if the device is powered down and a large input signal is applied, the ESD diodes will conduct.

NOTE: Human Body Model for +IN and –IN pins are rated at 0.8kV while all other pins are rated at 2.0kV.

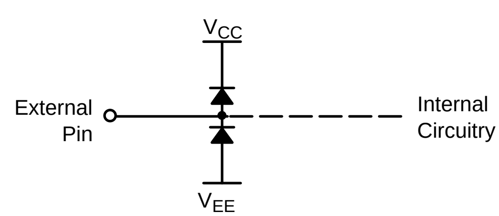


Figure 20. Internal ESD Protection

ORDERING INFORMATION

Device	Package	Shipping†
NCS2510SNT2	SOT23−6 (TSOP−6)	3000 Tape & Reel
NCS2510SNT2G	SOT23−6 (TSOP−6) (Pb−Free)	3000 Tape & Reel
NCS2510D*	SO−8	98 Units/Rail
NCS2510DR2*	SO−8	2500 Tape & Reel
NCS2510DG*	SO−8 (Pb−Free)	98 Units/Rail
NCS2510DR2G*	SO−8 (Pb−Free)	2500 Tape & Reel

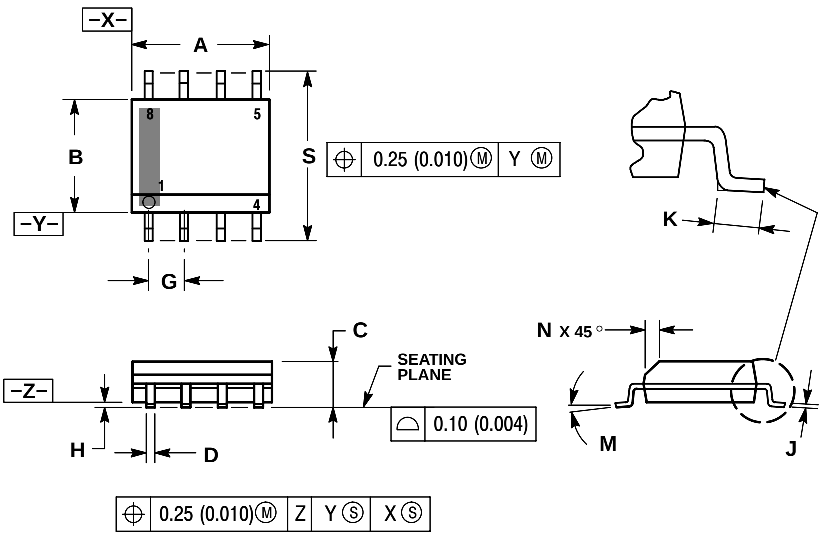
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*Contact ON Semiconductor for ordering information.

NCS2510

PACKAGE DIMENSIONS

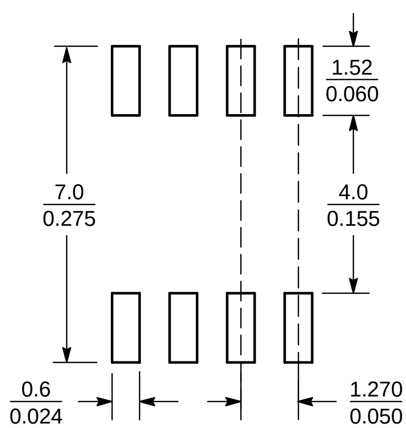
SO−8
D SUFFIX
CASE 751−07
ISSUE AG



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751−01 THRU 751−06 ARE OBSOLETE. NEW STANDARD IS 751−07.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0°	8°	0°	8°
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

SOLDERING FOOTPRINT*



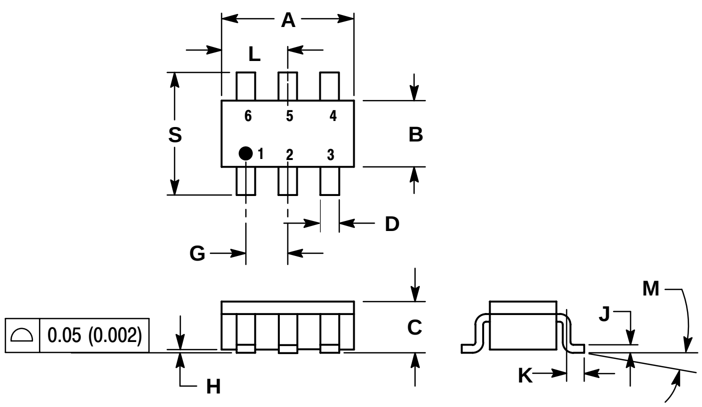
SCALE 6:1 (mm / inches)

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

NCS2510

PACKAGE DIMENSIONS

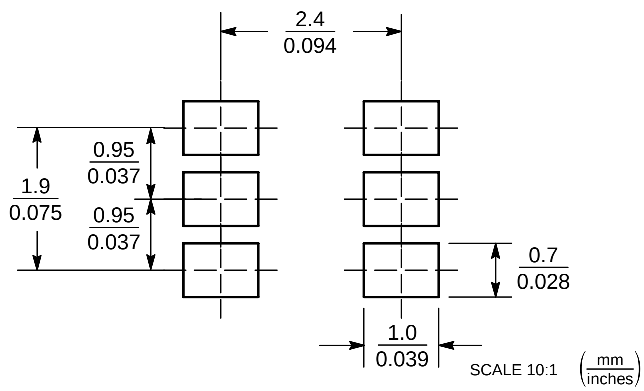
SOT23−6 (TSOP−6)
SN SUFFIX
CASE 318G−02
ISSUE M



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	2.90	3.10	0.1142	0.1220
B	1.30	1.70	0.0512	0.0669
C	0.90	1.10	0.0354	0.0433
D	0.25	0.50	0.0098	0.0197
G	0.85	1.05	0.0335	0.0413
H	0.013	0.100	0.0005	0.0040
J	0.10	0.26	0.0040	0.0102
K	0.20	0.60	0.0079	0.0236
L	1.25	1.55	0.0493	0.0610
M	0 °	10 °	0 °	10 °
S	2.50	3.00	0.0985	0.1181

SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
P.O. Box 61312, Phoenix, Arizona 85082−1312 USA
Phone: 480−829−7710 or 800−344−3860 Toll Free USA/Canada
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