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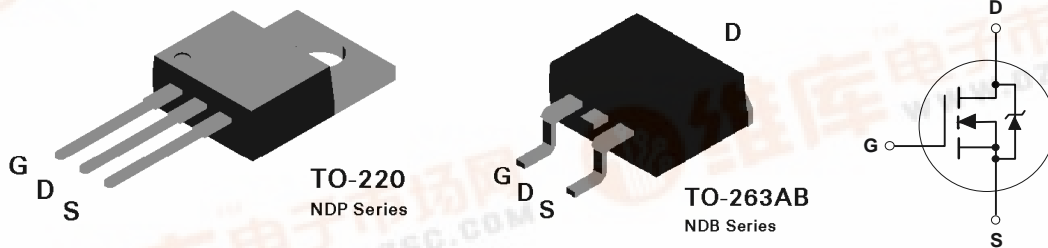
NDP4050L / NDB4050L N-Channel Logic Level Enhancement Mode Field Effect Transistor

General Description

These logic level N-Channel enhancement mode power field effect transistors are produced using Fairchild's proprietary, high cell density, DMOS technology. This very high density process has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulses in the avalanche and commutation modes. These devices are particularly suited for low voltage applications such as automotive, DC/DC converters, PWM motor controls, and other battery powered circuits where fast switching, low in-line power loss, and resistance to transients are needed.

Features

- 15A, 50V. $R_{DS(ON)} = 0.1\Omega @ V_{GS} = 5V$
- Low drive requirements allowing operation directly from logic drivers. $V_{GS(TH)} < 2.0V$.
- Critical DC electrical parameters specified at elevated temperature.
- Rugged internal source-drain diode can eliminate the need for an external Zener diode transient suppressor.
- 175°C maximum junction temperature rating.
- High density cell design for extremely low $R_{DS(ON)}$.
- TO-220 and TO-263 (D²PAK) package for both through hole and surface mount applications.



Absolute Maximum Ratings T_c = 25°C unless otherwise noted

Symbol	Parameter	NDP4050L	NDB4050L	Units
V _{DSS}	Drain-Source Voltage	50	50	V
V _{DGR}	Drain-Gate Voltage (R _{GS} ≤ 1 MΩ)	50	50	V
V _{GSS}	Gate-Source Voltage - Continuous - Nonrepetitive (t _p < 50 μs)	± 16	± 16	V
		± 25	± 25	
I _b	Drain Current - Continuous - Pulsed	15	15	A
		45	45	
P _D	Total Power Dissipation @ T _c = 25°C Derate above 25°C	50	50	W
		0.33	0.33	
T _J , T _{STG}	Operating and Storage Temperature	-65 to 175	-65 to 175	°C
T _L	Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds	275	275	°C

Electrical Characteristics ($T_c = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units	
DRAIN-SOURCE AVALANCHE RATINGS (Note 1)							
W_{DSS}	Single Pulse Drain-Source Avalanche Energy	$V_{DD} = 25\text{ V}$, $I_D = 15\text{ A}$			40	mJ	
I_{AR}	Maximum Drain-Source Avalanche Current				15	A	
OFF CHARACTERISTICS							
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}$, $I_D = 250\ \mu\text{A}$	50			V	
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 50\text{ V}$, $V_{GS} = 0\text{ V}$			250	μA	
			$T_J = 125^\circ\text{C}$		1	mA	
I_{GSSF}	Gate - Body Leakage, Forward	$V_{GS} = 16\text{ V}$, $V_{DS} = 0\text{ V}$			100	nA	
I_{GSSR}	Gate - Body Leakage, Reverse	$V_{GS} = -16\text{ V}$, $V_{DS} = 0\text{ V}$			-100	nA	
ON CHARACTERISTICS (Note 1)							
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}$, $I_D = 250\ \mu\text{A}$	1	1.5	2	V	
			$T_J = 125^\circ\text{C}$	0.65	1.1		1.5
$R_{DS(on)}$	Static Drain-Source On-Resistance	$V_{GS} = 5\text{ V}$, $I_D = 7.5\text{ A}$		0.085	0.1	Ω	
			$T_J = 125^\circ\text{C}$		0.14		0.16
			$V_{GS} = 10\text{ V}$, $I_D = 15\text{ A}$		0.07		0.08
$I_{D(on)}$	On-State Drain Current	$V_{GS} = 5\text{ V}$, $V_{DS} = 10\text{ V}$	15			A	
g_{FS}	Forward Transconductance	$V_{DS} = 10\text{ V}$, $I_D = 7.5\text{ A}$	3	8		S	
DYNAMIC CHARACTERISTICS							
C_{iss}	Input Capacitance	$V_{DS} = 25\text{ V}$, $V_{GS} = 0\text{ V}$, $f = 1.0\text{ MHz}$		510	600	pF	
C_{oss}	Output Capacitance			170	200	pF	
C_{rss}	Reverse Transfer Capacitance			50	100	pF	
SWITCHING CHARACTERISTICS (Note 1)							
$t_{D(on)}$	Turn - On Delay Time	$V_{DD} = 30\text{ V}$, $I_D = 15\text{ A}$, $V_{GS} = 5\text{ V}$, $R_{GEN} = 51\ \Omega$, $R_{GS} = 51\ \Omega$		9	20	nS	
t_r	Turn - On Rise Time			151	250	nS	
$t_{D(off)}$	Turn - Off Delay Time			35	100	nS	
t_f	Turn - Off Fall Time			61	150	nS	
Q_g	Total Gate Charge		$V_{DS} = 48\text{ V}$, $I_D = 15\text{ A}$, $V_{GS} = 5\text{ V}$		11	17	nC
Q_{gs}	Gate-Source Charge			2		nC	
Q_{gd}	Gate-Drain Charge			6.1		nC	

Electrical Characteristics ($T_c = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
DRAIN-SOURCE DIODE CHARACTERISTICS						
I_S	Maximum Continuous Drain-Source Diode Forward Current				15	A
I_{SM}	Maximum Pulsed Drain-Source Diode Forward Current				45	A
V_{SD}	Drain-Source Diode Forward Voltage	$V_{GS} = 0\text{ V}$, $I_S = 7.5\text{ A}$ (Note 1)		0.95	1.3	V
			$T_J = 125^\circ\text{C}$	0.88	1.2	
t_{rr}	Reverse Recovery Time	$V_{GS} = 0\text{ V}$, $I_F = 15\text{ A}$, $di_F/dt = 100\text{ A}/\mu\text{s}$		51	100	ns
I_{rr}	Reverse Recovery Current			3.6	7	A
THERMAL CHARACTERISTICS						
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case				3	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient				62.5	$^\circ\text{C}/\text{W}$

Note:

1. Pulse Test: Pulse Width $\leq 300\ \mu\text{s}$, Duty Cycle $\leq 2.0\%$.

Typical Electrical Characteristics

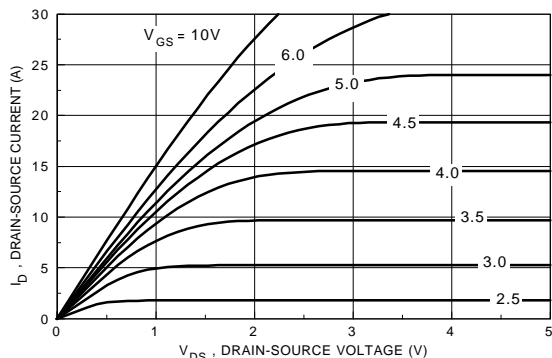


Figure 1. On-Region Characteristics

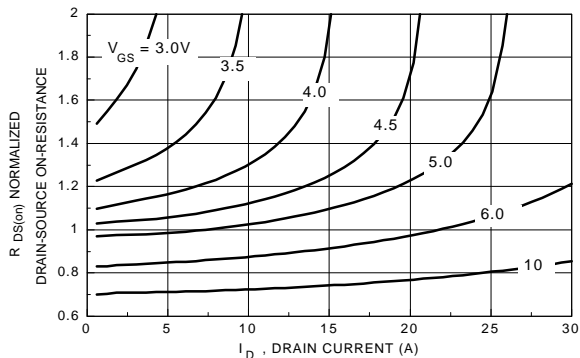


Figure 2. On-Resistance Variation with Gate Voltage and Drain Current

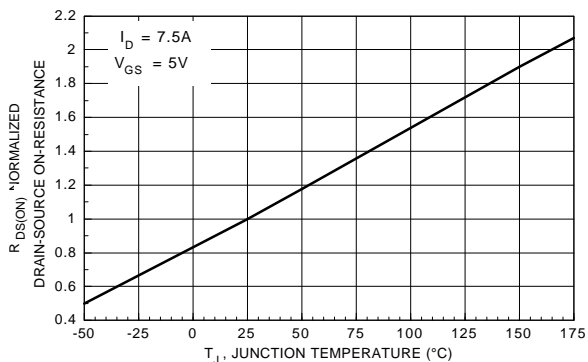


Figure 3. On-Resistance Variation with Temperature

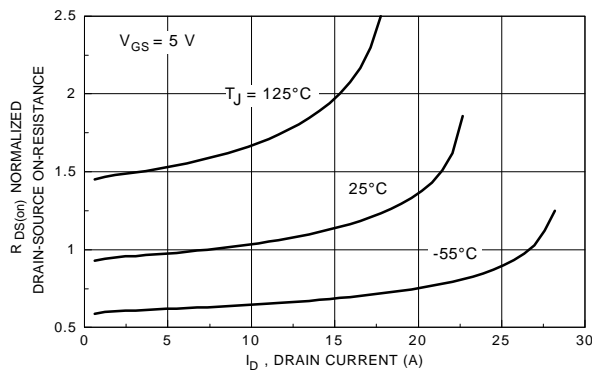


Figure 4. On-Resistance Variation with Drain Current and Temperature

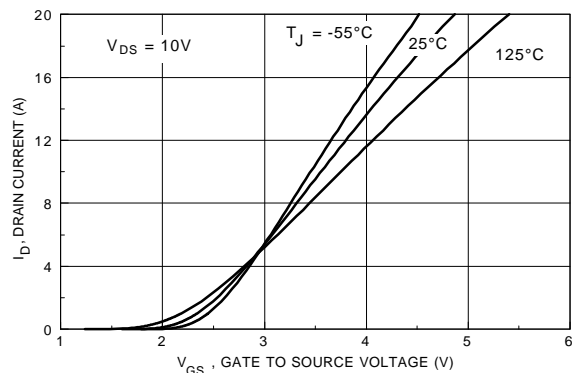


Figure 5. Transfer Characteristics

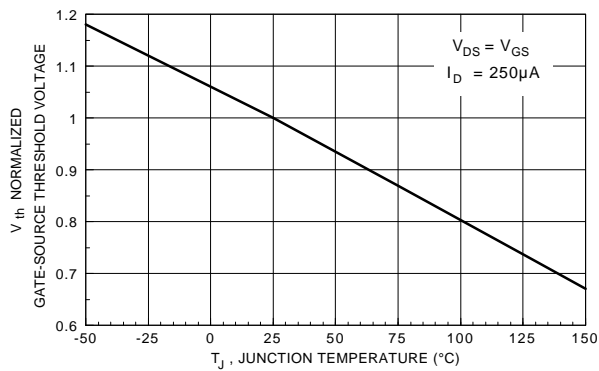


Figure 6. Gate Threshold Variation with Temperature

Typical Electrical Characteristics (continued)

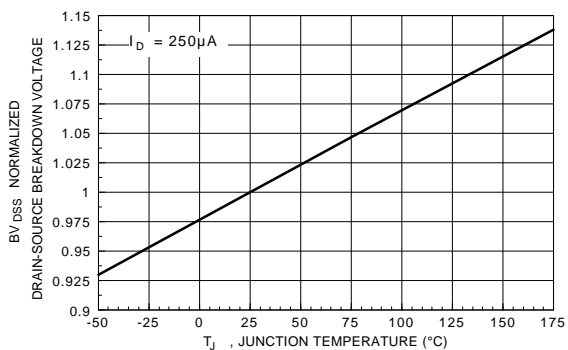


Figure 7. Breakdown Voltage Variation with Temperature

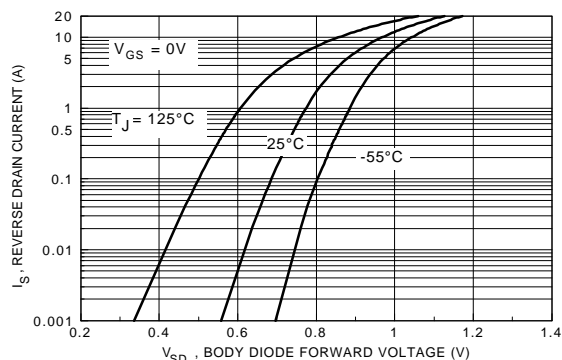


Figure 8. Body Diode Forward Voltage Variation with Current and Temperature

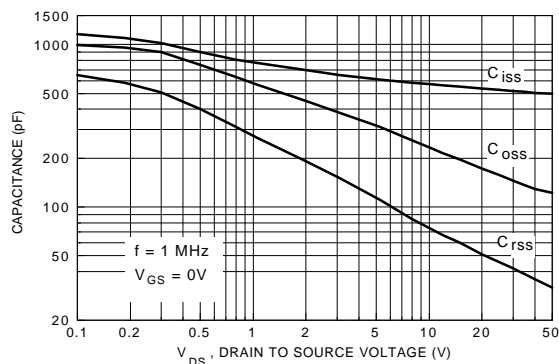


Figure 9. Capacitance Characteristics

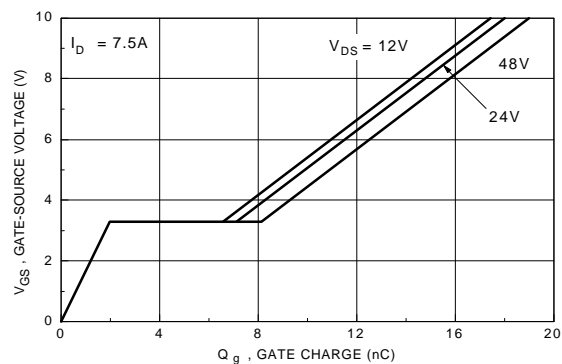


Figure 10. Gate Charge Characteristics

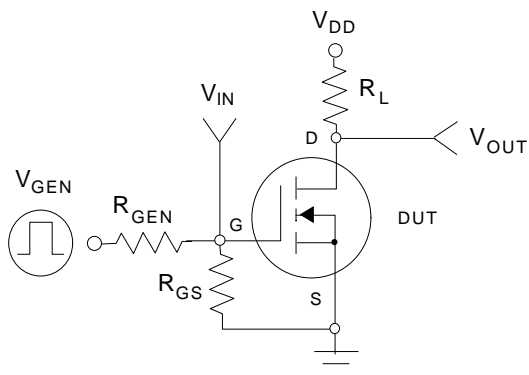


Figure 11. Switching Test Circuit

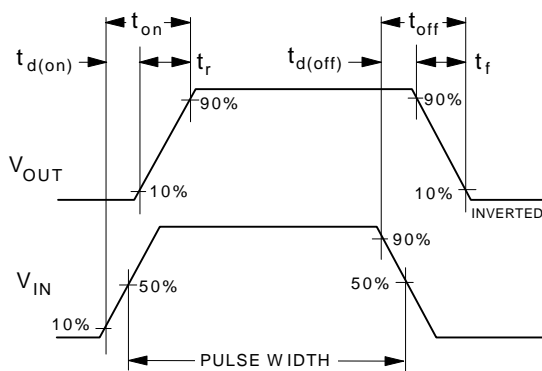


Figure 12. Switching Waveforms

Typical Electrical Characteristics (continued)

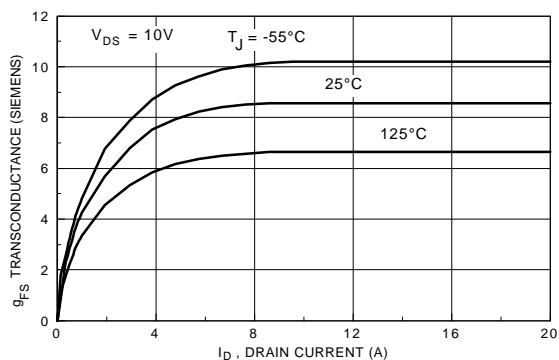


Figure 13. Transconductance Variation with Drain Current and Temperature

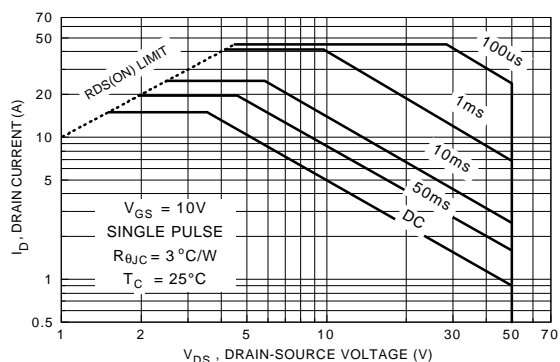


Figure 14. Maximum Safe Operating Area

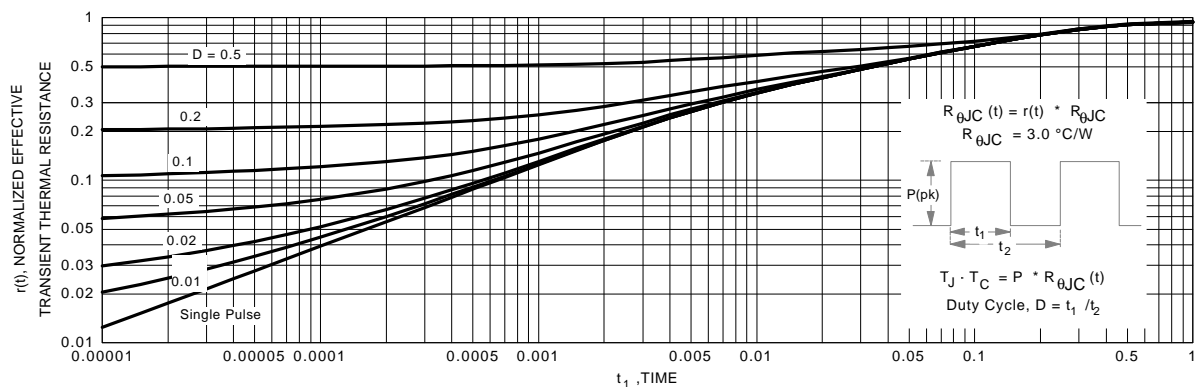


Figure 15. Transient Thermal Response Curve