

October 1996

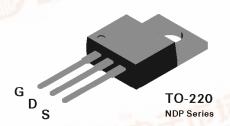
# NDP5060L / NDB5060L N-Channel Logic Level Enhancement Mode Field Effect Transistor

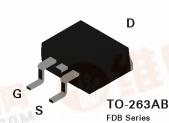
## **General Description**

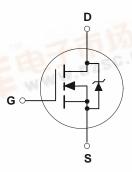
These logic level N-Channel enhancement mode power field effect transistors are produced using Fairchild's proprietary, high cell density, DMOS technology. This very high density process has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulses in the avalanche and commutation modes. These devices are particularly suited for low voltage applications such as automotive, DC/DC converters, PWM motor controls, and other battery powered circuits where fast switching, low in-line power loss, and resistance to transients are needed.

#### **Features**

- Critical DC electrical parameters specified at elevated temperature.
- Rugged internal source-drain diode can eliminate the need for an external Zener diode transient suppressor.
- 175°C maximum junction temperature rating.
- High density cell design for extremely low R<sub>DS(ON)</sub>.
- TO-220 and TO-263 (D<sup>2</sup>PAK) package for both through hole and surface mount applications.







## Absolute Maximum Ratings

 $T_{\rm C}$  = 25°C unless otherwise noted

Symbol	Parameter	NDP5060L	NDB5060L	Units			
V <sub>DSS</sub>	Drain-Source Voltage	60					
$V_{DGR}$	Drain-Gate Voltage ( $R_{\text{GS}} \leq 1 \text{ M}\Omega$ )	60 60					
V <sub>GSS</sub>	Gate-Source Voltage - Continuous	±16					
	- Nonrepetitive (t <sub>P</sub> < 50 μs)	±25	5				
I <sub>D</sub>	Drain Current - Continuous	26		Α			
	- Pulsed	78					
P <sub>D</sub>	Total Power Dissipation @ T <sub>C</sub> = 25°C	68		W			
140 1	Derate above 25°C	0.49	5	W/°C			
$T_J$ , $T_{STG}$	Operating and Storage Temperature Range	-65 to	175	°C			

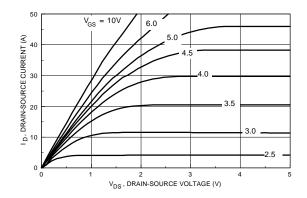


Symbol	Parameter	Conditions			Тур	Max	Units
DRAIN-S	OURCE AVALANCHE RATINGS (Note 1)	<u> </u>		•			
W <sub>DSS</sub>	Single Pulse Drain-Source Avalanche Energy	$V_{DD} = 30 \text{ V, } I_{D} = 26 \text{ A}$				100	mJ
I <sub>AR</sub>	Maximum Drain-Source Avalanche Curre	ent				26	Α
OFF CH	ARACTERISTICS						
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	$V_{GS} = 0 \text{ V}, I_{D} = 250 \mu\text{A}$		60			V
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	$V_{DS} = 60 \text{ V}, V_{GS} = 0 \text{ V}$				250	μA
			T <sub>J</sub> = 125°C			1	mA
I <sub>GSSF</sub>	Gate - Body Leakage, Forward	$V_{GS} = 16 \text{ V}, V_{DS} = 0 \text{ V}$	•			100	nA
I <sub>GSSR</sub>	Gate - Body Leakage, Reverse	$V_{GS} = -16 \text{ V}, V_{DS} = 0 \text{ V}$				-100	nA
ON CHAI	RACTERISTICS (Note 1)	<u> </u>		•			
V <sub>GS(th)</sub>	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_{D} = 250 \mu\text{A}$		1	1.4	2	V
			T <sub>J</sub> = 125°C	0.65	1	1.5	
R <sub>DS(ON)</sub>	Static Drain-Source On-Resistance	$V_{GS} = 5 \text{ V}, I_{D} = 13 \text{ A}$			0.042	0.05	Ω
			T <sub>J</sub> = 125°C		0.07	80.0	
		$V_{GS} = 10 \text{ V}, I_{D} = 13 \text{ A}$	•		0.031	0.035	Ī
I <sub>D(on)</sub>	On-State Drain Current	$V_{GS} = 5 \text{ V}, V_{DS} = 10 \text{ V}$		26			Α
<b>g</b> <sub>FS</sub>	Forward Transconductance	$V_{DS} = 10 \text{ V}, I_{D} = 13 \text{ A}$			16		S
DYNAMI	C CHARACTERISTICS						
$C_{iss}$	Input Capacitance	$V_{DS} = 30 \text{ V}, \ V_{GS} = 0 \text{ V}, $ f = 1.0 MHz			840		pF
C <sub>oss</sub>	Output Capacitance	7 f = 1.0 MHz			230		pF
C <sub>rss</sub>	Reverse Transfer Capacitance	7			75		pF
	NG CHARACTERISTICS (Note 1)	-					
t <sub>D(on)</sub>	Turn - On Delay Time	$V_{DD} = 30 \text{ V}, I_D = 26 \text{ A},$			13	20	nS
t,	Turn - On Rise Time	$V_{GS} = 5 \text{ V}, R_{GEN} = 30 \Omega$		200	400	nS	
t <sub>D(off)</sub>	Turn - Off Delay Time	$ R_{GS} = 30 \Omega$			45	80	nS
t <sub>f</sub>	Turn - Off Fall Time				102	200	nS
$Q_g$	Total Gate Charge	V <sub>DS</sub> = 24 V,			17	24	nC
$Q_{gs}$	Gate-Source Charge	$I_D = 26 \text{ A}, V_{GS} = 5 \text{ V}$			4		nC
$Q_{gd}$	Gate-Drain Charge			10		nC	

Symbol	Parameter	Conditions	Min	Тур	Max	Units
DRAIN-S	OURCE DIODE CHARACTERISTICS		·			
I <sub>s</sub>	Maximum Continuos Drain-Source Diode			26	Α	
I <sub>SM</sub>	Maximum Pulsed Drain-Source Diode Fo			78	Α	
$V_{SD}$	Drain-Source Diode Forward Voltage	V <sub>GS</sub> = 0 V, I <sub>S</sub> = 13 A (Note 1)		0.9	1.3	V
t <sub>rr</sub>	Reverse Recovery Time	$V_{GS} = 0 \text{ V}, I_F = 26 \text{ A},$		54	120	ns
I <sub>rr</sub>	Reverse Recovery Current	$\frac{1}{dl_F} dt = 100 \text{ A/} \mu \text{s}$		2.1	8	Α
THERMA	AL CHARACTERISTICS		·			
R <sub>ØJC</sub>	Thermal Resistance, Junction-to-Case			2.2	°C/W	
R <sub>OJA</sub>	Thermal Resistance, Junction-to-Ambien			62.5	°C/W	

Note:  $1. \ \text{Pulse Test: Pulse Width} \leq 300 \ \mu\text{s, Duty Cycle} \leq 2.0\%.$ 

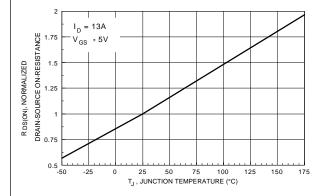
# **Typical Electrical Characteristics**



2 V<sub>GS</sub> = 3.0 V V<sub>GS</sub> = 3.0 V

Figure 1. On-Region Characteristics.

Figure 2. On-Resistance Variation with Gate Voltage and Drain Current.



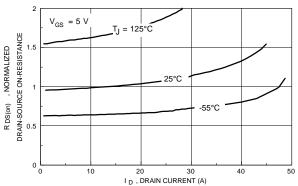
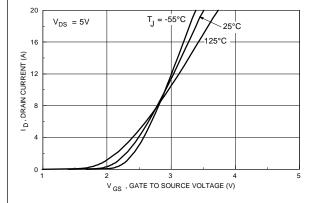


Figure 3. On-Resistance Variation with Temperature.

Figure 4. On-Resistance Variation with Drain Current and Temperature.



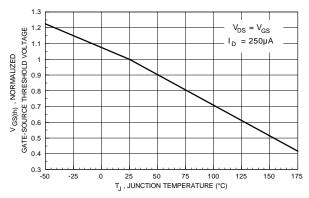


Figure 5. Transfer Characteristics.

Figure 6. Gate Threshold Variation with Temperature.

# **Typical Electrical Characteristics (continued)**

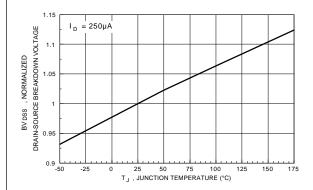


Figure 7. Breakdown Voltage Variation with Temperature.

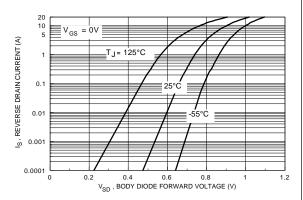


Figure 8. Body Diode Forward Voltage
Variation with Current and Temperature.

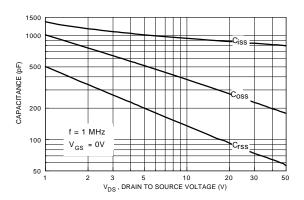


Figure 9. Capacitance Characteristics.

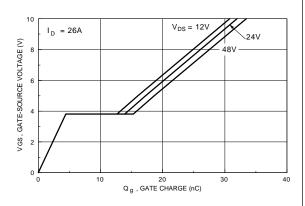


Figure 10. Gate Charge Characteristics.

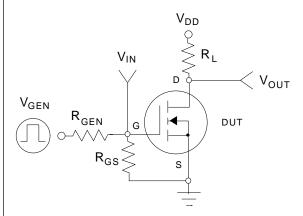


Figure 11. Switching Test Circuit.

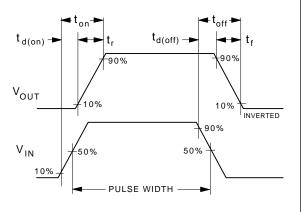
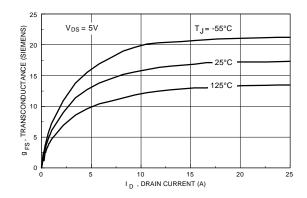


Figure 12. Switching Waveforms.

# **Typical Electrical Characteristics (continued)**



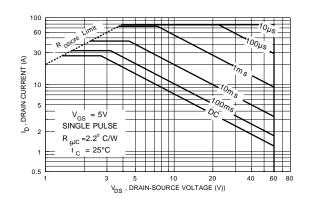


Figure 13. Transconductance Variation with Drain Current and Temperature.

Figure 14. Maximum Safe Operating Area.

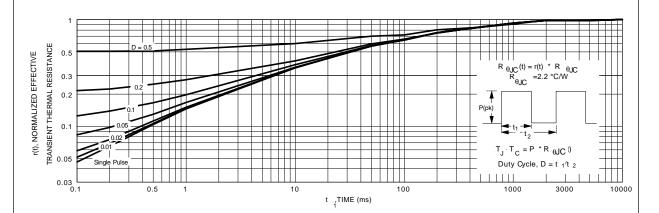
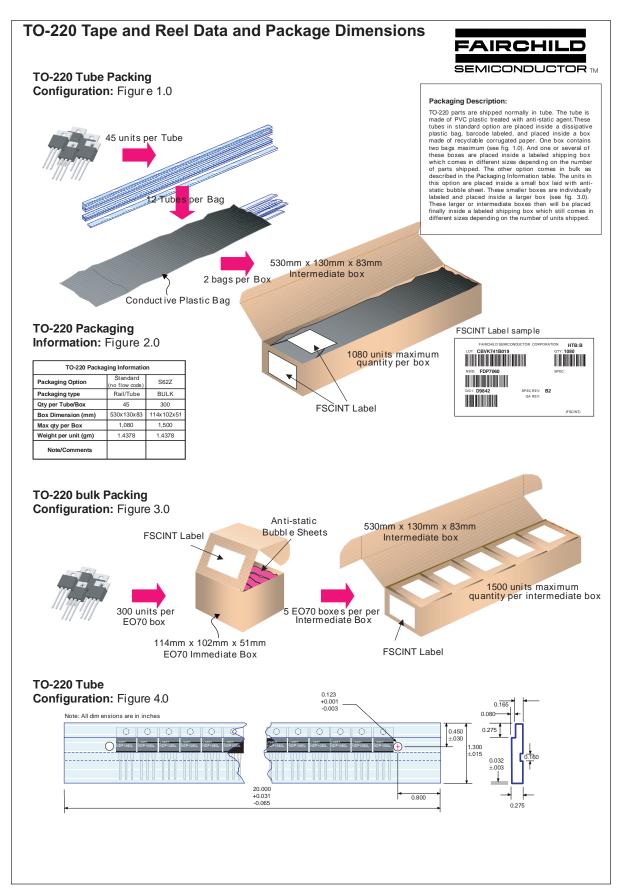
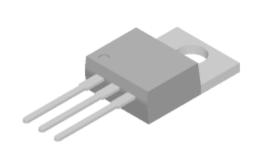


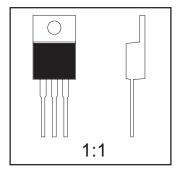
Figure 15. Transient Thermal Response Curve.



# TO-220 Tape and Reel Data and Package Dimensions, continued

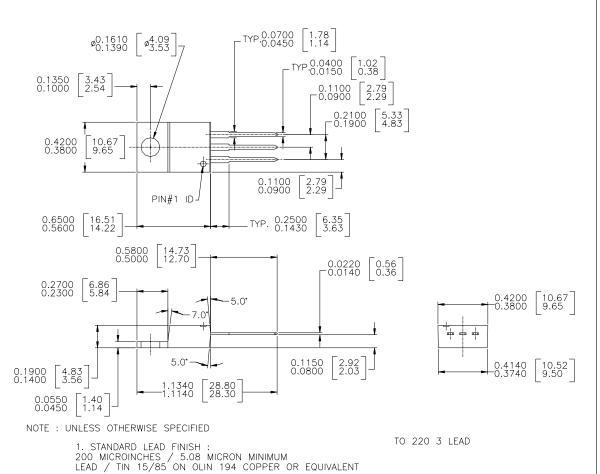
# TO-220 (FS PKG Code 37)



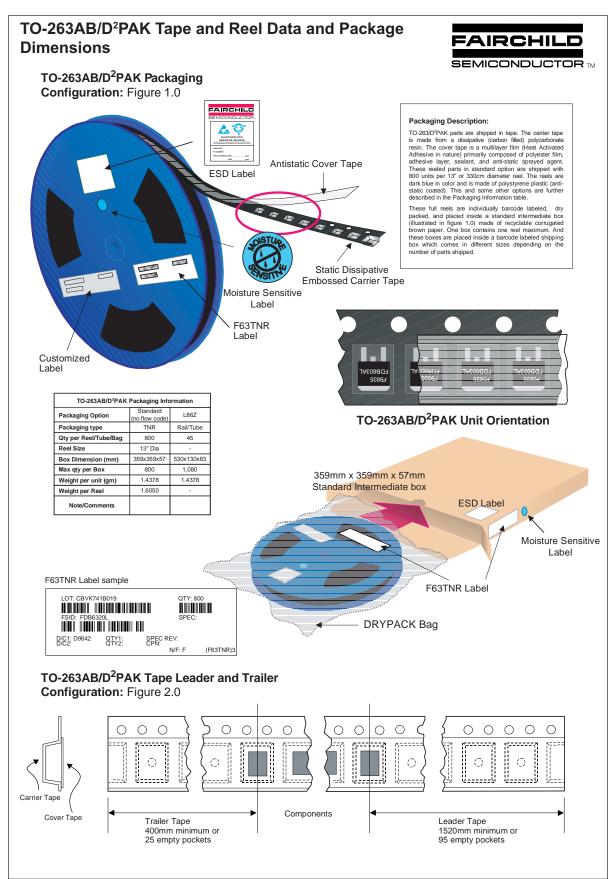


Scale 1:1 on letter size paper
Dimensions shown below are in:
inches [millimeters]

Part Weight per unit (gram): 1.4378

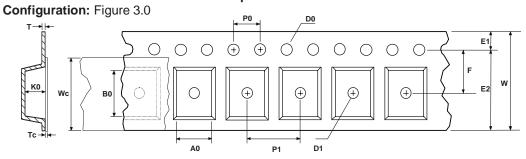


2. DIMENSION BASED ON JEDEC STANDARD TO-220 VARIATION AB, ISSUE J, DATED 3/24/87



# TO-263AB/D<sup>2</sup>PAK Tape and Reel Data and Package Dimensions, continued

# TO-263AB/D<sup>2</sup>PAK Embossed Carrier Tape



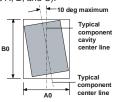
# User Direction of Feed

Dimensions are in millimeter														
Pkg type	Α0	В0	w	D0	D1	E1	E2	F	P1	P0	K0	Т	Wc	Тс
TO263AB/ D <sup>2</sup> PAK (24mm)	10.60 +/-0.10	15.80 +/-0.10	24.0 +/-0.3	1.55 +/-0.05	1.60 +/-0.10	1.75 +/-0.10	22.25 min	11.50 +/-0.10	16.0 +/-0.1	4.0 +/-0.1	4.90 +/-0.10	0.450 +/-0.150	21.0 +/-0.3	0.06 +/-0.02

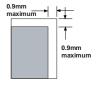
Notes: A0, B0, and K0 dimensions are determined with respect to the EIA/Jedec RS-481 rotational and lateral movement requirements (see sketches A, B, and C).



Sketch A (Side or Front Sectional View)
Component Rotation

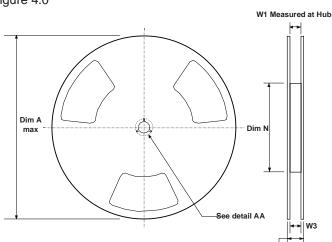


Sketch B (Top View)
Component Rotation

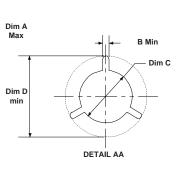


Sketch C (Top View)
Component lateral movement

# **TO-263AB/D<sup>2</sup>PAK Reel Configuration:** Figure 4.0



13" Diameter Option



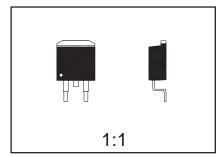
W2 max Measured at Hub

#### Dimensions are in inches and millimeters Reel Tape Size Dim A Dim B Dim C Dim D Dim N Dim W1 Dim W2 Dim W3 (LSL-USL) Option 512 +0.020/-0.008 13 +0.5/-0.2 0.961 +0.078/-0.000 24.4 +2/0 0.941 - 0.1.079 23.9 - 27.4 0.059 1.5 24mm 13" Dia

# TO-263AB/D²PAK Tape and Reel Data and Package Dimensions, continued

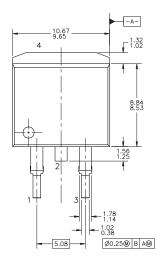
# TO-263AB/D<sup>2</sup>PAK (FS PKG Code 45)

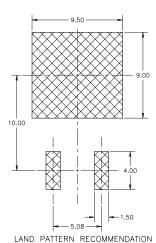


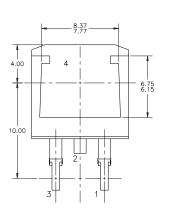


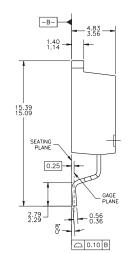
Scale 1:1 on letter size paper Dimensions shown below are in: inches [millimeters]

Part Weight per unit (gram): 1.4378









- NOTES: UNLESS OTHERWISE SPECIFIED

  A) ALL DIMENSIONS ARE IN MILLIMETERS.
  B) STANDARD LEAD FINISH:
  200 MICROINCHES / 5.08 MICROMETERS MIN.
  LEAD/TIN 15/85 ON OLIN 194 COPPER OR
  EQUIVALENT.
  C) MAXIMUM YERTICAL BURR ON HEATSINK NOT
  TO EXCEED 0.003 INCH / 0.05mm.
  D) NO PACKAGE CHIPS, CRACKS OR SURFACE
  IDENTIFICATION ALLOWED AFTER FORMING.
  E) REFERENCE JEDEC, TO—263, ISSUE C,
  VARIATION AB, DATED 2/92.

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Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
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No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
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