

June 1996

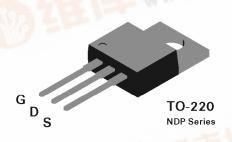
### NDP6030L / NDB6030L N-Channel Logic Level Enhancement Mode Field Effect Transistor

### **General Description**

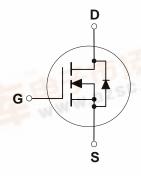
These N-Channel logic level enhancement mode power field effect transistors are produced using Fairchild's proprietary, high cell density, DMOS technology. This very high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage applications such as DC/DC converters and high efficiency switching circuits where fast switching, low in-line power loss, and resistance to transients are needed.

### **Features**

- 52 A, 30 V.  $R_{DS(ON)} = 0.0135 \Omega$  @  $V_{GS} = 10 V$   $R_{DS(ON)} = 0.020 \Omega$  @  $V_{GS} = 4.5 V$ .
- Critical DC electrical parameters specified at elevated temperature.
- Rugged internal source-drain diode can eliminate the need for an external Zener diode transient suppressor.
- High density cell design for extremely low R<sub>DS(ON)</sub>.
- 175°C maximum junction temperature rating.







Absolute Maximum Ratings T<sub>c</sub> = 25°C unless otherwise noted

Symbol	Parameter	NDP6030L	NDB6030L	Units		
V <sub>DSS</sub>	Drain-Source Voltage	30				
V <sub>GSS</sub>	Gate-Source Voltage - Continuous	± 16				
I <sub>D</sub>	Drain Current - Continuous	52				
	- Pulsed	c-\//o 1	56	]		
P <sub>D</sub>	Total Power Dissipation @ T <sub>C</sub> = 25°C	75				
	Derate above 25°C	C	.5	W/°C		
T <sub>J</sub> ,T <sub>STG</sub>	Operating and Storage Temperature Range	-65 to 175				
TL	Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds	2	75	°C		
THERMA	L CHARACTERISTICS					
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	;	2	°C/W		
R <sub>OJA</sub>	Thermal Resistance, Junction-to-Ambient	62.5				

Symbol	Parameter	Conditions		Min	Тур	Max	Units
DRAIN-S	OURCE AVALANCHE RATINGS (Note 1)	•					
W <sub>DSS</sub>	Single Pulse Drain-Source Avalanche En	ergy V <sub>DD</sub> = 15 V, I <sub>D</sub> = 52 A				100	mJ
I <sub>AR</sub>	Maximum Drain-Source Avalanche Curre	nt				52	Α
OFF CHA	ARACTERISTICS			•	•		
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	$V_{GS} = 0 \text{ V}, I_{D} = 250 \mu\text{A}$		30			V
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	$V_{DS} = 24 \text{ V}, \ V_{GS} = 0 \text{ V}$				10	μA
			T <sub>J</sub> = 125°C			1	mA
I <sub>GSSF</sub>	Gate - Body Leakage, Forward	$V_{GS} = 16 \text{ V}, V_{DS} = 0 \text{ V}$				100	nA
I <sub>GSSR</sub>	Gate - Body Leakage, Reverse	$V_{GS} = -16 \text{ V}, V_{DS} = 0 \text{ V}$				-100	nA
ON CHAP	RACTERISTICS (Note 1)	<del>_</del>		•	•		
V <sub>GS(th)</sub>	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_{D} = 250 \mu\text{A}$	$V_{DS} = V_{GS}, I_{D} = 250 \mu\text{A}$			3	V
			$T_J = 125^{\circ}C$	0.7	1	2.2	
R <sub>DS(ON)</sub>	Static Drain-Source On-Resistance	$V_{GS} = 10 \text{ V}, I_{D} = 26 \text{ A}$			0.011	0.0135	Ω
			T <sub>J</sub> = 125°C		0.017	0.024	
		$V_{GS} = 4.5 \text{ V}, I_{D} = 21 \text{ A}$			0.018	0.02	
I <sub>D(on)</sub>	On-State Drain Current	$V_{GS} = 10 \text{ V}, V_{DS} = 10 \text{ V}$		60			Α
		$V_{GS} = 4.5 \text{ V}, V_{DS} = 10 \text{ V}$		15			
g <sub>FS</sub>	Forward Transconductance	$V_{DS} = 10 \text{ V}, I_{D} = 26 \text{ A}$			32		S
DYNAMIC	CCHARACTERISTICS						
C <sub>iss</sub>	Input Capacitance	$V_{DS} = 15 \text{ V}, V_{GS} = 0 \text{ V},$			1350		pF
C <sub>oss</sub>	Output Capacitance	f = 1.0 MHz			800		pF
C <sub>rss</sub>	Reverse Transfer Capacitance				300		pF

Symbol	Parameter	Conditions		Min	Тур	Max	Units
SWITCH	ING CHARACTERISTICS (Note 1)						
t <sub>D(on)</sub>	Tum - On Delay Time	$V_{DD} = 15 \text{ V}, I_{D} = 52 \text{ A},$	$V_{DD} = 15 \text{ V}, I_{D} = 52 \text{ A},$				nS
ţ,	Turn - On Rise Time	$V_{GS}$ = 10 V, $R_{GEN}$ = 24 $\Omega$			130	250	nS
t <sub>D(off)</sub>	Turn - Off Delay Time				45	90	nS
t <sub>r</sub>	Turn - Off Fall Time				108	200	nS
$Q_g$	Total Gate Charge	V <sub>DS</sub> = 10 V			44	60	nC
$Q_{gs}$	Gate-Source Charge	$I_D = 52 \text{ A}, \ V_{GS} = 10 \text{ V}$	$I_D = 52 \text{ A}, \ V_{GS} = 10 \text{ V}$		6		nC
$Q_{gd}$	Gate-Drain Charge						nC
DRAIN-S	OURCE DIODE CHARACTERISTIC	cs					
I <sub>s</sub>	Maximum Continuos Drain-Source			52	Α		
I <sub>SM</sub>	Maximum Pulsed Drain-Source Diode Forward Current					120	Α
V <sub>SD</sub>	Drain-Source Diode Forward Volta	age $V_{GS} = 0 \text{ V}, I_{S} = 26 \text{ A (Note 1)}$			0.93	1.3	V
			T <sub>.</sub> = 125°C		0.85	1.2	]

Note: 1. Pulse Test: Pulse Width ≤ 300 µs, Duty Cycle ≤ 2.0%.

### **Typical Electrical Characteristics**

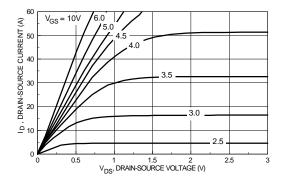


Figure 1. On-Region Characteristics.

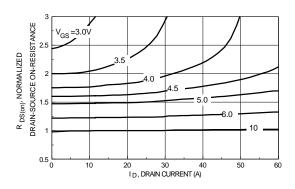


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

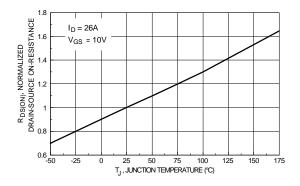


Figure 3. On-Resistance Variation with Temperature.

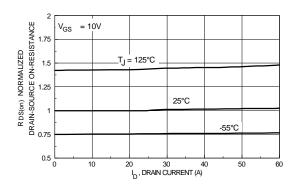


Figure 4. On-Resistance Variation with Drain Current and Temperature.

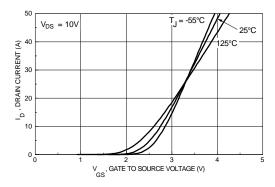


Figure 5. Transfer Characteristics.

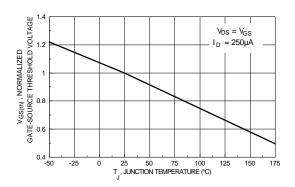


Figure 6. Gate Threshold Variation with Temperature.

### **Typical Electrical Characteristics (continued)**

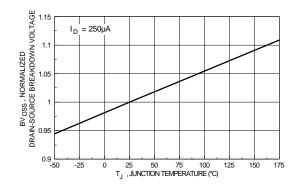


Figure 7. Breakdown Voltage Variation with Temperature.

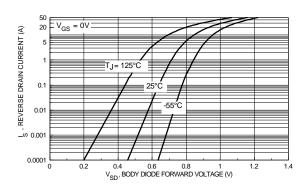


Figure 8. Body Diode Forward Voltage Variation with Source Current and Temperature.

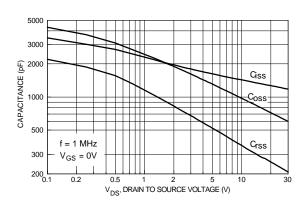


Figure 9. Capacitance Characteristics.

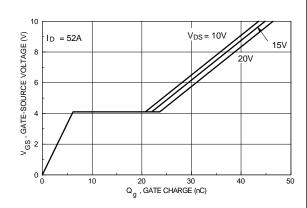


Figure 10. Gate Charge Characteristics.

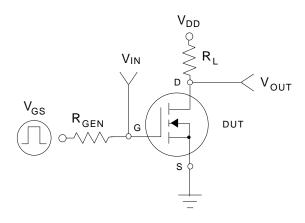


Figure 11. Switching Test Circuit.

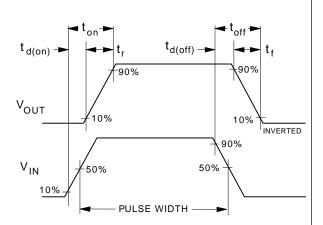
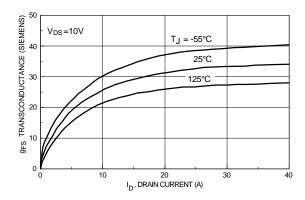


Figure 12. Switching Waveforms.

### Typical Electrical Characteristics (continued)



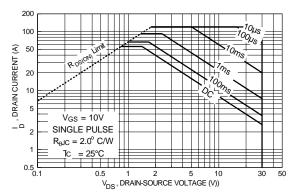


Figure 13. Transconductance Variation with Drain Current and Temperature.

Figure 14. Maximum Safe Operating Area.

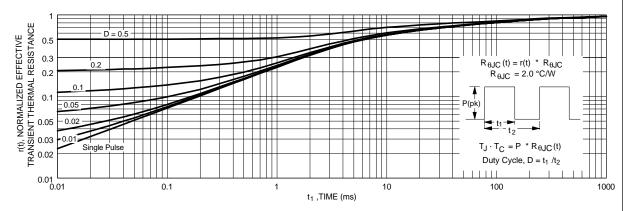
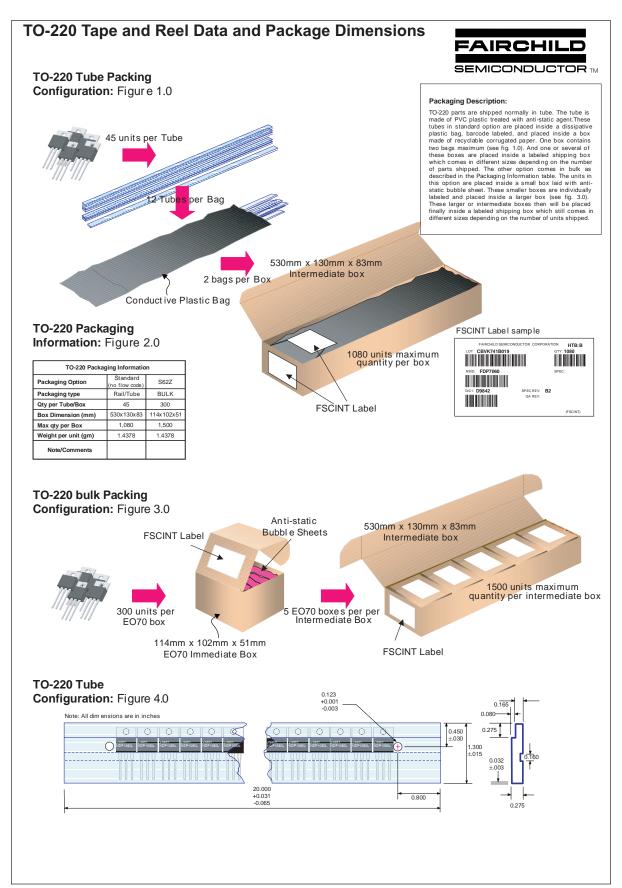
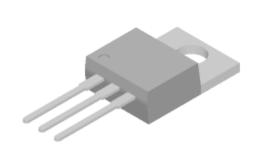


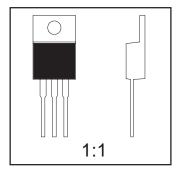
Figure 15. Transient Thermal Response Curve.



### TO-220 Tape and Reel Data and Package Dimensions, continued

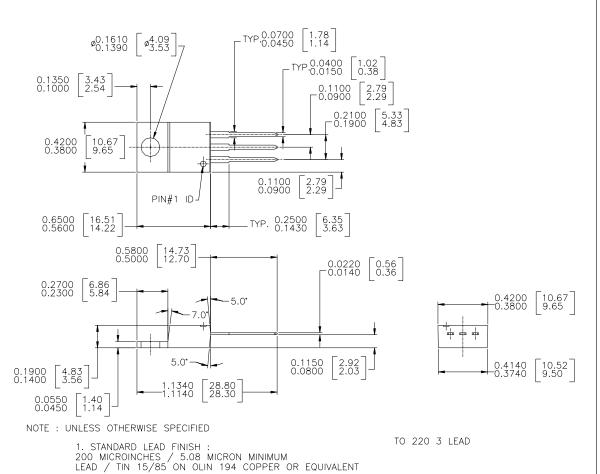
## TO-220 (FS PKG Code 37)



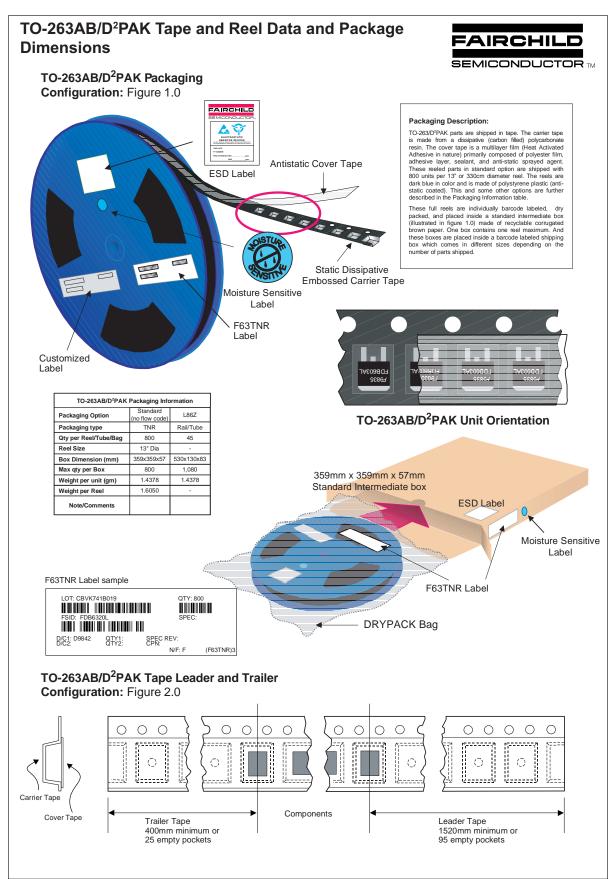


Scale 1:1 on letter size paper
Dimensions shown below are in:
inches [millimeters]

Part Weight per unit (gram): 1.4378

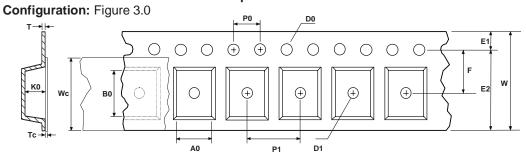


2. DIMENSION BASED ON JEDEC STANDARD TO-220 VARIATION AB, ISSUE J, DATED 3/24/87



### TO-263AB/D<sup>2</sup>PAK Tape and Reel Data and Package Dimensions, continued

## TO-263AB/D<sup>2</sup>PAK Embossed Carrier Tape



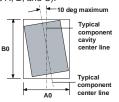
## User Direction of Feed

Dimensions are in millimeter														
Pkg type	Α0	В0	w	D0	D1	E1	E2	F	P1	P0	K0	Т	Wc	Тс
TO263AB/ D <sup>2</sup> PAK (24mm)	10.60 +/-0.10	15.80 +/-0.10	24.0 +/-0.3	1.55 +/-0.05	1.60 +/-0.10	1.75 +/-0.10	22.25 min	11.50 +/-0.10	16.0 +/-0.1	4.0 +/-0.1	4.90 +/-0.10	0.450 +/-0.150	21.0 +/-0.3	0.06 +/-0.02

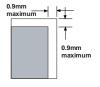
Notes: A0, B0, and K0 dimensions are determined with respect to the EIA/Jedec RS-481 rotational and lateral movement requirements (see sketches A, B, and C).



Sketch A (Side or Front Sectional View)
Component Rotation

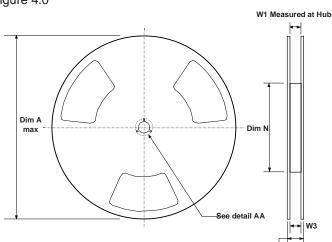


Sketch B (Top View)
Component Rotation

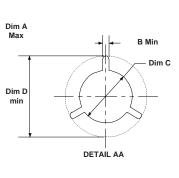


Sketch C (Top View)
Component lateral movement

# **TO-263AB/D<sup>2</sup>PAK Reel Configuration:** Figure 4.0



13" Diameter Option



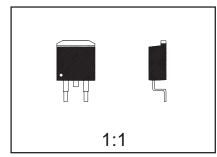
W2 max Measured at Hub

#### Dimensions are in inches and millimeters Reel Tape Size Dim A Dim B Dim C Dim D Dim N Dim W1 Dim W2 Dim W3 (LSL-USL) Option 512 +0.020/-0.008 13 +0.5/-0.2 0.961 +0.078/-0.000 24.4 +2/0 0.941 - 0.1.079 23.9 - 27.4 0.059 1.5 24mm 13" Dia

## TO-263AB/D²PAK Tape and Reel Data and Package Dimensions, continued

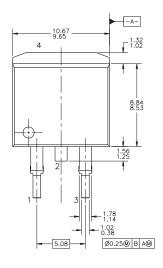
## TO-263AB/D<sup>2</sup>PAK (FS PKG Code 45)

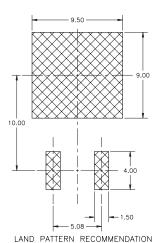


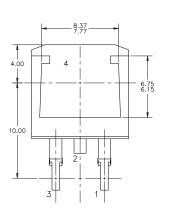


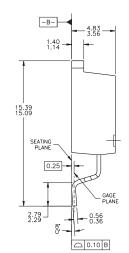
Scale 1:1 on letter size paper Dimensions shown below are in: inches [millimeters]

Part Weight per unit (gram): 1.4378









- NOTES: UNLESS OTHERWISE SPECIFIED

  A) ALL DIMENSIONS ARE IN MILLIMETERS.
  B) STANDARD LEAD FINISH:
  200 MICROINCHES / 5.08 MICROMETERS MIN.
  LEAD/TIN 15/85 ON OLIN 194 COPPER OR
  EQUIVALENT.
  C) MAXIMUM YERTICAL BURR ON HEATSINK NOT
  TO EXCEED 0.003 INCH / 0.05mm.
  D) NO PACKAGE CHIPS, CRACKS OR SURFACE
  IDENTIFICATION ALLOWED AFTER FORMING.
  E) REFERENCE JEDEC, TO—263, ISSUE C,
  VARIATION AB, DATED 2/92.

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Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data, and supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
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